# 74HC7540; 74HCT7540

## Octal Schmitt trigger buffer/line driver; 3-state; inverting

Rev. 4 — 31 December 2012 Product data sheet

## 1. General description

The 74HC7540; 74HCT7540 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74HC7540; 74HCT7540 provides eight inverting buffer/line drivers with 3-state outputs and Schmitt-trigger action. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$. A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state. Schmitt trigger action on the data inputs transforms slowly changing input signals into sharply defined, jitter-free output signals.

The 74HC7540; 74HCT7540 is identical to the 74HC540; 74HCT540 but has hysteresis on the data inputs.

## 2. Features and benefits

- Inverting outputs
- Low-power dissipation
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC7540N | −40 °C to +125 °C | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |
| 74HCT7540N | | | | |
| 74HC7540D | −40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HCT7540D | | | | |
| 74HC7540DB | −40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |

## 4. Functional diagram

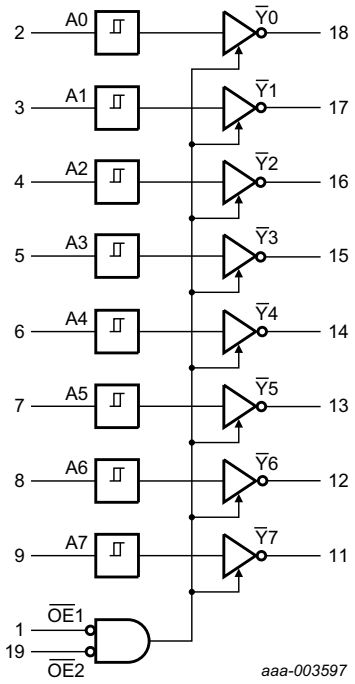



Fig 1. Logic symbol

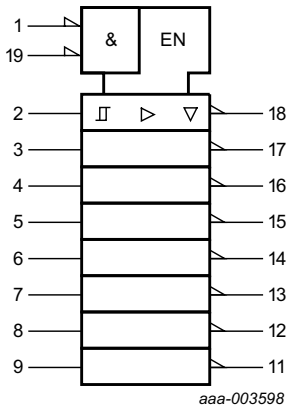



Fig 2. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

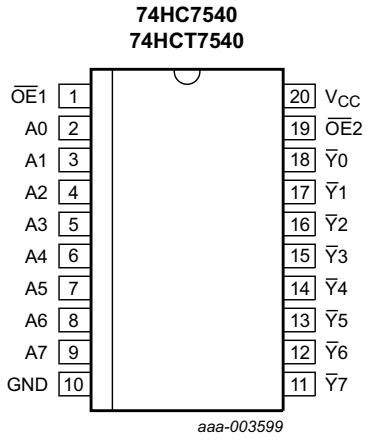



Fig 3. Pin configuration DIP20, SO20

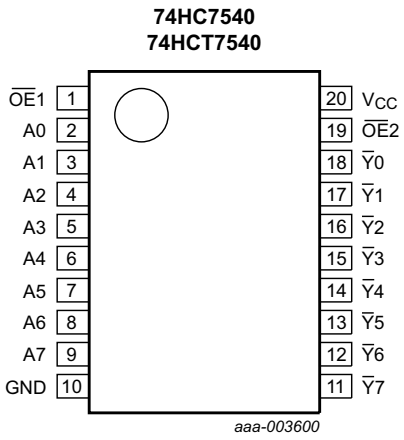



Fig 4. Pin configuration SSOP20

### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}1$ | 1 | output enable input (active LOW) |
| A0 to A7 | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| $\overline{Y}0$ to $\overline{Y}7$ | 18, 17, 16, 15, 14, 13, 12, 11 | data output |
| $\overline{OE}2$ | 19 | output enable input (active LOW) |
| $V_{CC}$ | 20 | supply voltage |

## 6. Functional description

**Table 3. Functional table[1]**

| Control | | Input | Output |
|---|---|---|---|
| $\overline{OE}1$ | $\overline{OE}2$ | An | $\overline{Y}n$ |
| L | L | L | H |
| L | L | H | L |
| X | H | X | Z |
| H | X | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | | - | ±35 | mA |
| $I_{CC}$ | supply current | | | - | 70 | mA |
| $I_{GND}$ | ground current | | | −70 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | | [2] | | | |
| | DIP20 | | | - | 750 | mW |
| | SO20, SSOP20 | | | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of $P_{tot}$ derates linearly with 12 mW/K.
For SO20 packages: above 70 °C the value of $P_{tot}$ derates linearly with 8 mW/K.
For SSOP20 packages: above 60 °C the value of $P_{tot}$ derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | 74HC7540 | | | 74HCT7540 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | +25 | +125 | −40 | +25 | +125 | °C |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = 25 °C | | | $T_{amb}$ = −40 °C to +85 °C | | $T_{amb}$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC7540** | | | | | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | | | |
| | | $I_O$ = −20 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O$ = −6.0 mA; $V_{CC}$ = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_O$ = −7.8 mA; $V_{CC}$ = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 6.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 7.8 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| $I_{OZ}$ | OFF-state output current | per input pin; $V_I = V_{T+}$ or $V_{T-}$; $V_O = V_{CC}$ or GND; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 6.0 V; $I_O$ = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| **74HCT7540** | | | | | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{T+}$ or $V_{T-}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = −20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = −6.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |

**Table 6. Static characteristics** *...continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = 25 °C | | | $T_{amb}$ = –40 °C to +85 °C | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{T+}$ or $V_{T-}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 20 μA; | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 6.0 mA; | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| $I_{OZ}$ | OFF-state output current | per input pin; $V_I = V_{T+}$ or $V_{T-}$; $V_O = V_{CC}$ or GND; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5 V; $I_O$ = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $I_O$ = 0 A; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | An input | - | 20 | 72 | - | 90 | - | 98 | μA |
| | | $\overline{OE}$n input | - | 130 | 468 | - | 585 | - | 637 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; $C_L$ = 50 pF; for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Max (85 °C) | Max (125 °C) | |
| **74HC7540** | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to $\overline{Y}$n; see Figure 5 | [1] | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 39 | 120 | 150 | 180 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 14 | 24 | 30 | 36 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 11 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | | - | 11 | 20 | 26 | 31 | ns |
| $t_{en}$ | enable time | $\overline{OE}$n to $\overline{Y}$n; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 41 | 150 | 190 | 225 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 15 | 30 | 38 | 45 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 12 | 26 | 33 | 38 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$n to $\overline{Y}$n; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 52 | 150 | 190 | 225 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 19 | 30 | 38 | 45 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 15 | 26 | 33 | 38 | ns |

**Table 7. Dynamic characteristics**

*GND = 0 V; $C_L$ = 50 pF; for test circuit see Figure 7.*

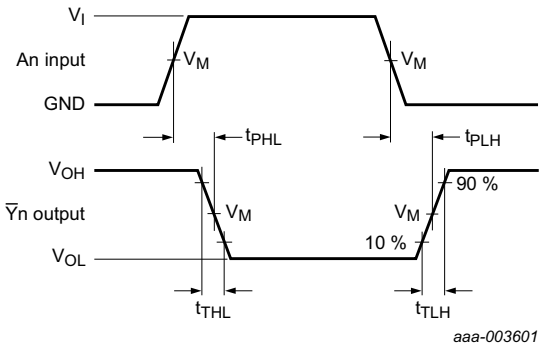
| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Max (85 °C) | Max (125 °C) | |
| $t_t$ | transition time | see Figure 5 | [2] | | | | | | |
| | | $V_{CC}$ = 2.0 V | | - | 14 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 4.5 V | | - | 5 | 12 | 15 | 18 | ns |
| | | $V_{CC}$ = 6.0 V | | - | 4 | 10 | 13 | 15 | ns |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ | [3] | - | 29 | - | - | - | pF |
| **74HCT7540** | | | | | | | | | |
| $t_{pd}$ | propagation delay | An to $\overline{Y}$n; see Figure 5 | [1] | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 19 | 32 | 40 | 48 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 16 | - | - | - | ns |
| $t_{en}$ | enable time | $\overline{OE}$n to $\overline{Y}$n; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 19 | 32 | 40 | 48 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$n to $\overline{Y}$n; see Figure 6 | [1] | | | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 20 | 32 | 40 | 48 | ns |
| $t_t$ | transition time | $V_{CC}$ = 4.5 V; see Figure 5 | [2] | - | 5 | 12 | 15 | 18 | ns |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ – 1.5 V | [3] | - | 31 | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[2] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

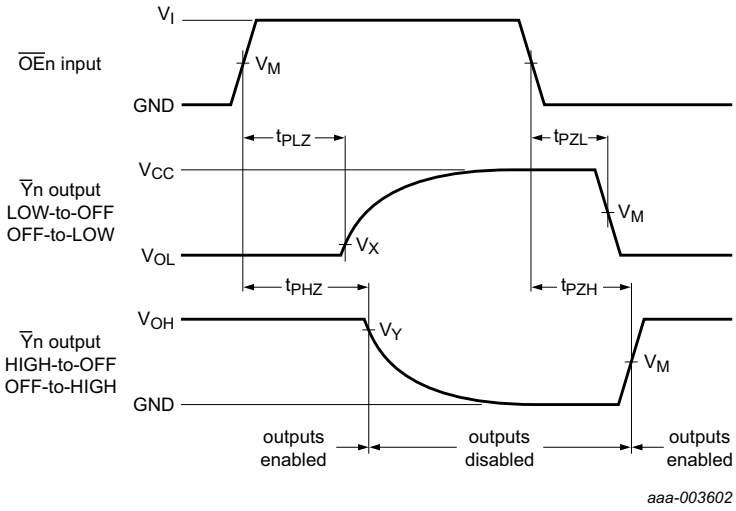
## 11. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 5. Input to output propagation delays**



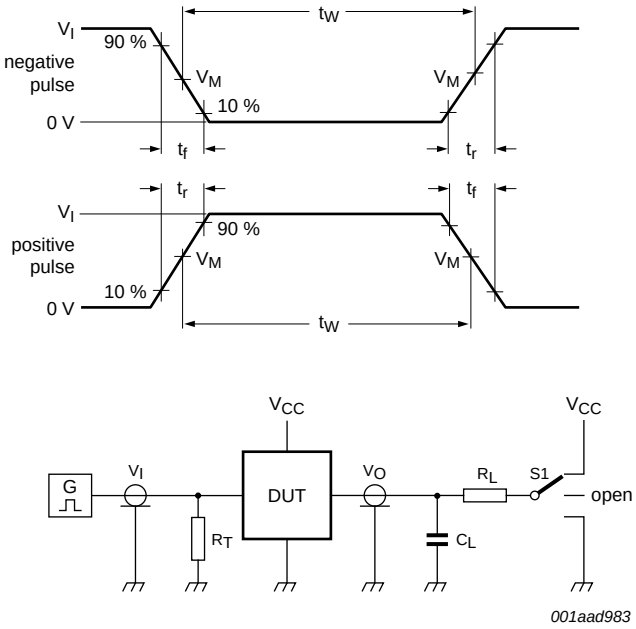

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 6. 3-state enable and disable times**

**Table 8. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 74HC7540 | $0.5V_{CC}$ | $0.5V_{CC}$ | $0.1V_{CC}$ | $0.9V_{CC}$ |
| 74HCT7540 | 1.3 V | 1.3 V | $0.1V_{CC}$ | $0.9V_{CC}$ |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator

$C_L$ = Load capacitance including jig and probe capacitance

$R_L$ = Load resistance

S1 = Test selection switch

**Fig 7. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 74HC7540 | $V_{CC}$ | 6 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |
| 74HCT7540 | 3 V | 6 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |

## 12. Transfer characteristics

**Table 10. Transfer characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Figure 8 and Figure 9.*

| Symbol | Parameter | Conditions | $T_{amb}$ = 25 °C | | | $T_{amb}$ = −40 °C to +85 °C | | $T_{amb}$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC7540** | | | | | | | | | | |
| $V_{T+}$ | positive-going threshold voltage | $V_{CC}$ = 2.0 V | - | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | $V_{CC}$ = 4.5 V | - | - | 3.15 | - | 3.15 | - | 3.15 | V |
| | | $V_{CC}$ = 6.0 V | - | - | 4.2 | - | 4.2 | - | 4.2 | V |
| $V_{T-}$ | negative-going threshold voltage | $V_{CC}$ = 2.0 V | 0.3 | - | - | 0.3 | - | 0.3 | - | V |
| | | $V_{CC}$ = 4.5 V | 1.35 | - | - | 1.35 | - | 1.35 | - | V |
| | | $V_{CC}$ = 6.0 V | 1.8 | - | - | 1.8 | - | 1.8 | - | V |
| $V_H$ | hysteresis voltage | $V_{CC}$ = 2.0 V | 0.1 | 0.20 | - | 0.1 | - | 0.1 | - | V |
| | | $V_{CC}$ = 4.5 V | 0.25 | 0.40 | - | 0.25 | - | 0.25 | - | V |
| | | $V_{CC}$ = 6.0 V | 0.3 | 0.5 | - | 0.3 | - | 0.3 | - | V |
| **74HCT7540** | | | | | | | | | | |
| $V_{T+}$ | positive-going threshold voltage | $V_{CC}$ = 4.5 V | - | - | 2.0 | - | 2.0 | - | 2.0 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 2.1 | - | 2.1 | - | 2.1 | V |
| $V_{T-}$ | negative-going threshold voltage | $V_{CC}$ = 4.5 V | 0.7 | - | - | 0.64 | - | 0.6 | - | V |
| | | $V_{CC}$ = 5.5 V | 0.8 | - | - | 0.74 | - | 0.7 | - | V |
| $V_H$ | hysteresis voltage | $V_{CC}$ = 4.5 V | 0.17 | 0.23 | - | - | - | - | - | V |
| | | $V_{CC}$ = 5.5 V | 0.17 | 0.23 | - | - | - | - | - | V |

## 13. Transfer characteristics waveforms

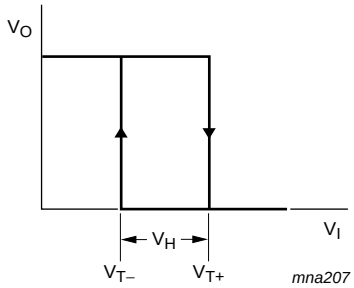



**Fig 8. Transfer characteristics**

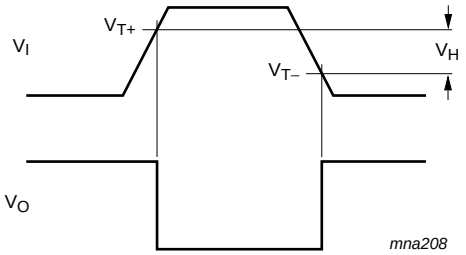
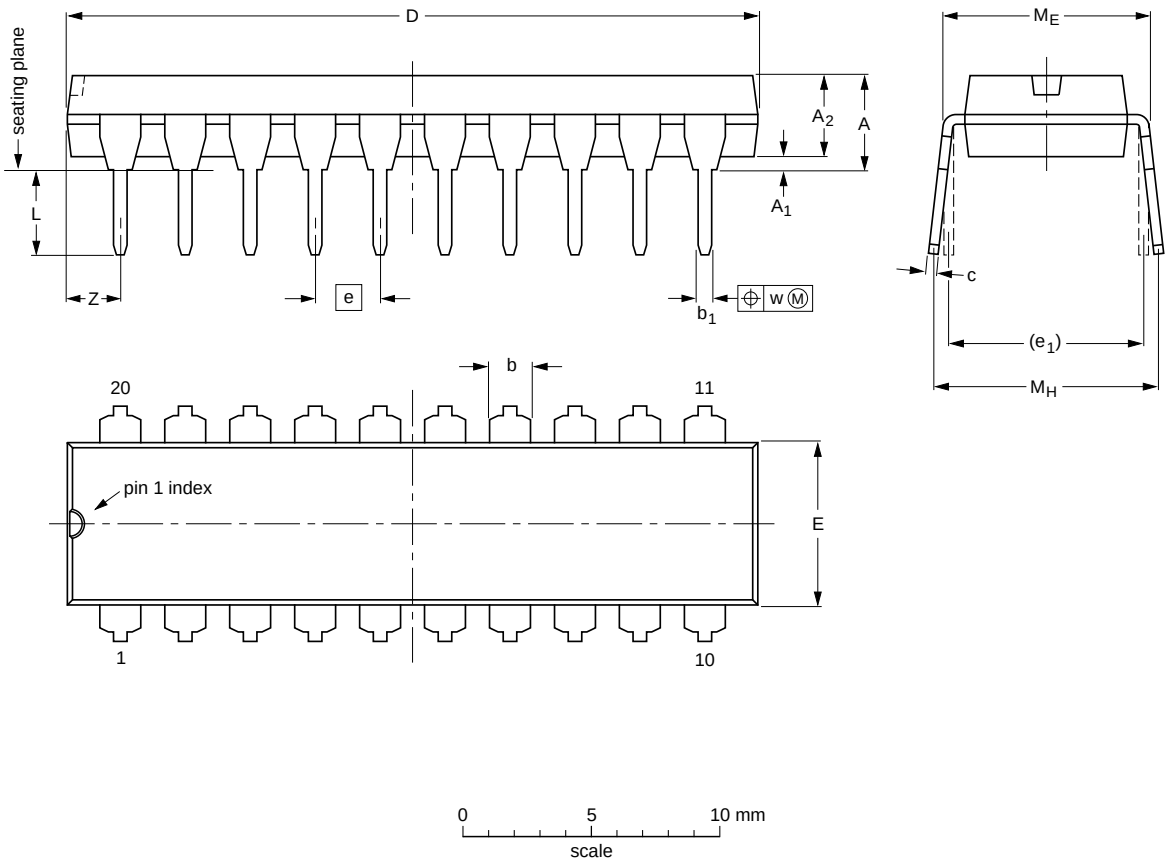



**Fig 9. Transfer characteristics definitions**

## 14. Package outline

**DIP20: plastic dual in-line package; 20 leads (300 mil)** **SOT146-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 0.36<br>0.23 | 26.92<br>26.54 | 6.40<br>6.22 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 2 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045 | 0.25<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.078 |

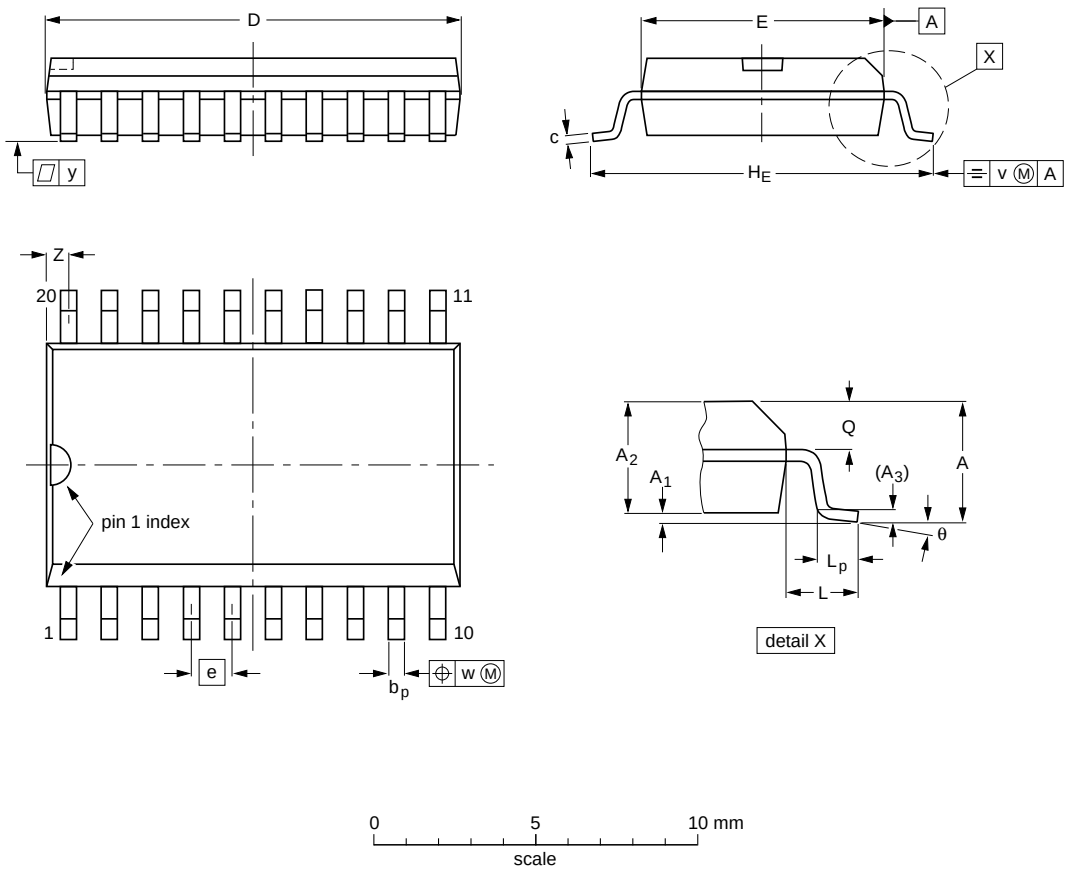
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT146-1 | | MS-001 | SC-603 | | | ~~99-12-27~~<br>03-02-13 |

**Fig 10. Package outline SOT146-1 (DIP20)**

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

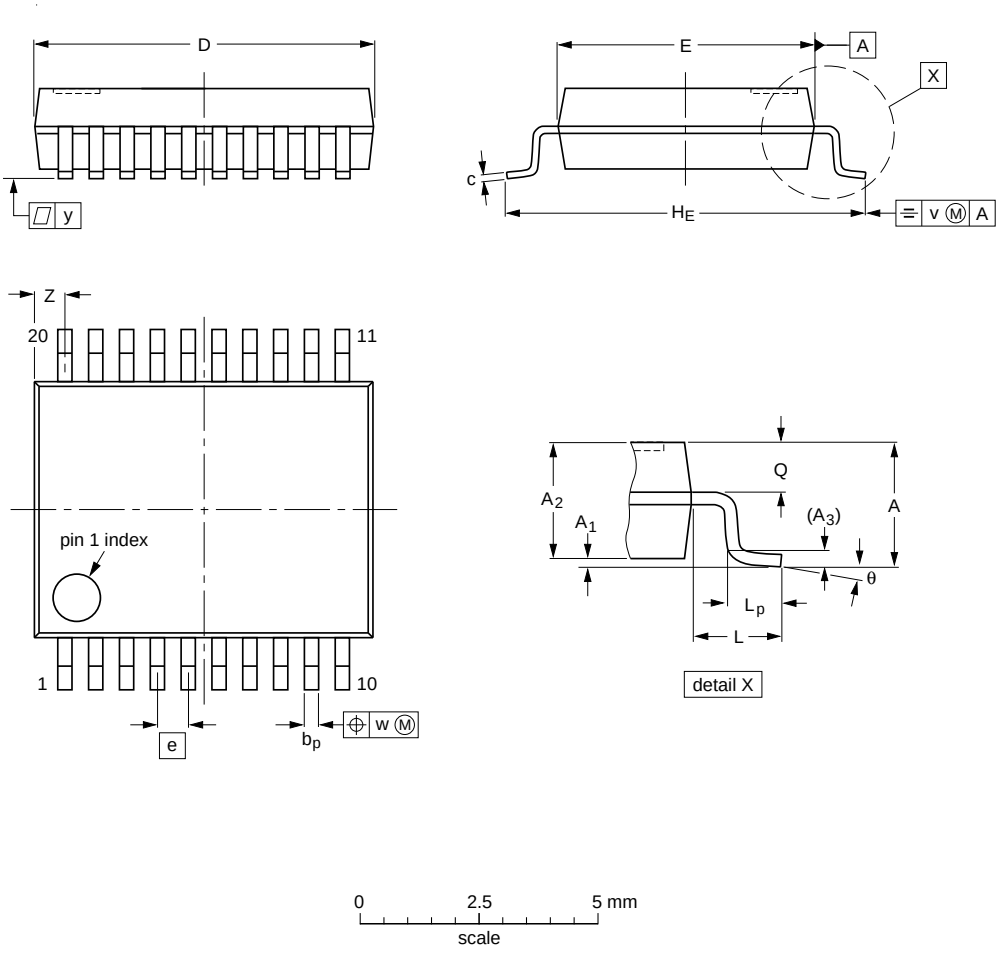
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 11. Package outline SOT163-1 (SO20)**

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm** **SOT339-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 7.4<br>7.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT339-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT339-1 (SSOP20)**

## 15. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |

## 16. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT7540 v.4 | 20121231 | Product data sheet | - | 74HC_HCT7540 v.3 |
| Modifications: | • $I_{OZ}$ added to static characteristics table. | | | |
| 74HC_HCT7540 v.3 | 20120827 | Product data sheet | - | 74HC_HCT7540_CNV v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT7540_CNV v.2 | 19970917 | Product specification | - | - |

# 17. Legal information

## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 19. Contents





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