74AUP2G57

Low-power dual PCB configurable multiple function gate

Rev. 1 — 4 November 2014 Product data sheet

1. General description

The 74AUP2G57 is a dual configurable multiple function gate with Schmitt-trigger inputs. Each gate within the device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10% of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G57DP	−40 °C to +85 °C	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
74AUP2G57GM	−40 °C to +125 °C	XQFN10	plastic extremely thin quad flat package; no leads; 10 terminals; body 2 × 1.55 × 0.5 mm	SOT1049-3
74AUP2G57GU	−40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 × 1.80 × 0.50 mm	SOT1160-1
74AUP2G57GF	−40 °C to +125 °C	XSON10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.0 × 1.7 × 0.5 mm	SOT1081-2

4. Marking

Table 2. Marking

Type number	Marking code[1]
74AUP2G57DP	aC
74AUP2G57GM	aC
74AUP2G57GU	aC
74AUP2G57GF	aC

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

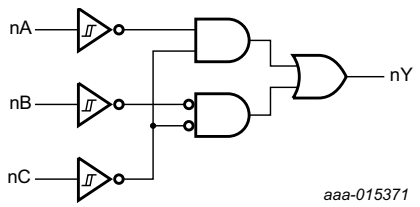


Fig 1. Logic symbol (one gate)

6. Pinning information

6.1 Pinning

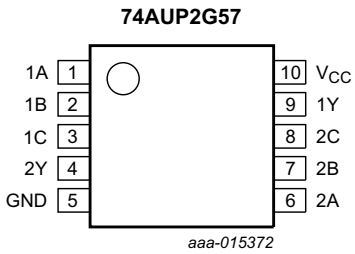


Fig 2. Pin configuration SOT552-1 (TSSOP10)

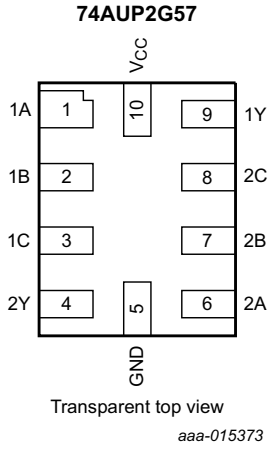


Fig 3. Pin configuration SOT1049-3 (XQFN10)

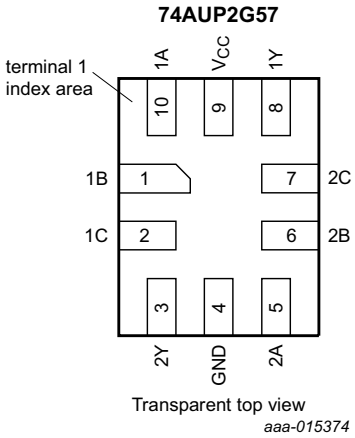


Fig 4. Pin configuration SOT1160-1 (XQFN10)

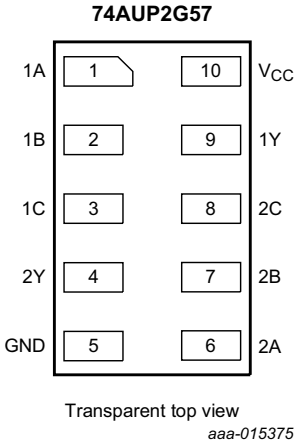


Fig 5. Pin configuration SOT1081-2 (XSON10)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT552-1, SOT1049-3 and SOT1081-2	SOT1160-1	
1A, 2A	1, 6	10, 5	data input
1B, 2B	2, 7	1, 6	data input
1C, 2C	3, 8	2, 7	data input
1Y, 2Y	9, 4	8, 3	data output
GND	5	4	ground (0 V)
V_{CC}	10	9	supply voltage

7. Functional description

Table 4. Function table[1]

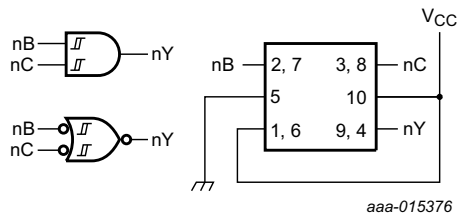
Input			Output
nC	nB	nA	nY
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7.1 Logic configurations

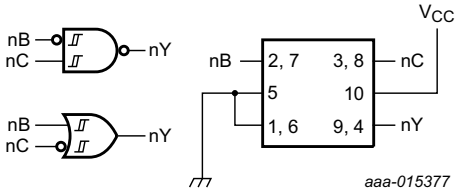
Table 5. Function selection table

Logic function	Figure
2-input AND	see Figure 6
2-input AND with both inputs inverted	see Figure 9
2-input NAND with inverted input	see Figure 7 and Figure 8
2-input OR with inverted input	see Figure 7 and Figure 8
2-input NOR	see Figure 9
2-input NOR with both inputs inverted	see Figure 6
2-input XNOR	see Figure 10
Inverter	see Figure 11
Buffer	see Figure 12



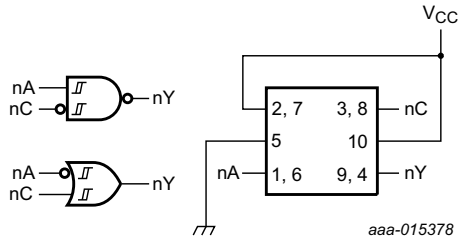
Pin numbers are not valid for SOT1160-1 package

Fig 6. 2-input AND gate or 2-input NOR gate with both inputs inverted



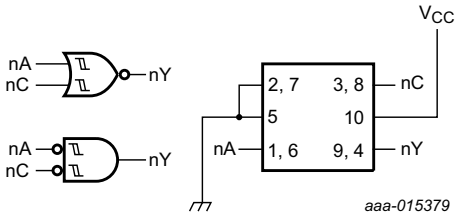
Pin numbers are not valid for SOT1160-1 package

Fig 7. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input



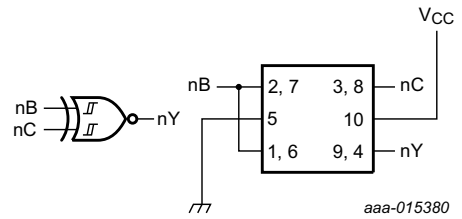
Pin numbers are not valid for SOT1160-1 package

Fig 8. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input



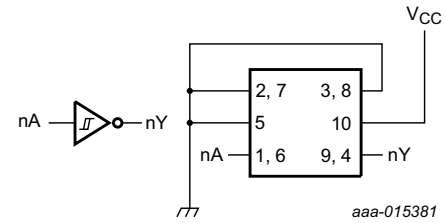
Pin numbers are not valid for SOT1160-1 package

Fig 9. 2-input NOR gate or 2-input AND gate with both inputs inverted



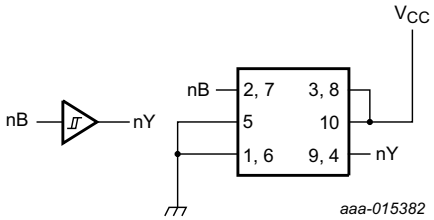
Pin numbers are not valid for SOT1160-1 package

Fig 10. 2-input XNOR gate



Pin numbers are not valid for SOT1160-1 package

Fig 11. Inverter



Pin numbers are not valid for SOT1160-1 package

Fig 12. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	−50	-	mA
V_I	input voltage	[1]	−0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	−50	-	mA
V_O	output voltage	Active mode and Power-down mode [1]	−0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP10 package: above 55°C the value of P_{tot} derates linearly with 2.5 mW/K.
For XQFN10 (SOT1049-3) package: above 132 °C the value of P_{tot} derates linearly with 14.1 mW/K.
For XQFN10 (SOT1160-1) package: above 128 °C the value of P_{tot} derates linearly with 11.5 mW/K.
For XSON10 package: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		−40	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	-	-	40	μA
C_I	input capacitance	V_I = GND or V_{CC}; V_{CC} = 0 V to 3.6 V	-	1.1	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.7	-	pF

Table 8. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.7 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	-	-	50	μA

Table 8. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.11	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.6 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	0.93	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.17	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.77	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.67	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.40	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.33 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	-	-	75	μA

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 5 pF									
t_{pd}	propagation delay	nA, nB and nC to nY; see Figure 13 [2]							
		V_{CC} = 0.8 V	-	22.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.8	6.5	12.6	2.5	13.0	13.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	4.6	7.6	2.5	8.2	8.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	3.9	6.2	2.0	6.8	7.2	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	3.1	4.5	1.8	5.1	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	2.8	3.9	1.5	4.1	4.3	ns
C_L = 10 pF									
t_{pd}	propagation delay	nA, nB and nC to nY; see Figure 13 [2]							
		V_{CC} = 0.8 V	-	26.1	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.2	7.3	14.4	2.8	14.9	15.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.6	5.2	8.7	2.8	9.3	9.8	ns
		V_{CC} = 1.65 V to 1.95 V	2.5	4.5	7.0	2.2	7.8	8.2	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	3.7	5.2	2.1	5.9	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	2.3	3.4	4.6	1.9	4.9	5.1	ns
C_L = 15 pF									
t_{pd}	propagation delay	nA, nB and nC to nY; see Figure 13 [2]							
		V_{CC} = 0.8 V	-	31.6	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.4	8.0	15.7	3.1	16.7	17.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.8	5.7	9.4	3.1	10.4	10.9	ns
		V_{CC} = 1.65 V to 1.95 V	2.6	4.9	7.7	2.5	8.7	9.2	ns
		V_{CC} = 2.3 V to 2.7 V	2.6	4.1	5.7	2.4	6.5	6.9	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	3.8	5.0	2.2	5.5	5.7	ns
C_L = 30 pF									
t_{pd}	propagation delay	nA, nB and nC to nY; see Figure 13 [2]							
		V_{CC} = 0.8 V	-	37.8	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.6	10.4	20.9	3.9	21.8	22.3	ns
		V_{CC} = 1.4 V to 1.6 V	3.6	7.4	12.2	3.8	13.4	14.1	ns
		V_{CC} = 1.65 V to 1.95 V	3.5	6.2	9.9	3.1	11.1	11.8	ns
		V_{CC} = 2.3 V to 2.7 V	3.4	5.2	7.4	3.1	8.3	8.8	ns
		V_{CC} = 3.0 V to 3.6 V	3.2	4.9	6.6	2.8	7.0	7.4	ns

Table 9. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 5 pF, 10 pF, 15 pF and 30 pF									
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3] [4]							
		V_{CC} = 0.8 V	-	2.6	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	2.8	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	2.9	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	3.1	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.7	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	4.3	-	-	-	-	pF

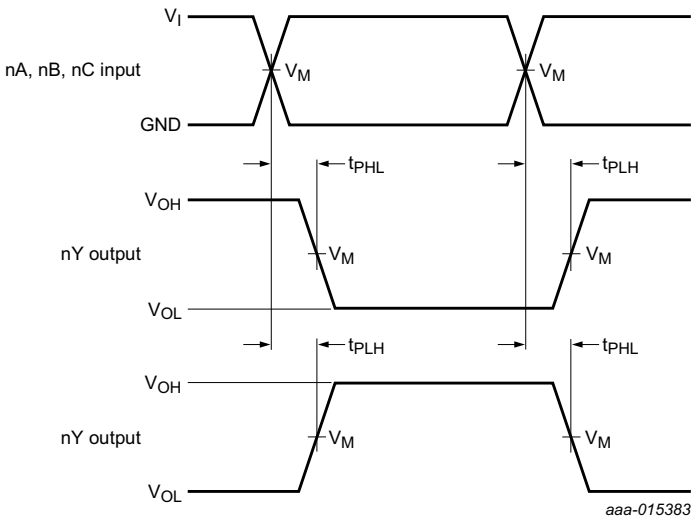
[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] All specified values are the average typical values over all stated loads.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms



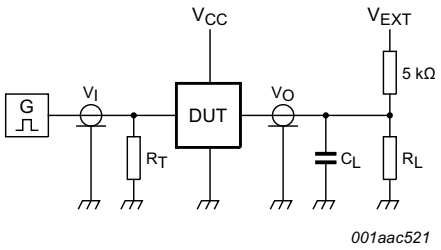
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 13. Input nA, nB and nC to output nY propagation delay times

Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 14. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L[1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times, R_L = 5 kΩ. For measuring propagation delays, set-up and hold times, and pulse width, R_L = 1 MΩ.

13. Transfer characteristics

Table 12. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{T+}	positive-going threshold voltage	see Figure 15 and Figure 16							
		V_{CC} = 0.8 V	0.30	-	0.60	0.30	0.60	0.62	V
		V_{CC} = 1.1 V	0.53	-	0.90	0.53	0.90	0.92	V
		V_{CC} = 1.4 V	0.74	-	1.11	0.74	1.11	1.13	V
		V_{CC} = 1.65 V	0.91	-	1.29	0.91	1.29	1.31	V
		V_{CC} = 2.3 V	1.37	-	1.77	1.37	1.77	1.80	V
		V_{CC} = 3.0 V	1.88	-	2.29	1.88	2.29	2.32	V
V_{T-}	negative-going threshold voltage	see Figure 15 and Figure 16							
		V_{CC} = 0.8 V	0.10	-	0.60	0.10	0.60	0.60	V
		V_{CC} = 1.1 V	0.26	-	0.65	0.26	0.65	0.65	V
		V_{CC} = 1.4 V	0.39	-	0.75	0.39	0.75	0.75	V
		V_{CC} = 1.65 V	0.47	-	0.84	0.47	0.84	0.84	V
		V_{CC} = 2.3 V	0.69	-	1.04	0.69	1.04	1.04	V
		V_{CC} = 3.0 V	0.88	-	1.24	0.88	1.24	1.24	V
V_H	hysteresis voltage	($V_{T+} - V_{T-}$); see Figure 15, Figure 16, Figure 17 and Figure 18							
		V_{CC} = 0.8 V	0.07	-	0.50	0.07	0.50	0.50	V
		V_{CC} = 1.1 V	0.08	-	0.46	0.08	0.46	0.46	V
		V_{CC} = 1.4 V	0.18	-	0.56	0.18	0.56	0.56	V
		V_{CC} = 1.65 V	0.27	-	0.66	0.27	0.66	0.66	V
		V_{CC} = 2.3 V	0.53	-	0.92	0.53	0.92	0.92	V
		V_{CC} = 3.0 V	0.79	-	1.31	0.79	1.31	1.31	V

14. Waveform transfer characteristics

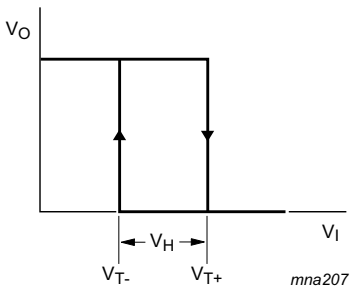
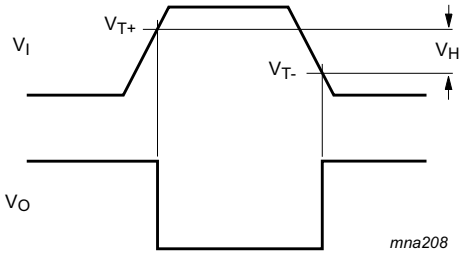


Fig 15. Transfer characteristic



V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig 16. Definition of V_{T+}, V_{T-}, and V_H

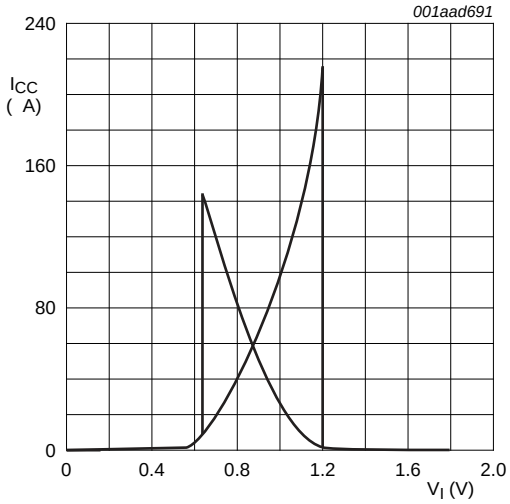


Fig 17. Typical transfer characteristics; V_{CC} = 1.8 V

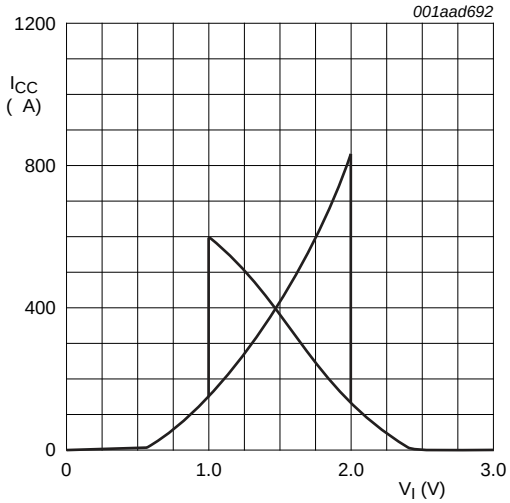
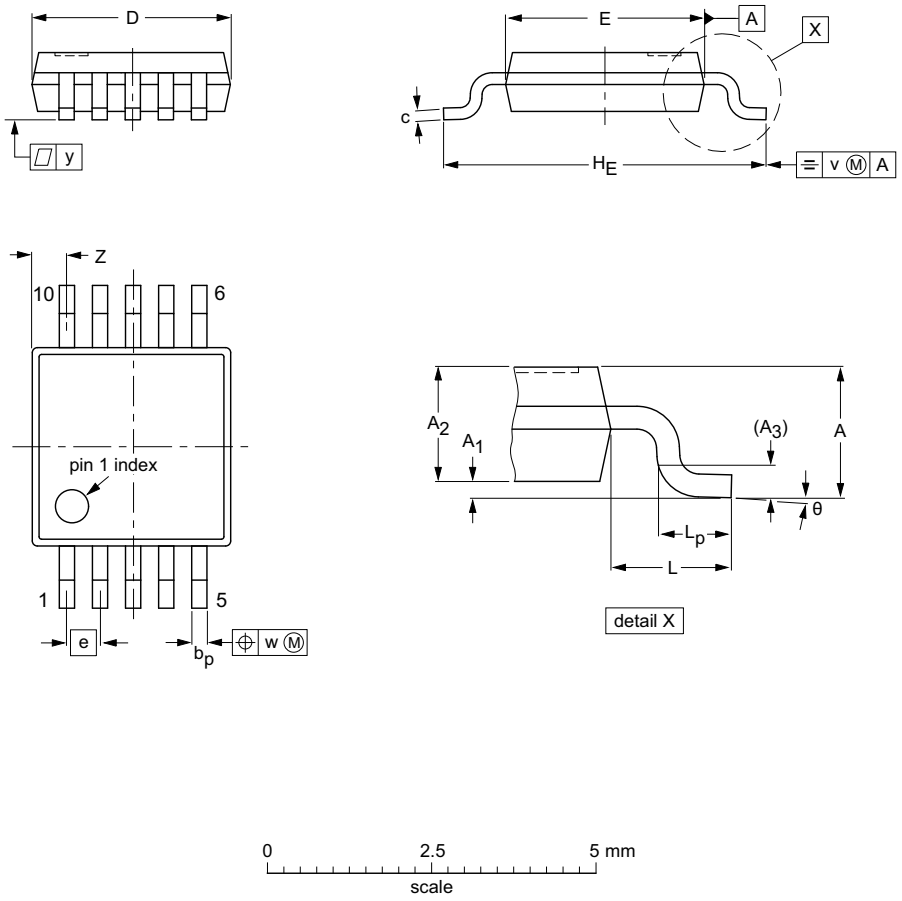


Fig 18. Typical transfer characteristics; V_{CC} = 3.0 V

15. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

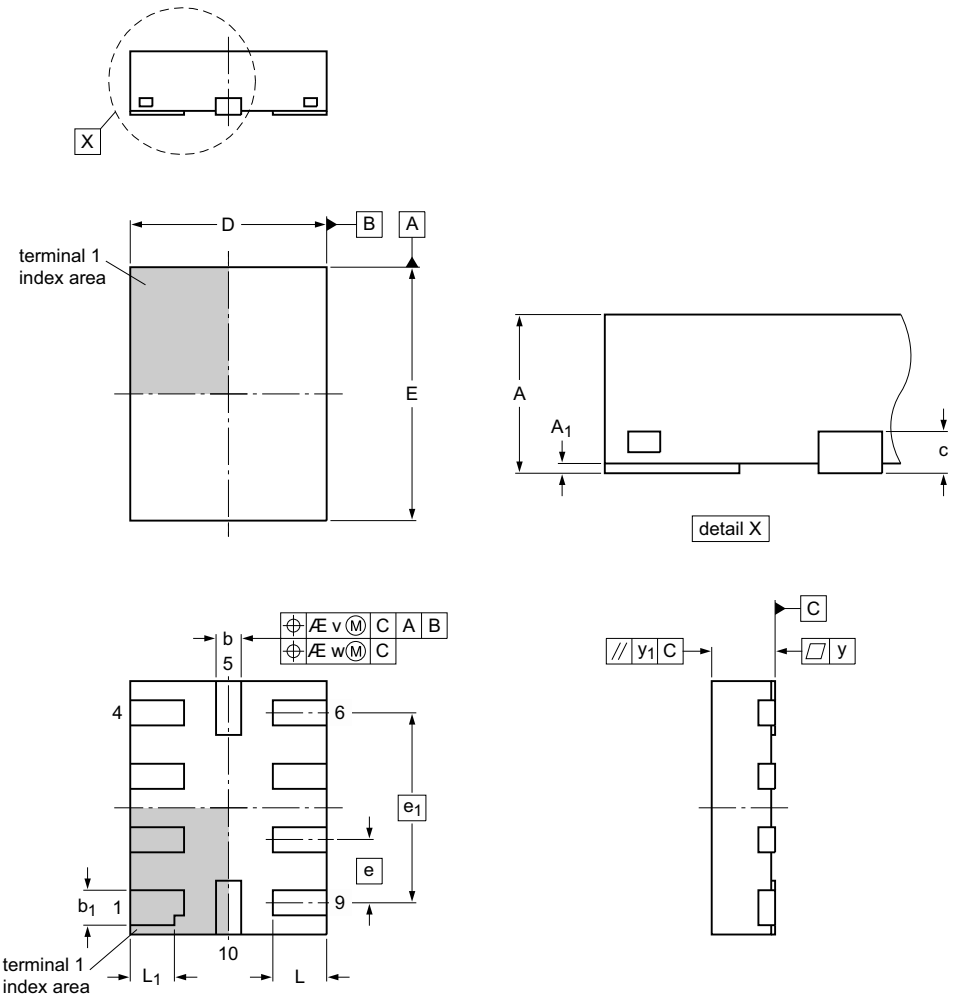
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						~~99-07-29~~ 03-02-18

Fig 19. Package outline SOT552-1 (TSSOP10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm **SOT1049-3**



Dimensions

Unit[1]		A	A_1	b	b_1	c	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.33		1.65	2.1			0.48	0.40				
	nom			0.20	0.28	0.127	1.55	2.0	0.5	1.5	0.43	0.35	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.23		1.45	1.9			0.38	0.30				

Note

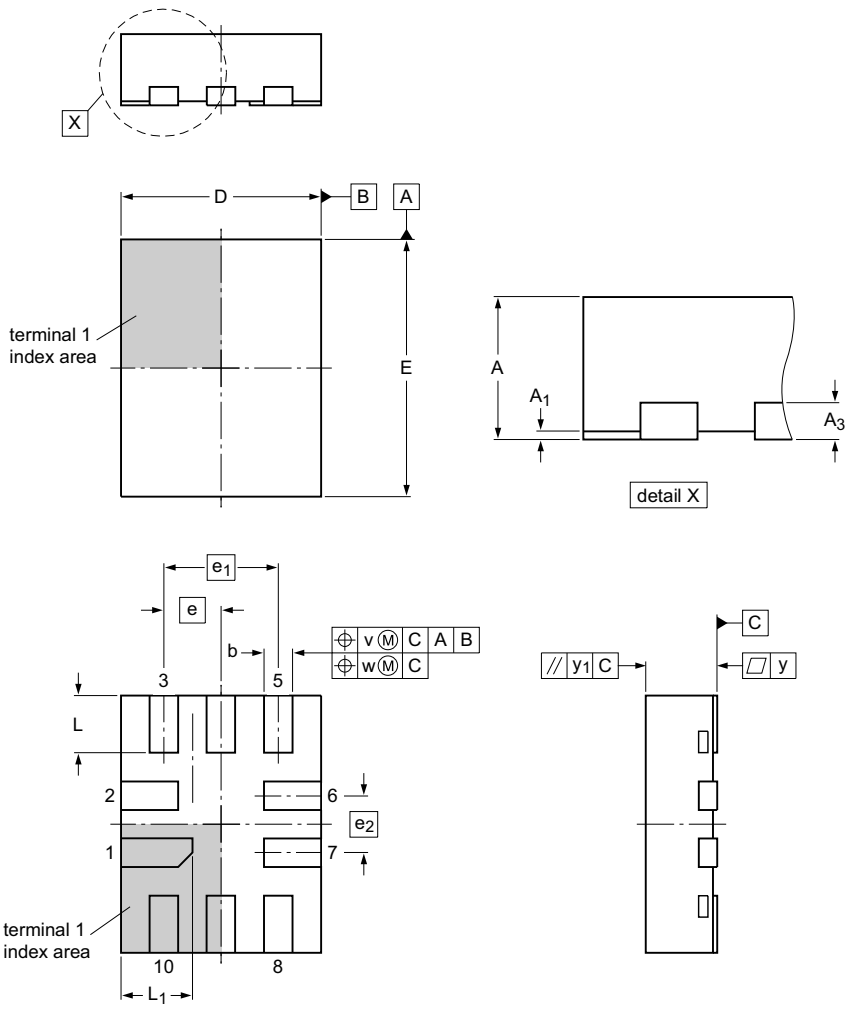
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1049-3	- - -	MO255	- - -			~~10-12-06~~ 11-03-30

Fig 20. Package outline SOT1049-3 (XQFN10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.5	0.05		0.25	1.5	1.9				0.45	0.55				
	nom			0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.3	1.7				0.35	0.45				

Note

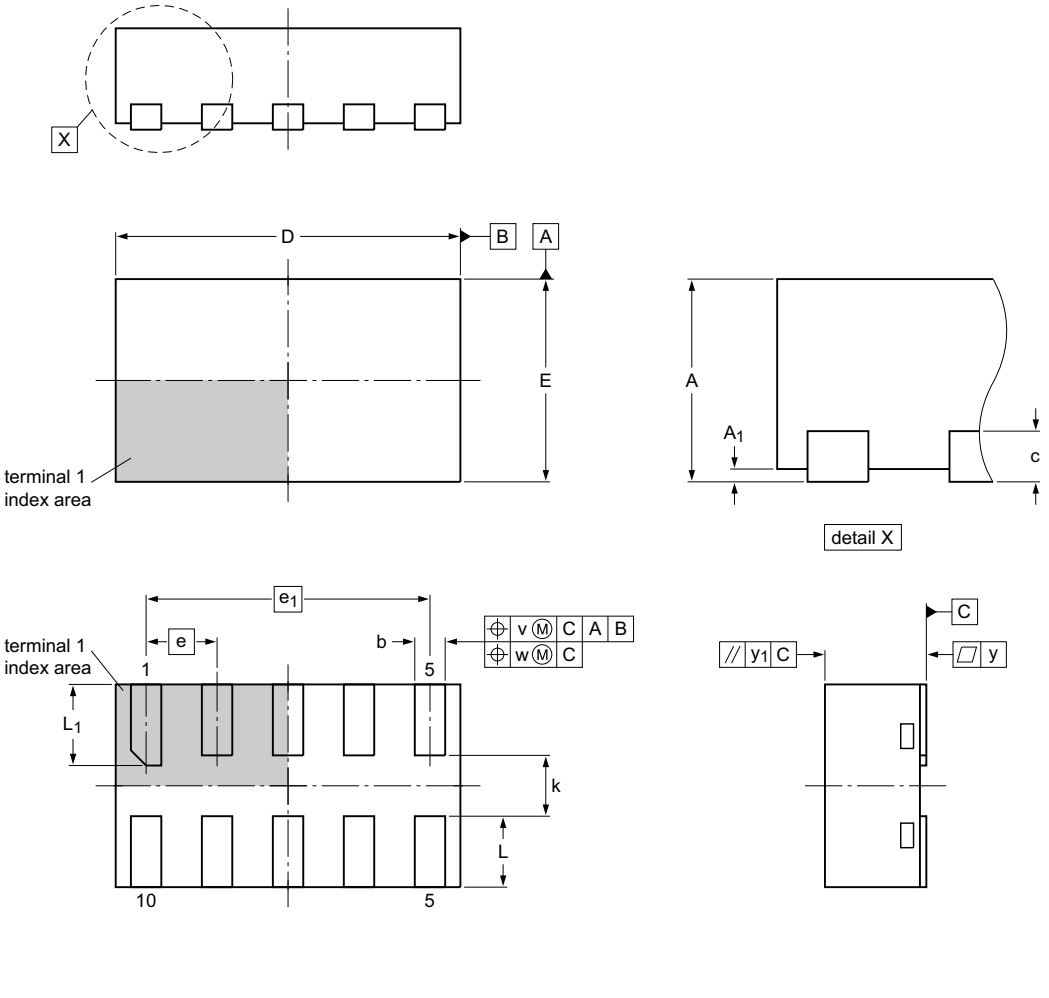
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	---	---	---		~~09-12-28~~ 09-12-29

Fig 21. Package outline SOT1160-1 (XQFN10)

XSON10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.0 x 1.7 x 0.5 mm **SOT1081-2**



Dimensions

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.20		1.8	1.1				0.40	0.45				
	nom			0.15	0.127	1.7	1.0	0.35	1.4		0.35	0.40	0.1	0.05	0.05	0.05
	min		0.00	0.10		1.6	0.9			0.2	0.30	0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1081-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1081-2	- - -	- - -	- - -			~~10-11-08~~ 11-03-30

Fig 22. Package outline SOT1081-2 (XSON10)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PCB	Printed Circuit Board

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G57 v.1	20141104	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 November 2014
Document identifier: 74AUP2G57