Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

DATA SHEET

74ABT16841A
20-bit bus interface latch (3-State)

Product data

2004 Feb 02

Replaces data sheet 74ABT16841A/74ABTH16841A of 2002 Dec 17

Philips
Semiconductors

PHILIPS

20-bit bus interface latch (3-State) 74ABT16841A

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA / –32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16841A Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841A consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is LOW. When $n\overline{OE}$ is HIGH the output is in the high-impedance state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50 pF; V_{CC} = 5 V	3.1 2.2	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0 V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5 V	500	μA
I_{CCL}		Outputs LOW; V_{CC} = 5.5 V	10	mA

ORDERING INFORMATION

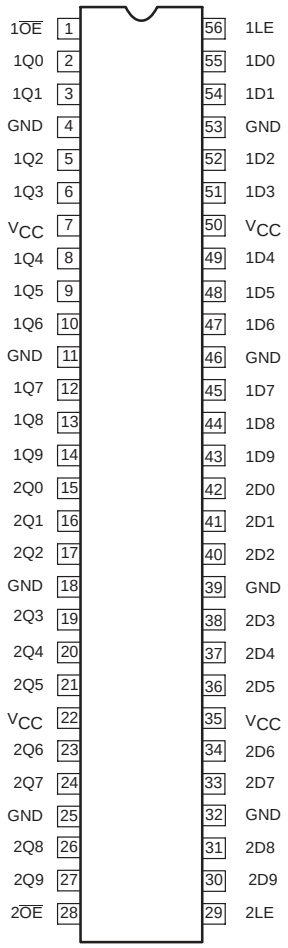
T_{amb} = –40 °C to +85 °C

Type number	Package		
	Name	Description	Version
74ABT16841ADL	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ABT16841ADGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

PIN DESCRIPTION

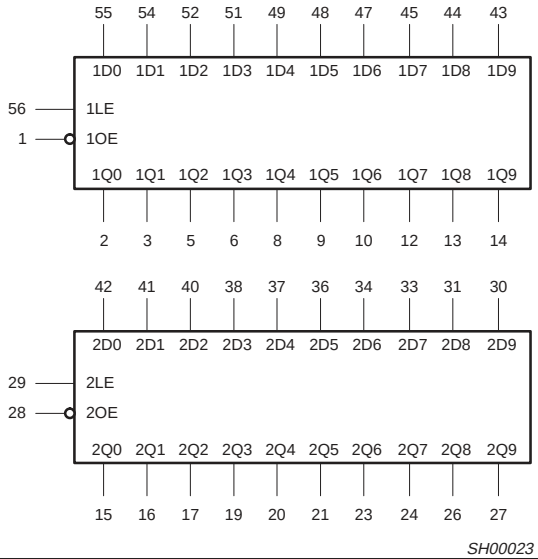
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-LOW)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



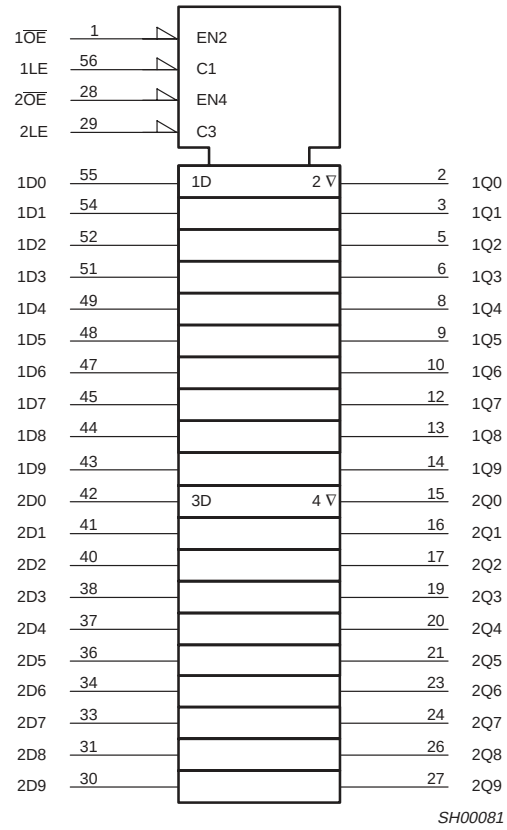
SA00076

LOGIC SYMBOL



SH00023

LOGIC SYMBOL (IEEE/IEC)



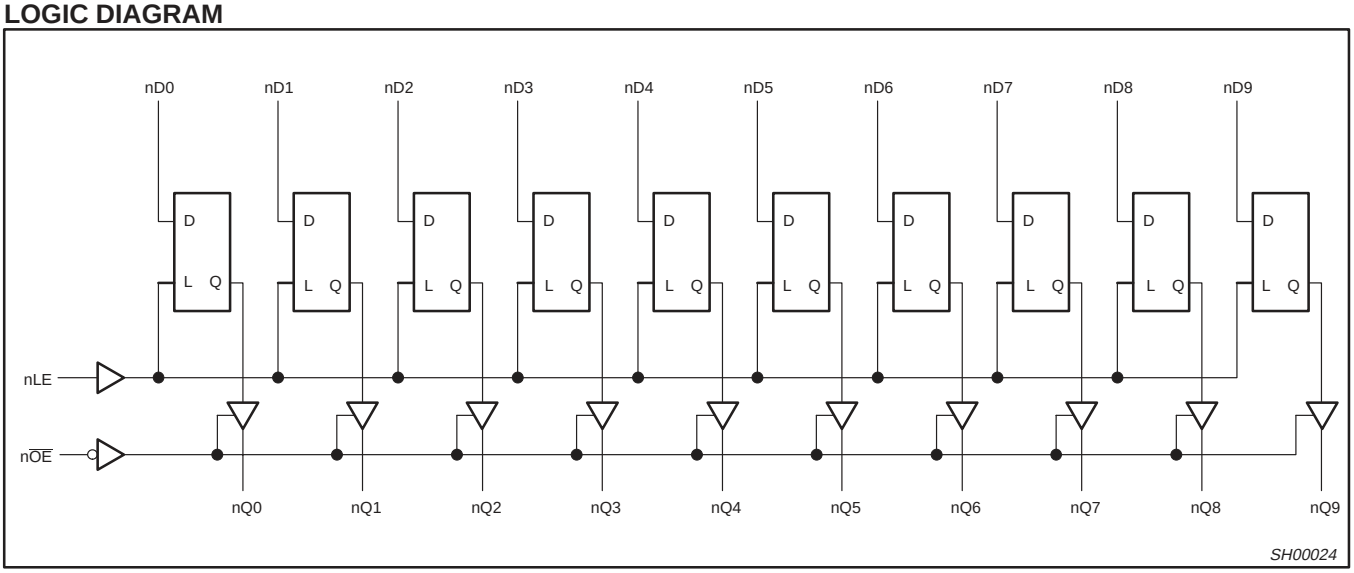
SH00081

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$n\overline{OE}$	nLE	nDx	nQ0 – nQ9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
↓ = HIGH-to-LOW LE transition
NC = No change
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9	–	2.5	–	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4	–	3.0	–	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4	–	2.0	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	–	0.42	0.55	–	0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	–	0.13	0.55	–	0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	–	±0.01	±1	–	±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or $V_I \leq$ 4.5 V	–	±5.0	±100	–	±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care	–	±5.0	±50	–	±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}	–	5.0	10	–	10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}	–	–5.0	–10	–	–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	–	5.0	50	–	50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs High, V_I = GND or V_{CC}	–	0.5	1	–	1	mA
I_{CCL}		V_{CC} = 5.5 V; Outputs Low, V_I = GND or V_{CC}	–	10	19	–	19	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}	–	0.5	1	–	1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	–	0.2	1	–	1	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.
5. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.1 1.5	3.1 2.2	4.1 3.1	1.1 1.5	4.9 3.6	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.0	2.5 2.1	3.3 2.8	1.5 1.0	3.7 3.1	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	4 5	1.2 1.2	2.4 2.2	3.2 2.9	1.2 1.2	4.0 3.6	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	4 5	1.8 1.5	3.0 2.5	4.0 3.2	1.8 1.5	4.9 3.7	ns

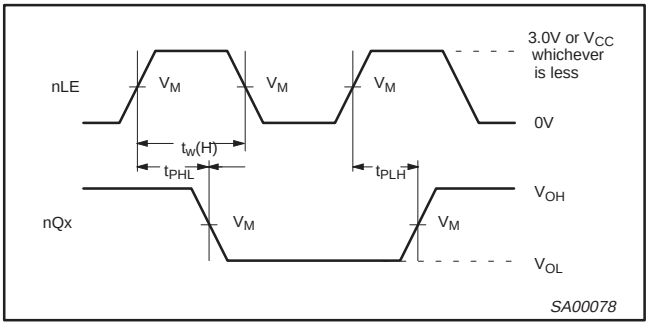
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

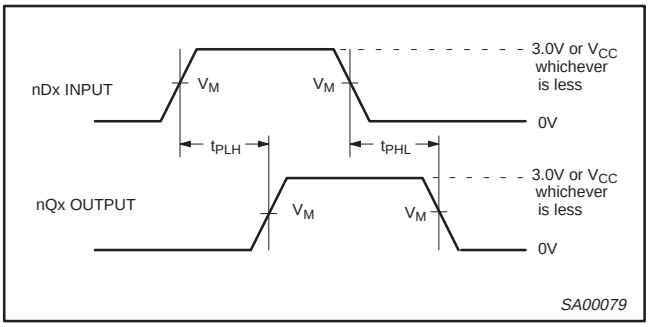
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = +25 °C, V_{CC} = +5.0 V		T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ±0.5 V		
			Min	Typ	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW nDx to nLE	3	2.0 1.0	1.0 0.4	2.0 1.0	– –	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW nDx to nLE	3	2.0 2.0	–0.3 –0.7	2.0 2.0	– –	ns
$t_w(H)$	nLE pulse width HIGH	1	2.9	1.9	2.9	–	ns

AC WAVEFORMS

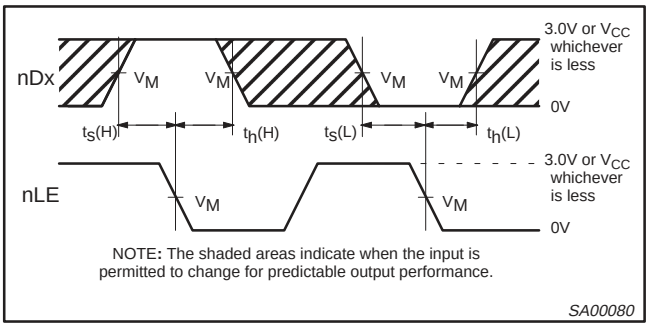
V_M = 1.5 V, V_{IN} = GND to 3.0 V



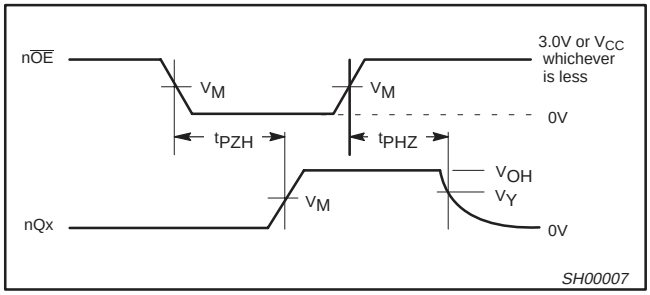
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



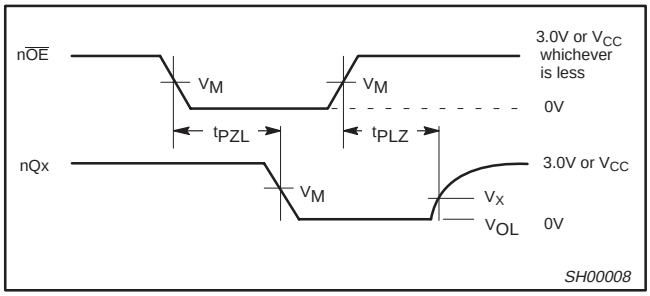
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Set-up and Hold Times

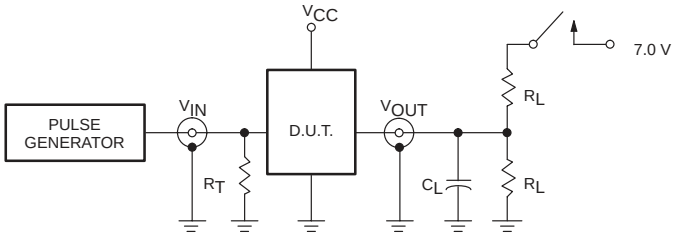


Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

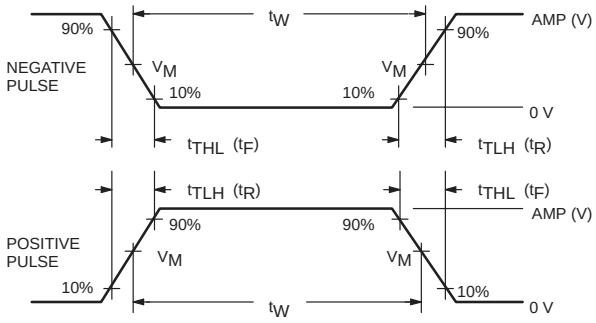


Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

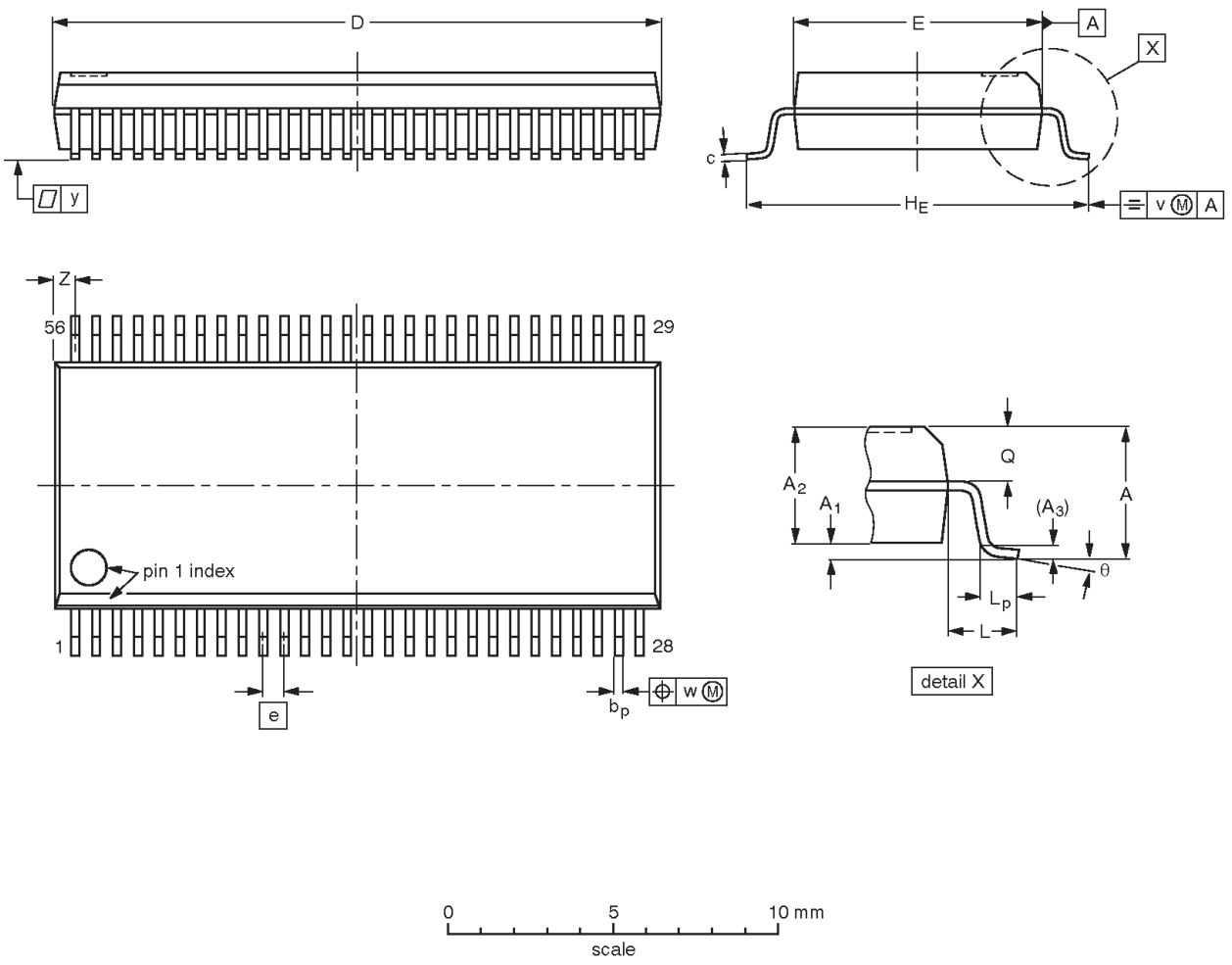
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

SA00654

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

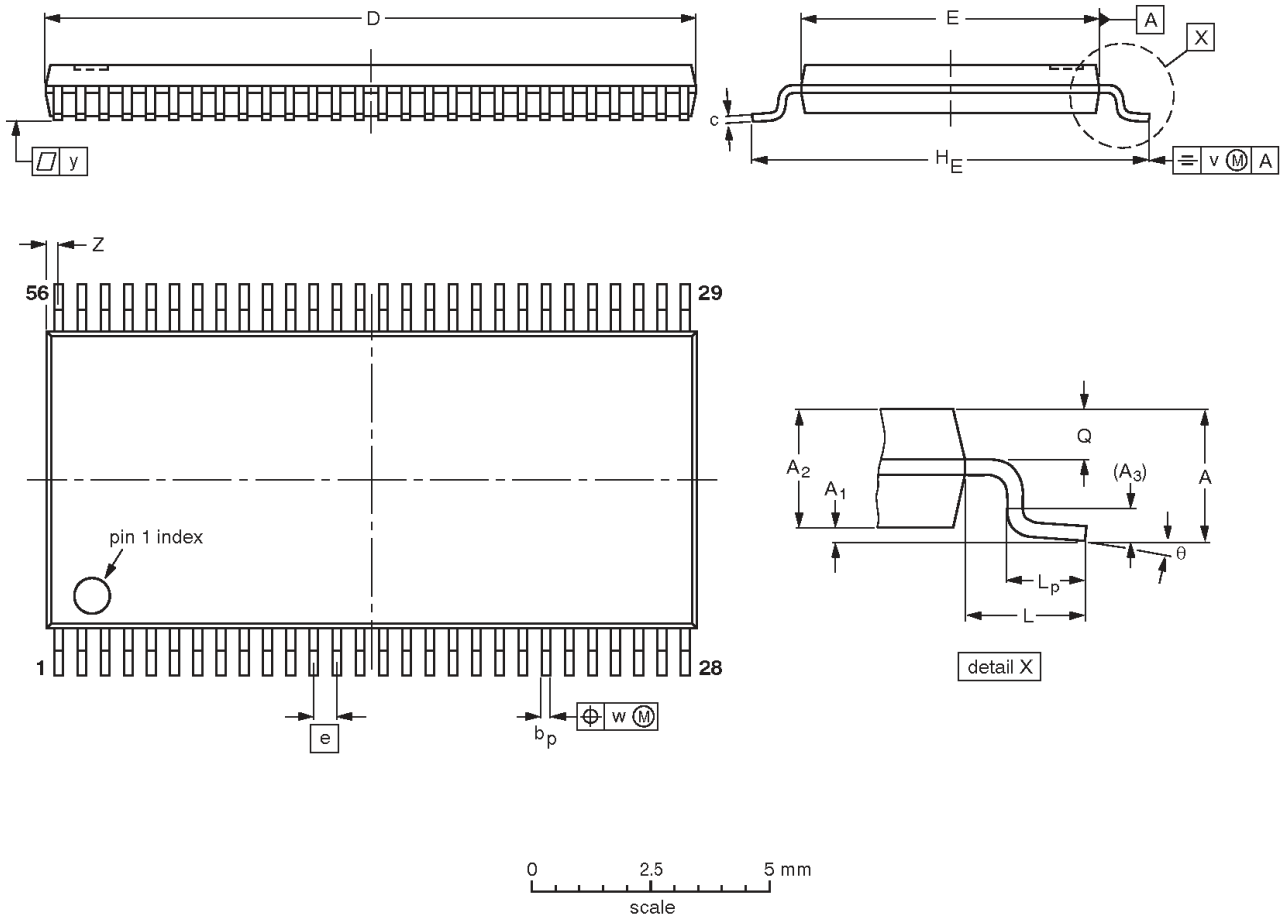
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040202	**Product data (9397 750 12821); 853-1797 ECN 01–A15433 of 27 January 2004. Replaces data sheet 74ABT_H16841A_2 of 2002 Dec 17 (9397 750 10845).** Modifications: ● Delete all references to 74ABTH16841A (product discontinued).
_2	20021217	**Product data (9397 750 10845); ECN 853-1797 29296 of 12 December 2002. Supersedes data of 27 February 1998 (9397 750 03506).**
_1	19980227	**Product specification (9397 750 03506). ECN 853-1797 19025 of 27 February 1998.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

Date of release: 02-04

Document order number: 9397 750 12821

Let's make things better.

Philips Semiconductors

PHILIPS