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Vishay Dale

RoHS

IHLP® Commercial Inductors, Low DCR Series





LINKS TO ADDITIONAL RESOURCES





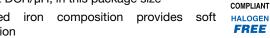
STANDARD ELECTRICAL SPECIFICATIONS				
L ₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (μH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) ⁽¹⁾	SATURATION CURRENT DC TYP. (A) (2)
1.0	7.6	8.0	12.5	9.5
2.2	15.7	16.5	9.0	7.0
3.3	24.8	26.0	7.0	6.5
4.7	31.8	33.4	6.0	4.0
6.8	44.6	46.8	5.5	4.0
8.2	52.3	54.9	5.0	4.0
10	67.8	71.2	4.0	3.5
15	88.4	95.0	3.7	3.2
22	128.9	135.0	2.9	2.5

Notes

- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +125 °C
- The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.
- Rated operating voltage (across inductor) = 50 V
- ⁽¹⁾ DC current (A) that will cause an approximate ΔT of 40 °C
- (2) DC current (A) that will cause L₀ to drop approximately 20 %

FEATURES

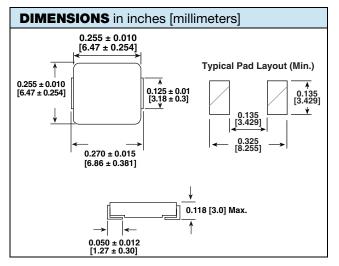
- Shielded construction
- Frequency range up to 1.0 MHz
- Lowest DCR/µH, in this package size
- Powered iron composition provides saturation

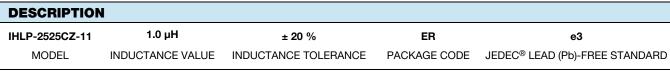


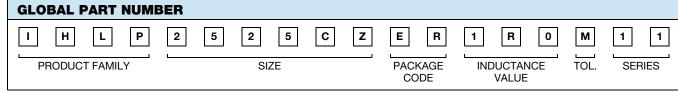
- · Handles high transient current spikes without hard saturation
- Ultra low buzz noise, due to composite construction
- IHLP design; PATENT(S): www.vishay.com/patents
- · Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- PDA / notebook / desktop / server applications
- High current POL converters
- · Low profile, high current power supplies
- · Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for field programmable gate array (FPGA)





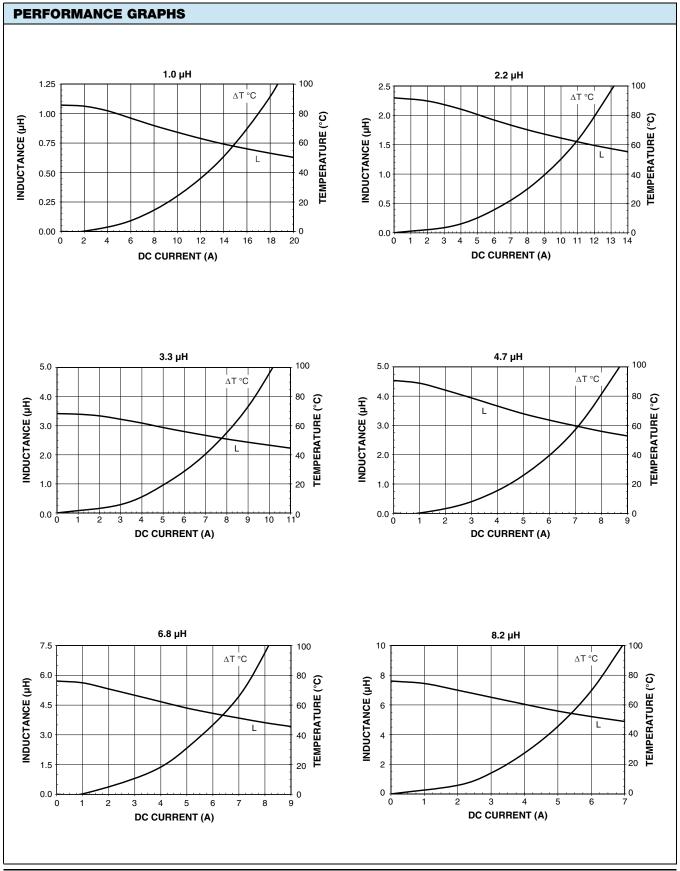


PATENT(S): www.vishay.com/patents

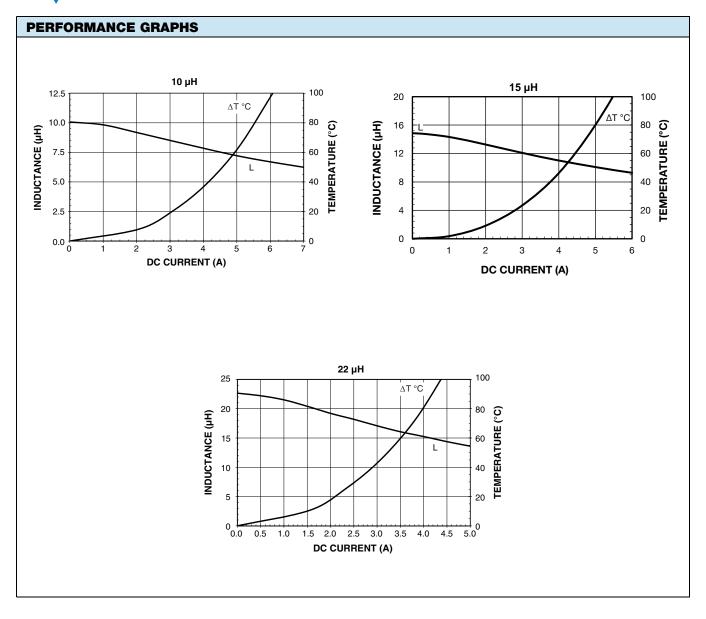
Revision: 13-Oct-2020

This Vishay product is protected by one or more United States and international patents.

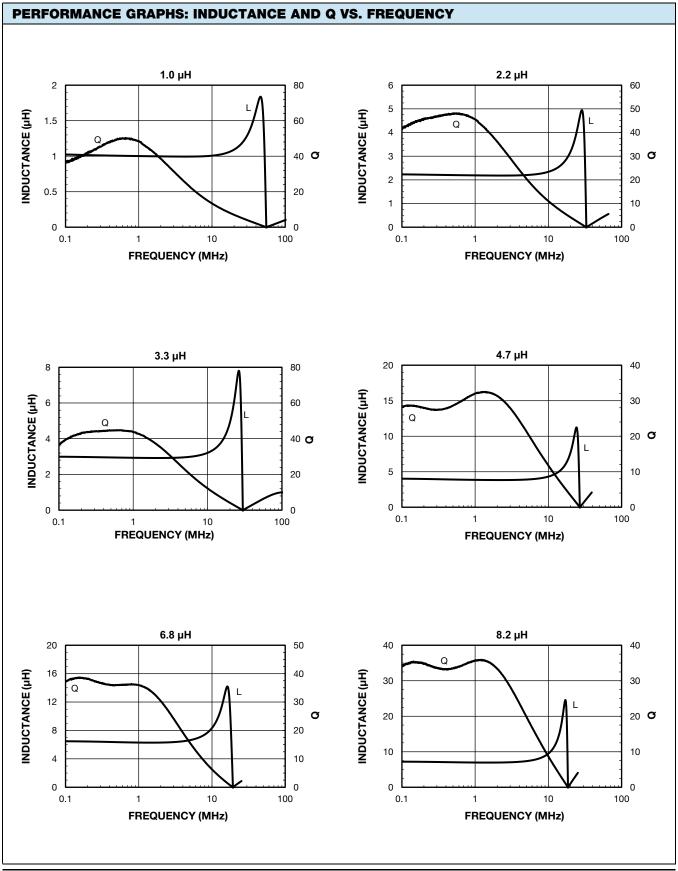




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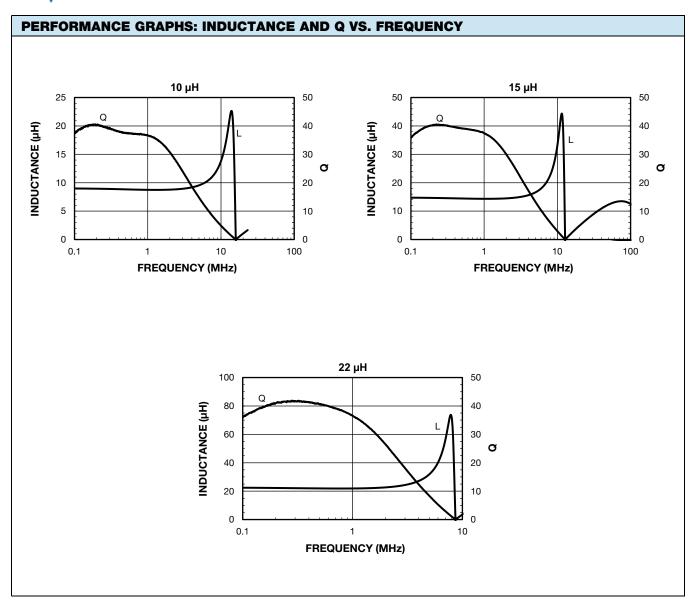








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