Title	***Reference Design Report for a 60 W USB PD 3.0 Power Supply with 5 V / 9 V/ 15 V / 20 V Outputs Using InnoSwitch™4-CZ PowiGaN™ INN4073C, ClampZero™ CPZ1062M and MinE-CAP™ MIN1072M***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A Outputs
Application	USB PD Power Adapter
Author	Applications Engineering Department
Document Number	RDR-928
Date	October 11, 2021
Revision	1.3

Summary and Features

- InnoSwitch4-CZ - active clamp flyback switcher IC with integrated high-voltage PowiGaN, synchronous rectification and FluxLink™ feedback
- Zero voltage switching in both CCM and DCM operating conditions
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <60 mW no-load input power, >20 mW consumed by micro controller
- Compact design with high power density: 30.3 W/ inch^3 without enclosure (60 W / 1.77 in X 1.77 in X 0.63 in)

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Table of Contents

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 60 W USB PD power supply with 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 3 A, output using InnoSwitch4-CZ INN4073C, ClampZero CPZ1062M, and MinE-CAP MIN1072M. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch4-CZ active clamp controller providing exceptional performance and is paired with the input capacitor volume-reduction capabilities of the MinE-CAP IC.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics and adapter case specifications, and performance data.

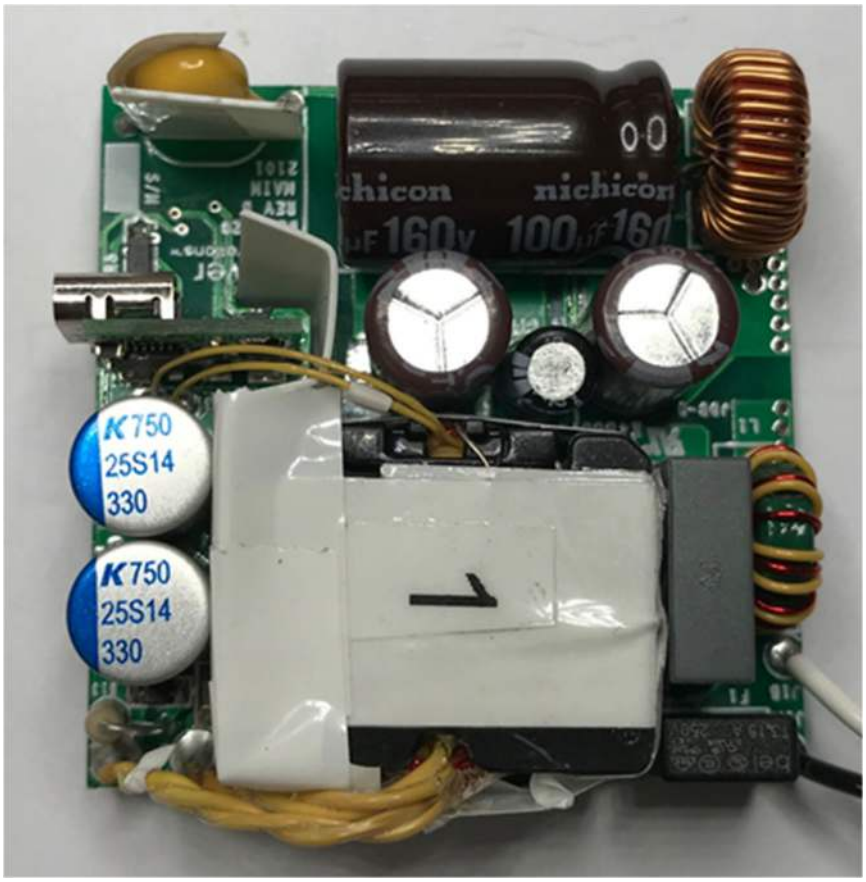


Figure 1 – Populated Circuit Board Photograph - Top.

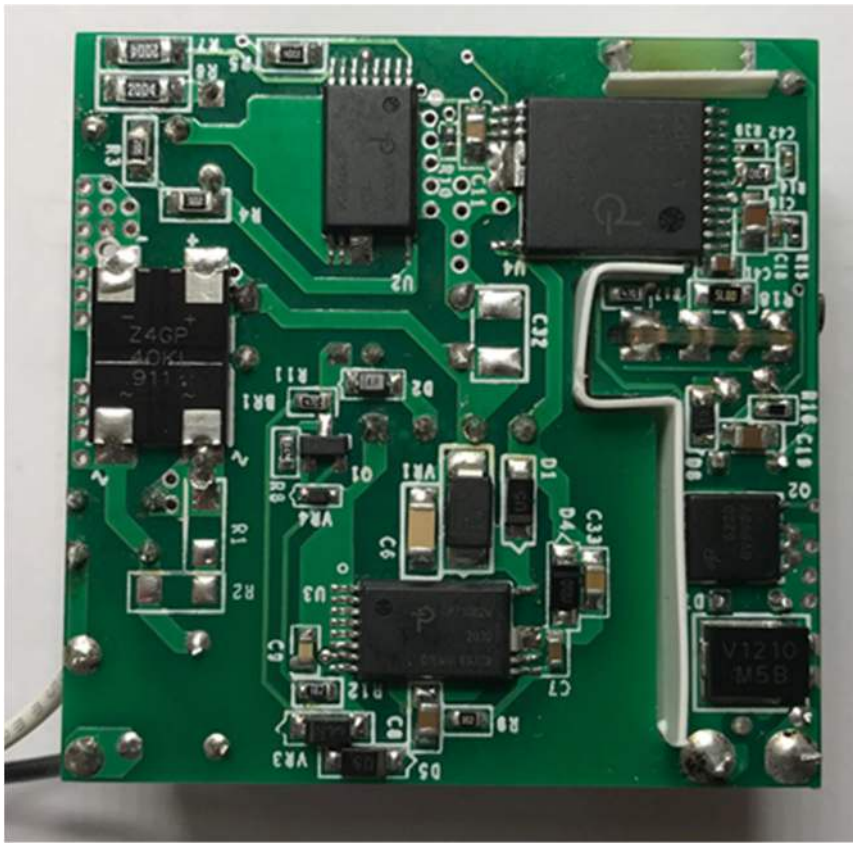


Figure 2 – Populated Circuit Board Photograph - Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				15.4	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			150	mV	Measured on board. (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		>90		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			150	mV	Measured on board. (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		>92		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			150	mV	Measured on board. (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(15\ V)}$		>93		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±2%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			200	mV	Measured on board. (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			3	A	±3%
Average Efficiency	$\eta_{(20\ V)}$		>93		%	Measured at 230 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			60	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. EMI, ESD and Line surge performance should be evaluated and adjust the layout to meet the target specification.

3 Schematic

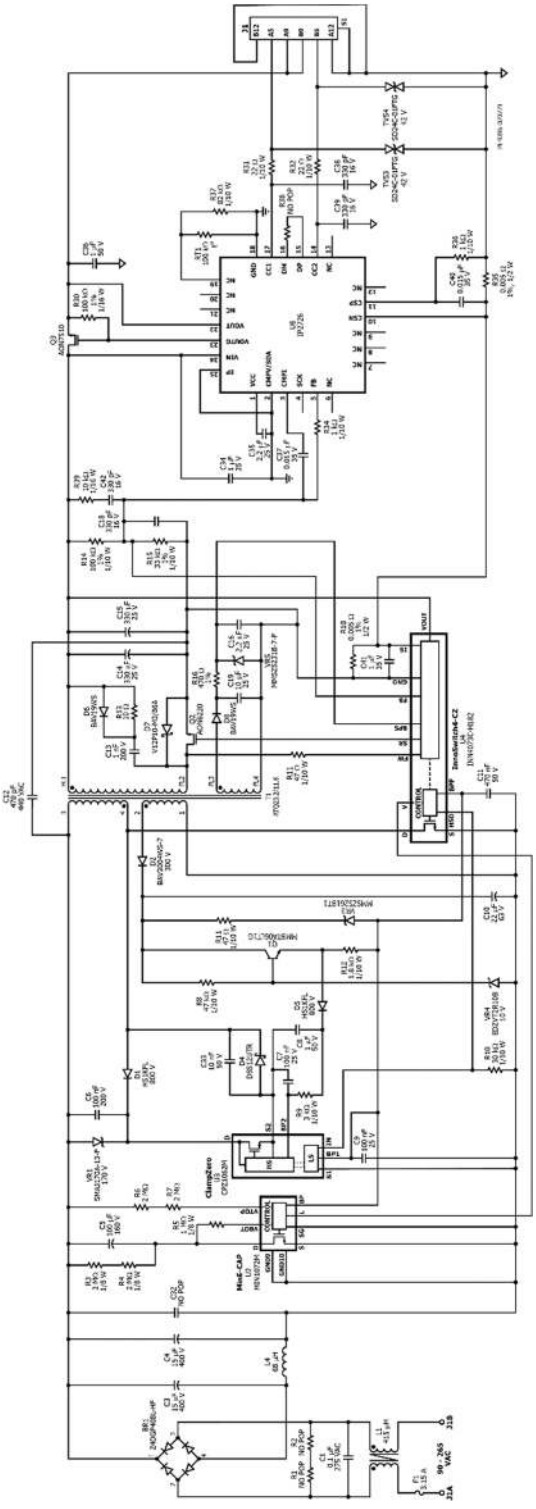


Figure 3 – Schematic.

Note:
Component references R1, R2, R38 and C32 although present in the layout, should not be populated.

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

Input fuse F1 isolates the circuit and provides protection from component failure, and the inductor L1 with capacitor C1 attenuates the EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitor C3. Inductor L4 forms a pi filter with capacitors C3 and C4 and attenuates the EMI. Y capacitor C12 connected between the power supply output and input helps to reduce common mode EMI.

4.2 *InnoSwitch4-CZ IC Primary*

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4-CZ IC (U4).

The V pin of the InnoSwitch4-CZ IC is connected directly to the L pin of the MinE-CAP IC. Resistors R6 and R7 provide input voltage sensing for both the MinE-CAP IC and InnoSwitch4-CZ ICs. The MinE-CAP uses resistors R6 and R7 to monitor the line voltage as well as the voltage across the high-voltage bulk capacitor, C4. Resistor R3 and R4 are bleeder resistors used to help regulate the voltage across C5, while resistor R5 is used by the MinE-CAP to sample the voltage at the negative terminal of C5. The MinE-CAP IC combines the information from the VTOP and VBOT pins to determine and control the voltage across the low-voltage bulk capacitor, C5. The InnoSwitch4-CZ IC uses the current from the L pin to determine line under voltage and over voltage conditions. During regular operation, the current from the L pin follows the value of the current flowing through R6 and R7. Thus, the InnoSwitch4-CZ IC operates as if said resistors are directly connected to the V pin. For this specific design, bypass capacitor C11 is shared by both the BPP pin of the InnoSwitch4-CZ IC and the BP pin of the MinE-CAP IC. The value of C11 is chosen based on the desired current limit of the InnoSwitch4-CZ. The BYPASS pin of Innoswitch4-CZ also supplies the ClampZero IC (U3) BP1 pin during start-up.

The primary clamp formed by diode D1 and capacitor C6 limits the peak drain voltage of U4 at the instant of turn-off of the switch inside U4. The energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C6. Part of the magnetizing energy will also get transferred to C6 depending on the capacitance value used. VR1 is used to protect the InnoSwitch4-CZ from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink signal is received from the secondary-side, the InnoSwitch4-CZ generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U3) turns on, to achieve soft switching of the InnoSwitch4-CZ primary switch, clamp capacitor C6 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. Diodes D1 and D4 are used to divert the transformer current from the

body diode of ClampZero IC high-side switch to minimize the reverse-recovery energy. A small delay is provided from the instant the high-side switch turns off in order to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R10. Capacitor C33 will help reduce the voltage on the ClampZero IC (U3) to provide soft turn-on.

Capacitor C9 is used to provide local decoupling at the BP1 pin of IC U3. Capacitor C7 provides the decoupling for BP2 pin. Diode D5 and capacitor C8 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R9 limits the current flowing into the BP2 pin.

The InnoSwitch4-CZ IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C11) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C10. Linear regulator circuit comprises of Q1, R8 and VR4 is used to provide a constant voltage source to supply BPP pin of U4 through resistor R12. Resistor R12 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch4-CZ IC (U4).

Output regulation is achieved using modulation control, where the frequency and I_{LIM} of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of I_{LIM} in the selected I_{LIM} range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR3 with current limiting resistor R11. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4-CZ IC U4. If the current flowing into the BPP pin increases above the ISD threshold, the U4 controller latches off to prevent any further increase in output voltage.

4.3 *InnoSwitch4-CZ IC Secondary*

The secondary-side of the InnoSwitch4-CZ IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q2/D7 and filtered by capacitors C14 and C15. Capacitor C36 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R13, C13, and D6. Diode D6 minimizes the dissipation in resistor R10.

The gate of Q2 is turned on by the secondary-side controller of IC U4, based on the winding voltage sensed via resistor R17 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV.

The secondary-side of the IC U4 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve the system efficiency and reduce the secondary-side internal consumption, a bias winding circuit was used. Bias winding voltage is rectified by diode D8 and filtered by capacitor C19. Resistor R16 limits the current flowing to the BPS pin of U4. Zener diode VR5 shunts the excess current supplied by bias winding output. Capacitor C16 connected to the BPS pin of IC U4 provides decoupling for the internal circuitry.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R14 and R15. The voltage across R15 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. The output voltage is regulated to achieve a voltage of 1.265 V on the FB pin. Capacitor C18 provides noise filtering of the signal at the FB pin.

Output current is sensed by monitoring the voltage drop across resistor R18 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. C41 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current. However, in this design current limit implemented by external PD controller. Resistor R18 is used for backup protection in case if there is a short-circuit at output.

4.4 *USB Type-C and PD Interface*

In this design, Injoinic IP2726 (U6) is the USB Type-C and PD controller. Output of the InnoSwitch4-CZ IC U4 powers the IP2726 device directly from Vbus.

IP2726 (U6) monitors and sets the feedback divider ratio such that InnoSwitch4-CZ IC U6 regulates the output voltage at required level. IP2726 (U6) changes the output voltage divider ratio to required level when there is a request through CC1 and CC2 lines. The default output voltage is maintained at 5 V.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which type-C plug is connected.

N-MOSFET Q3 makes the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. VBUS_OUT is discharged via U6. Resistor R35 is used to sense the output current for the microcontroller. Resistor R36 and C40 is used to filter any noise from output current sense.

Capacitor C34 is used as decoupling capacitor on VIN pin of U6 and capacitor C35 is used as decoupling capacitor on VCC pin of U6.

Resistor R31, R32, C38, C39, TVS3 and TVS4 are used to protect the CC1 and CC2 lines from ESD surge events.

Thermistor RT1 is used to sense USB Type-C connector temperature.

5 PCB Layout

PCB copper thickness is 0.040 inches.

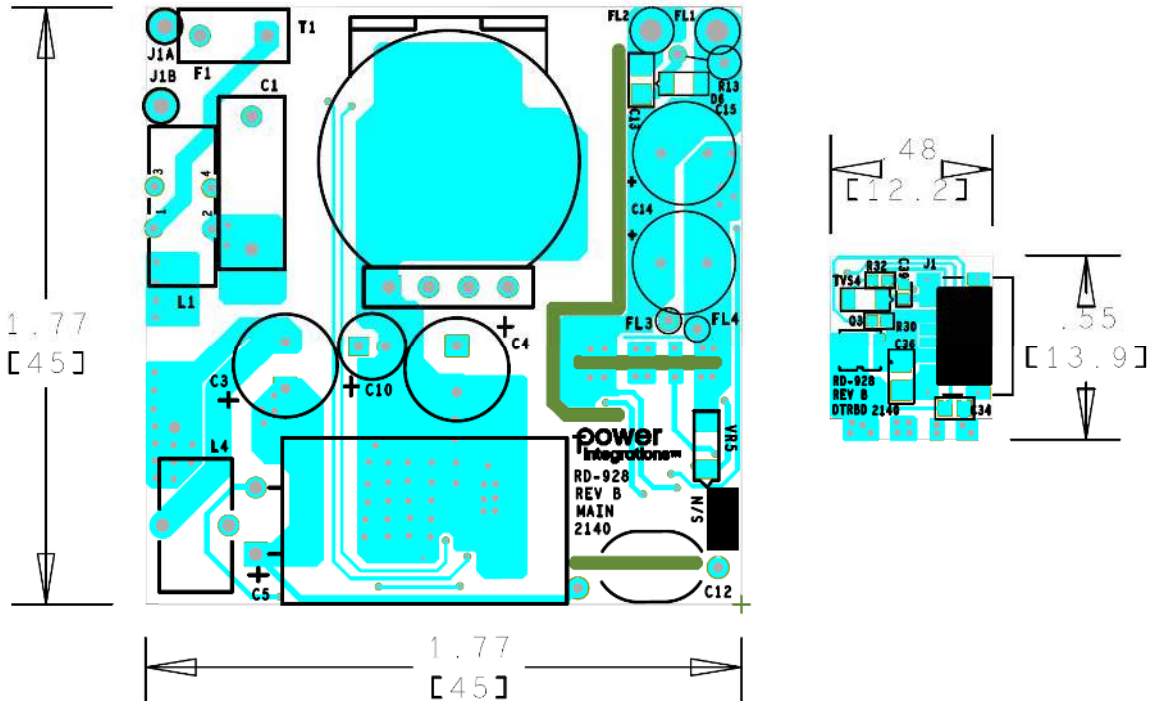


Figure 4 – Printed Circuit Layout, Top.

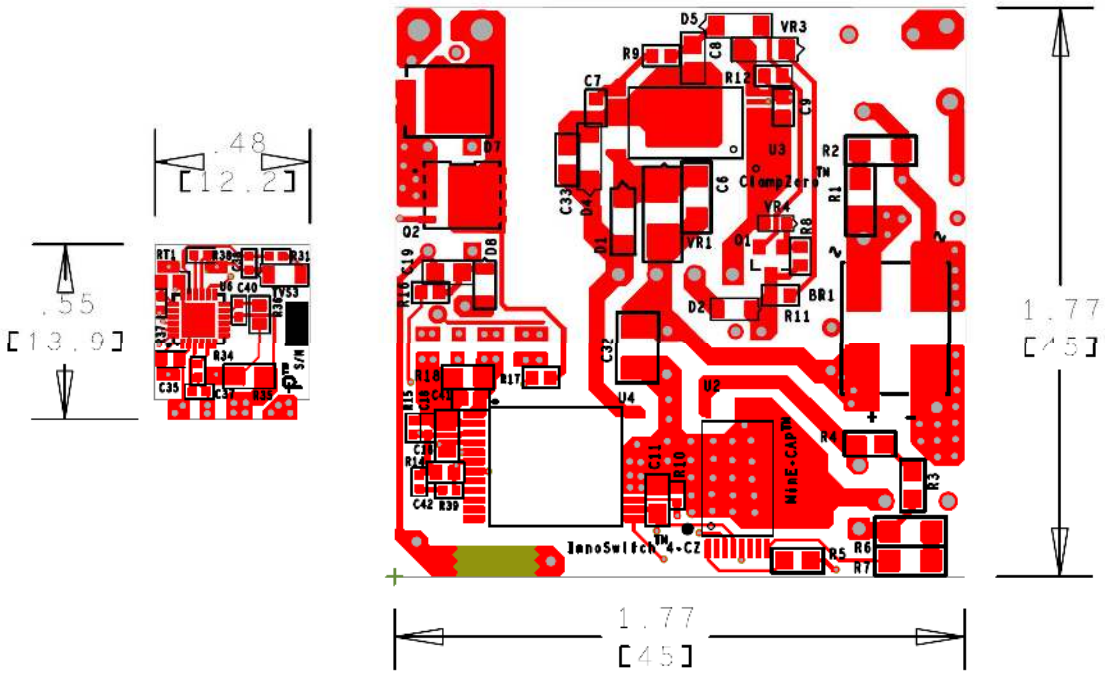


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	0.1 μF, 20%, 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	2	C3 C4	15 μF, ±20%, 400 V, Al Electrolytic, Gen. Purpose, Can, (8 mm x 13 mm)	AKCXD1302G150MF	sh-ymin, http://www.sh-ymin.com
4	1	C5	Electrolytic, 100 μF, ±20%, 160 V, Aluminum, Radial, Can (12.5 X 20)	UCY2C101MHD	Nichicon
5	1	C6	100 nF, 200 V, Ceramic, X7R, 1206	C1206C104K2RACTU	Kemet
6	2	C7 C9	100 nF, 0.1 μF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
7	2	C8 C36	1 μF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AV
8	1	C10	22 μF, ±20%, 63 V, Electrolytic (5 x 12.5), LS 2 mm	63YXJ22M5X11	Rubycon
9	1	C11	470 nF, ±10%,50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung
10	1	C12	470 pF, ±10%, 440 VAC, (X1, Y2) rated, Ceramic, Y5S, Radial, Disc, -40°C ~ 125°C	VY2471K29Y5SS63V7	Vishay
11	1	C13	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
12	2	C14 C15	330 μF, ±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105 °C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
13	1	C16	2.2 μF, ±10%, 25 V, Ceramic, X7R, 0805	CL21B225KAFNFNE	Samsung
14	4	C18 C38 C39 C42	330 pF 16 V, Ceramic, X7R, 0402	C0402C331K4RACTU	Kemet
15	1	C19	10 μF ±10% 25V Ceramic X7S 0805	C2012X7S1E106K125AC	TDK
16	1	C33	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
17	2	C34 C41	1 μF, ±10%,35 V, Ceramic, X7R, 0603	CGA3E1X7R1V105K080AE	TDK
18	1	C35	2.2 μF, ±10%, 25 V, Ceramic, X7R, 0603, -55 to 125 °C	GRM188Z71E225KE43D	Murata
19	2	C37 C40	0.015 μF ±10% 35V Ceramic X7R 0402	CGCGA2B3X7R1V153K050BB	TDK
20	2	D1 D5	800 V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
21	1	D2	DIODE, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
22	1	D4	Diode, Schottky, 20 V, 1 A, SMT, SOD-123FL	DSS12UTR	SMC Diode
23	2	D6 D8	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
24	1	D7	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay
25	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
26	2	FL1 FL2	Flying Lead, Hole size 70 mils	N/A	N/A
27	2	FL3 FL4	Flying Lead, Hole size 30 mils	N/A	N/A
28	1	J1	USB-C (USB TYPE-C) Receptacle Connector 24 (6+18 Dummy) Position Surface Mount, Ra; TH	UJC-HP-3-SMT-TR	CUI Devices
29	2	J1A J1B	PCB Terminal Hole, #22 AWG	N/A	N/A
30	1	L1	415 μH, Toroidal Common Mode Choke, custom, wound on 32-00330-00 core CMC	32-00412-00 TSD-4697	Power Integrations Premier Magnetics
31	1	L4	68 μH, Unshielded Toroidal Inductor, 2 A, 55 mΩ Max, Radial, Vertical (Open) Inductor	7447033 TSD-4405	Wurth Premier Magnetics
32	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
33	1	Q2	MOSFET, N-CH, 100V, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
34	1	Q3	MOSFET, N-CH, 30V, 45A (Ta), 75A (Tc), 4.1W (Ta), 46W (Tc), 8-DFN-EP (3.3x3.3),8-PowerWDFN	AON7510	Alpha & Omega Semi
35	2	R6 R7	RES, 2.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
36	2	R3 R4	RES, 2 MΩ, 5%, 1/8 W, Thick Film, 0805	KTR10EZPJ205	Rohm
37	1	R5	RES, 1.0 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ105V	Panasonic

38	1	R8	RES, 47 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
39	1	R9	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
40	1	R10	RES, 30 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ303X	Panasonic
41	2	R11 R17	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
42	1	R12	RES, 1.8 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ182V	Panasonic
43	1	R13	RES, 10 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-10R	Yageo
44	1	R14	RES, 100 kΩ ±1%, 1/10 W Chip Resistor 0603 Moisture Resistant Thick Film	RC0603FR-07100KL	Yageo
45	1	R15	RES, 33.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3302X	Panasonic
46	1	R16	RES, 470 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ471V	Panasonic
47	1	R18	RES, 0.005 Ω, ±1%, 1/2W, 0805, Current Sense, Thick Film, ±300ppm/°C, -55°C ~ 155°C	ERJ-6LWFR005V	Panasonic
48	1	R30	RES, 100 kΩ, 1%, 1/16 W, Moisture Resistant Thick Film, 0402	RC0402FR-07100KL	Yageo
49	2	R31 R32	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
50	1	R34	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
51	1	R35	RES, 0.005 Ω, 0.5 W, 1%, 0805	PMR10EZPFU5L00	Rohm
52	1	R36	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
53	1	R37	RES, 82 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ823X	Panasonic
54	1	R39	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
55	1	RT1	NTC Thermistor, 100 kΩ, 1%, 0603	NTCG164KF104FT1S	TDK
56	1	SHT1	Isolation Barrier for DER928RevA. Made from White color Formex GK-17 material (PI# 66-00015-00)	61-00301-00	Power Integrations
57	1	SHT2	Y cap Isolation Barrier\DER928RevA. Made from White color Formex GK-17 material (PI# 66-00015-00)	61-00302-00	Power Integrations
58	1	T1	Bobbin, ATQ23.2/11.6, Horizontal, 4 pins. (Mates with core 99-00090-00) Transformer	TBI-238-10501.11x6 POL-INN048	TBI -Transformer Bobbin Industrial Co Premier Magnetics
59	2	TVS3 TVS4	Bidirectional TVS Diode, Voltage - Reverse Standoff (Typ) 24Vmax, 42V Clamp, 7A (8/20µs) Ipp, Surface Mount, SC-76, SOD-323	SD24C-01FTG	Littlefuse
60	1	U2	MinE-CAP	MIN1072M	Power Integrations
61	1	U3	ClampZero, MinSOP-16	CPZ1062M	Power Integrations
62	1	U4	InnoSwitch4-CZ, insop-24D	INN4073C-H182	Power Integrations
63	1	U6	IC, Fast Charging Physical Layer IC for USB Interfaces	IP2726	INJOINIC TECHNOLOGY
64	1	VR1	TVS DIODE, 275 V Clamp, 1.4 A Ipp, Tvs Diode, Surface Mount, SMA SMAJ (DO-214AC)	SMAJ170A-13-F	Diodes, Inc.
65	1	VR3	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
66	1	VR4	10 V, 5%, 150 mW, SSMINI-2,SC-79, SOD-523,EMD2	EDZVT2R10B	Rohm
67	1	VR5	DIODE ZENER 5.1 V 500 mW SOD123	MMSZ5231B-7-F	Diodes, Inc.

7 Transformer Specification

7.1 *Electrical Diagram*

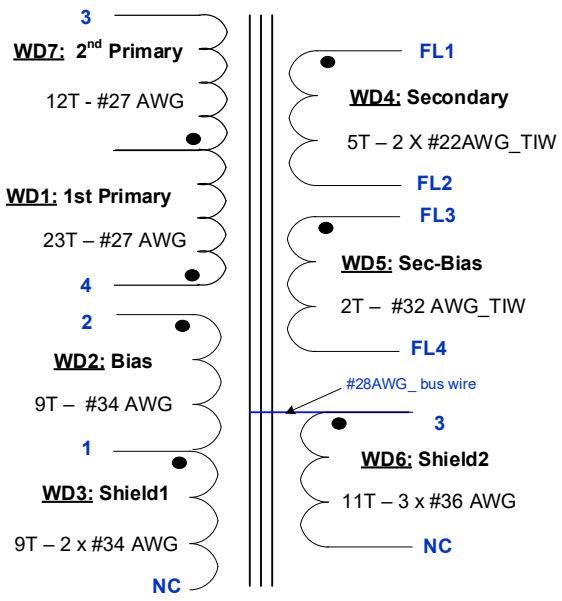


Figure 6 –Transformer Electrical Diagram

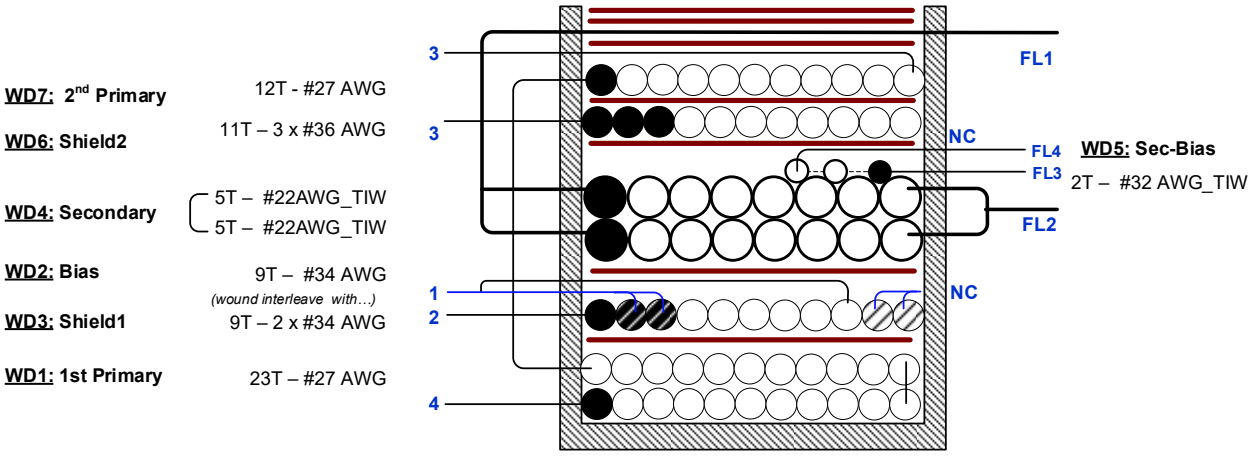
7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	530 µH ±5%
Resonant Frequency	Between pin 3 and 4, other windings open.	1,200 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 4, with pins: FL1-FL2 shorted.	7.5 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: ATQ23/11.
[2]	Bobbin: ATQ23/11-Vertical - 4pins (4/0).
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #36 AWG, Double Coated.
[6]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[7]	Magnet Wire: #32 AWG, Triple Insulated Wire.
[8]	Bus Wire: #28 AWG, Alpha wire, tinned copper, 40.0 mm Length.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 5.2 mm Width.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 26 mm x 48 mm.
[11]	Varnish: Dolph BC-359.

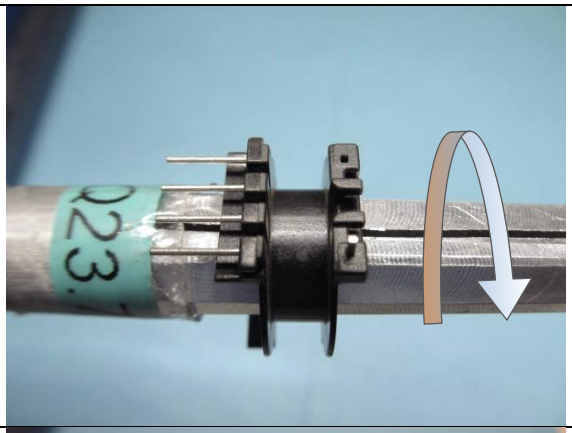
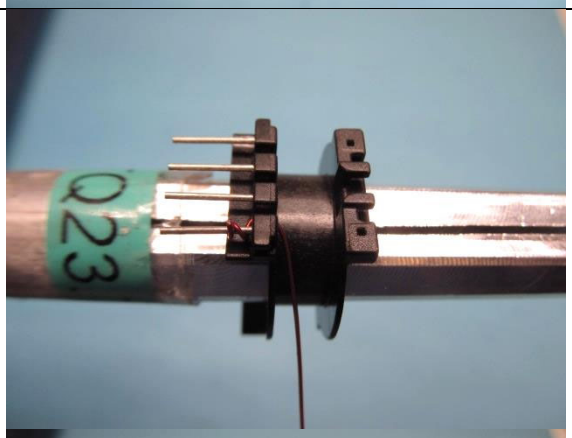
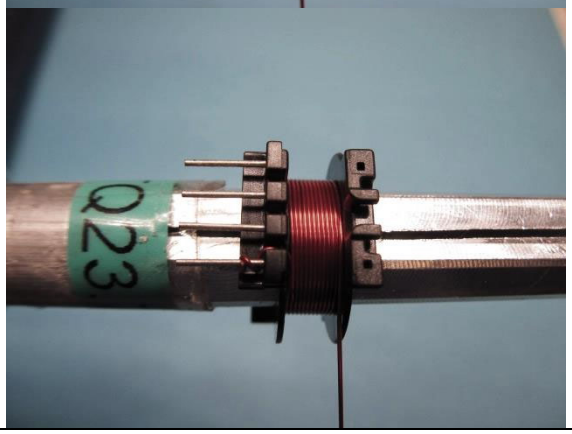
7.4 *Transformer Build Diagram*

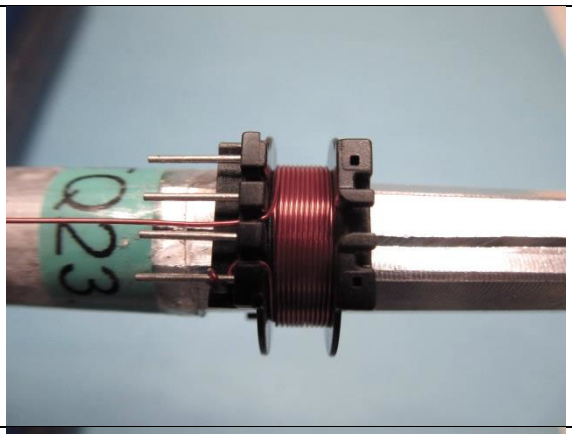
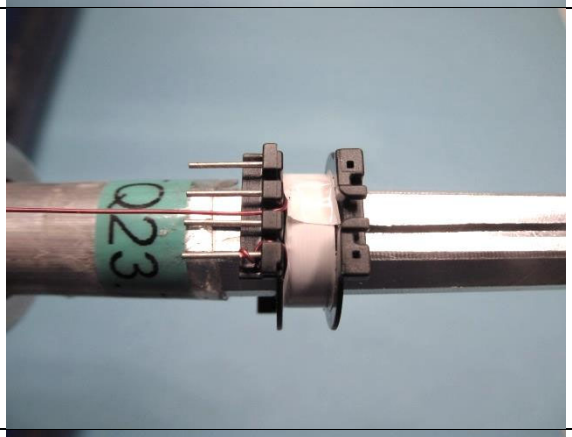
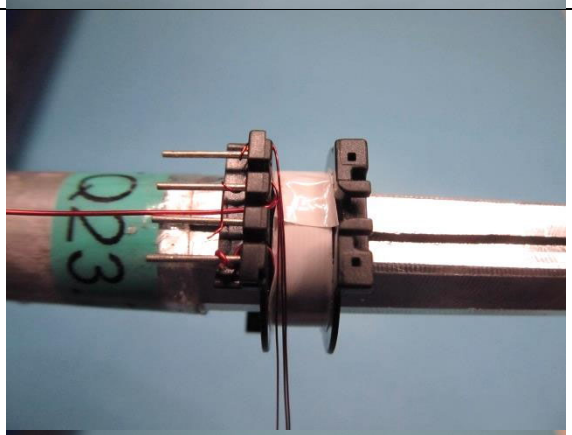
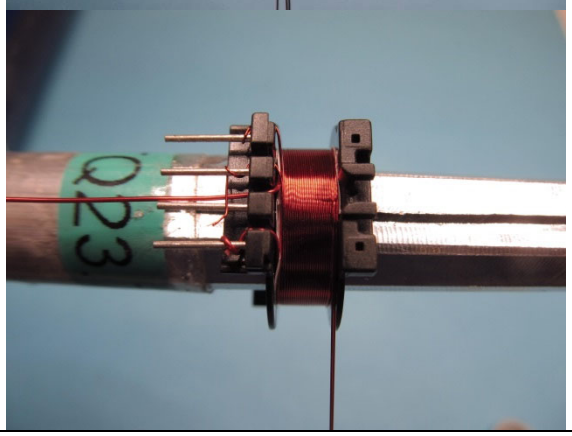


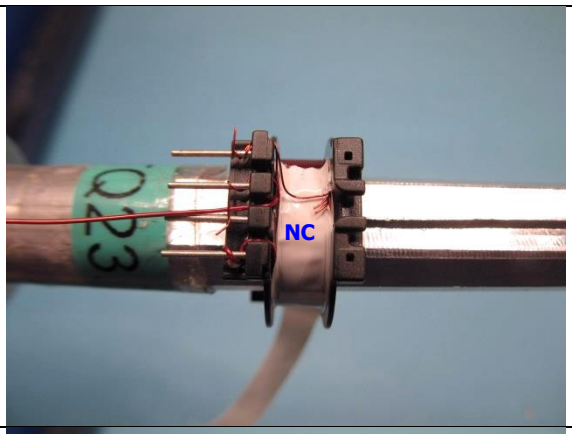
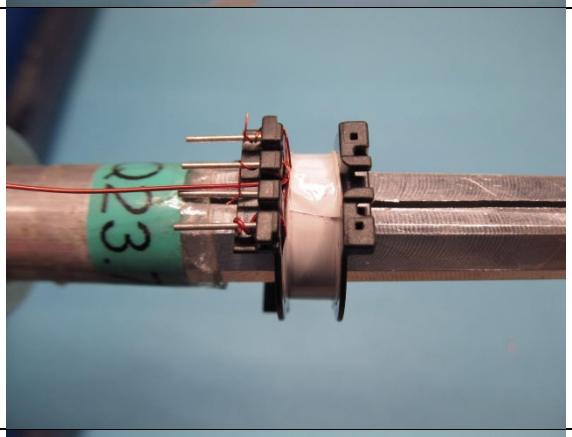
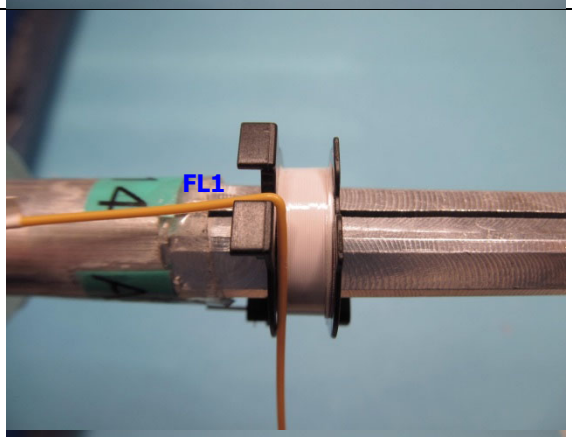
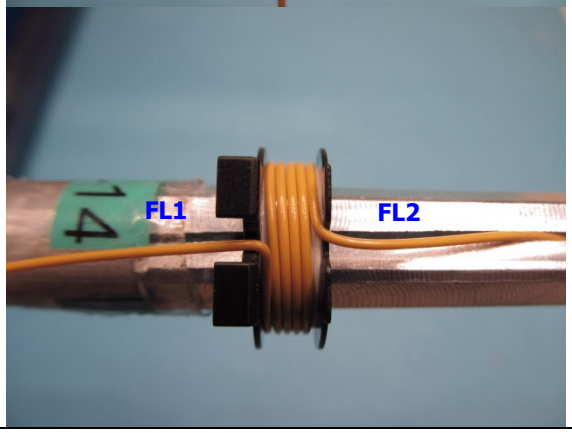
7.5 *Transformer Winding Instruction*

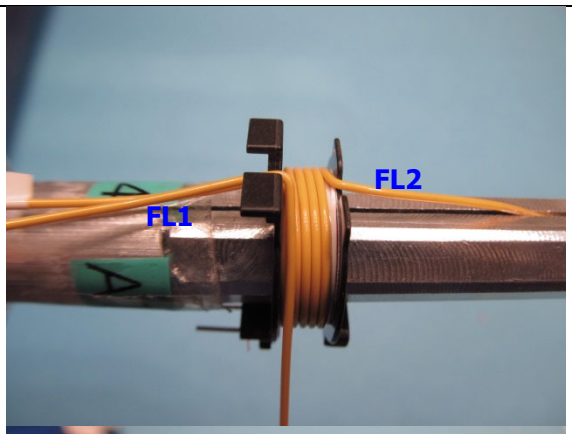
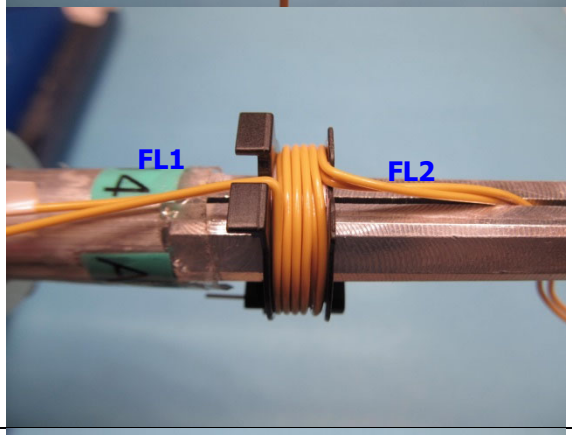
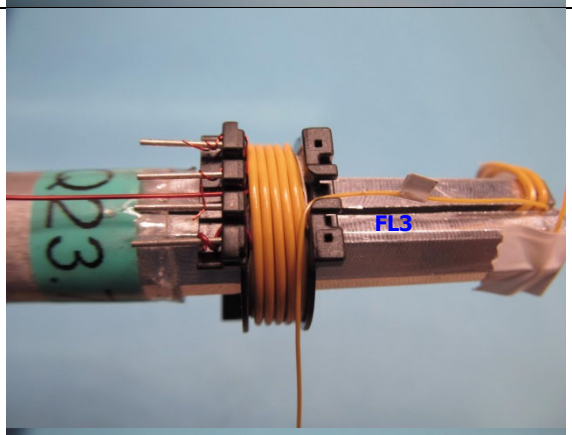
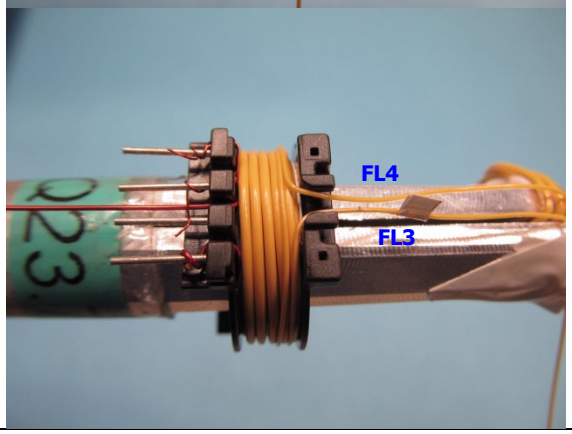
Winding Preparation	Place the bobbin Item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 1st Primary	Start at pin 4, wind 12 turns of wire Item [3] in 1 layer, from left to right, then continue winding another 11 turns from right to left, at the last turn exit the wire out of the bobbin leave enough length of this wire for WD7:2nd Primary.
Insulation	1 layer of tape Item [9].
WD2 & WD3 Bias & Shield 1	Use 1 wire Item [4], starting at pin 2 for WD2-Bias and 2 wires also Item [4], starting at pin 1 for WD3-Shield1. Wind all 3 wires in parallel, at 9th turn, bring the single wire for WD2 to the left to terminate at pin 1, and cut short 2 wires for WD3 as No-Connect (NC).
Insulation	1 layer of tape Item [9].
WD4 Secondary	Start at the slot on the left on secondary side of the bobbin, use 1 wire Item [6], leave ~40mm floating, and mark as FL1, wind 5 turns in 1 layer. At the last turn, exit the wire at the slot on the right also leave ~ 30mm floating and mark as FL2 for 1st halves of Secondary. Repeat another winding as above for 2nd halves of Secondary which is parallel with 1st halves Secondary.
WD5 Secondary Bias	Use wire Item [7], start from the right and on the primary side of bobbin, leaving ~ 30mm and mark as FL3. Wind 2 turns and exit the wire also leaving 30mm and mark as FL4.
Insulation	1 layer of tape Item [9].
WD6 Shield2	Start at pin 3, wind 11 tri-filar turns of wire Item [5]. At the last turn cut short the wires as No-Connect.
Insulation	1 layer of tape Item [9].
WD7 2nd Primary	Use wire floating from WD1, wind 12 turns from left to right. At the last turn, bring the wire back to the left to finish at pin 3.
Insulation	1 layer of tape Item [9] and bring the secondary wires FL1 to the right in between layers of tape.
Finish	Gap cores to get 377uH, solder bus wire Item [6] to pin 3which leans along with core halves, and secure with tape. Varnish Item [11]. Places 2 layers of tape Item [10] at the bottom of transformer and wrap up to cover secondary side of transformer. Wrap around the body of transformer 1 layer of tape Item [9], *(see illustration below).*

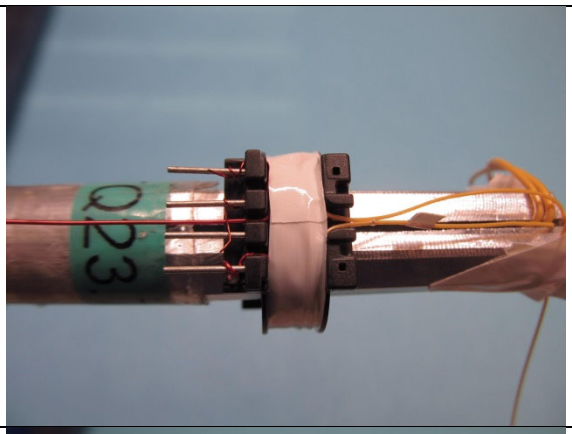
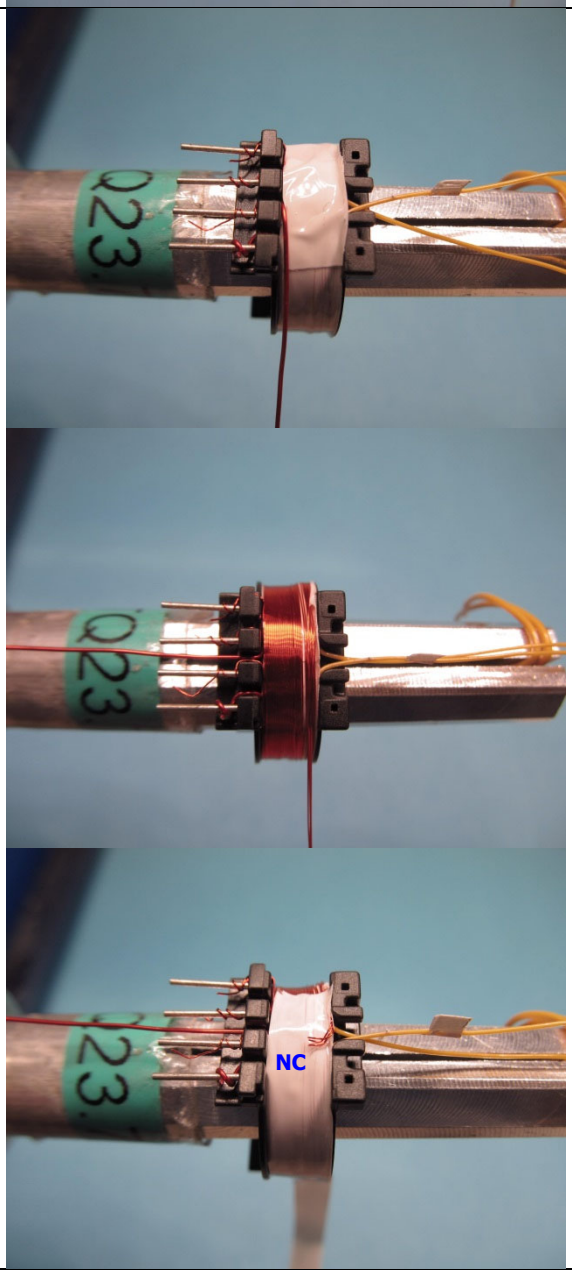
7.6 *Winding Illustrations*

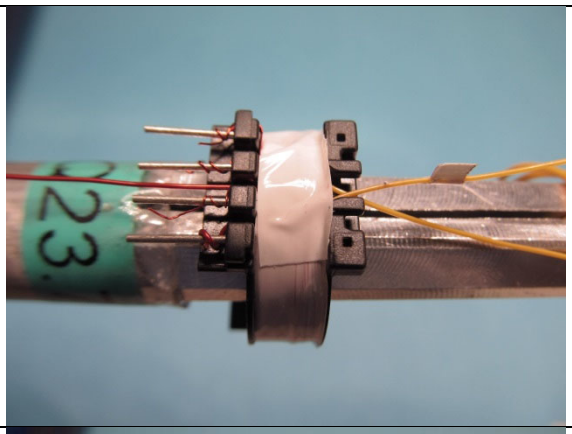
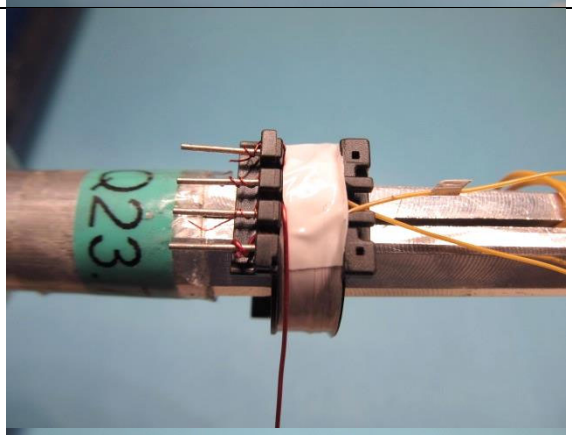
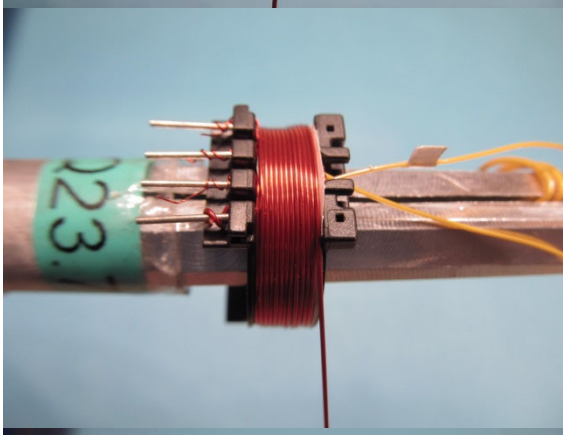
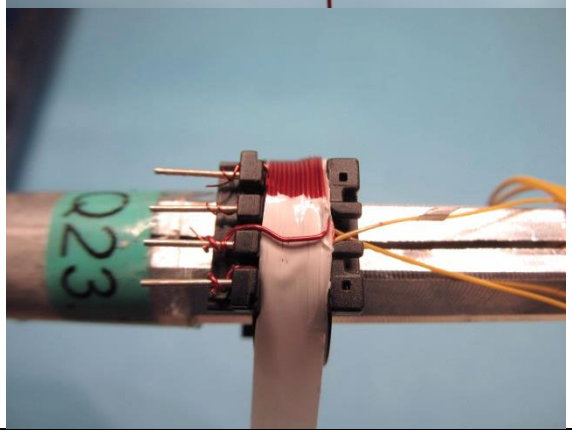
Winding Preparation		Place the bobbin Item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 **1st Primary**	 	Start at pin 4, wind 12 turns of wire Item [3] in 1 layer, from left to right, then continue winding another 11 turns from right to left, at the last turn, exit the wire out of the bobbin leave enough length of this wire for WD7:2nd Primary.

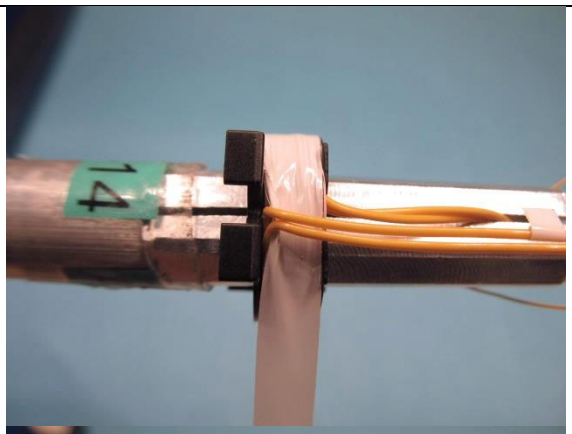
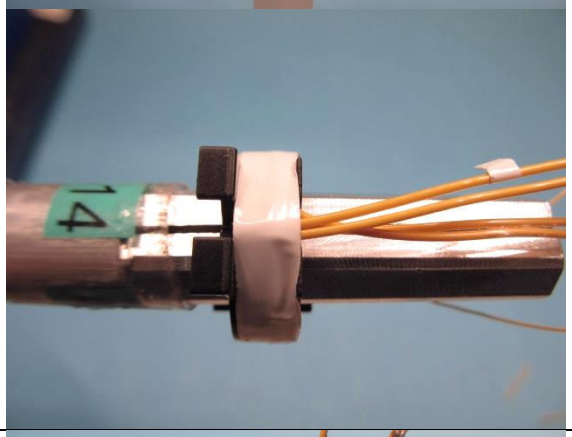
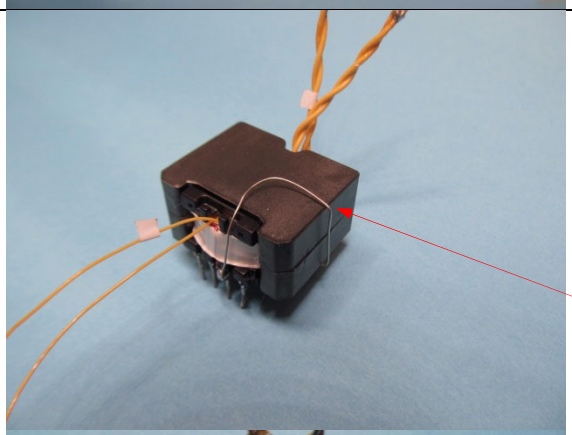
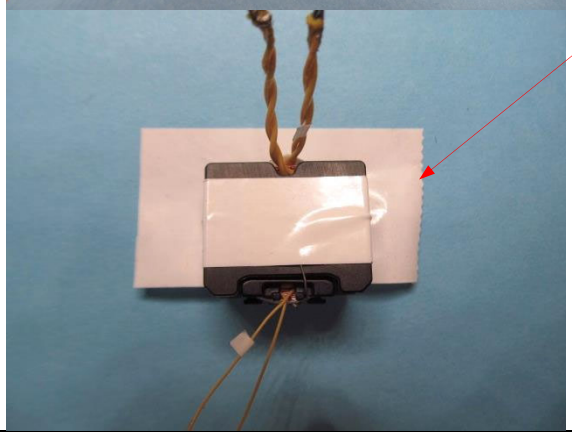
		
Insulation		1 layer of tape Item [9].
WD2 & WD3 Bias & Shield 1	 	Use 1 wire Item [4], starting at pin 2 for WD2-Bias and 2 wires also Item [4], starting at pin 1 for WD3-Shield1. Wind all 3 wires in parallel, at 9th turn, bring the single wire for WD2 to the left to terminate at pin 1, and cut short 2 wires for WD3 as No-Connect (NC).

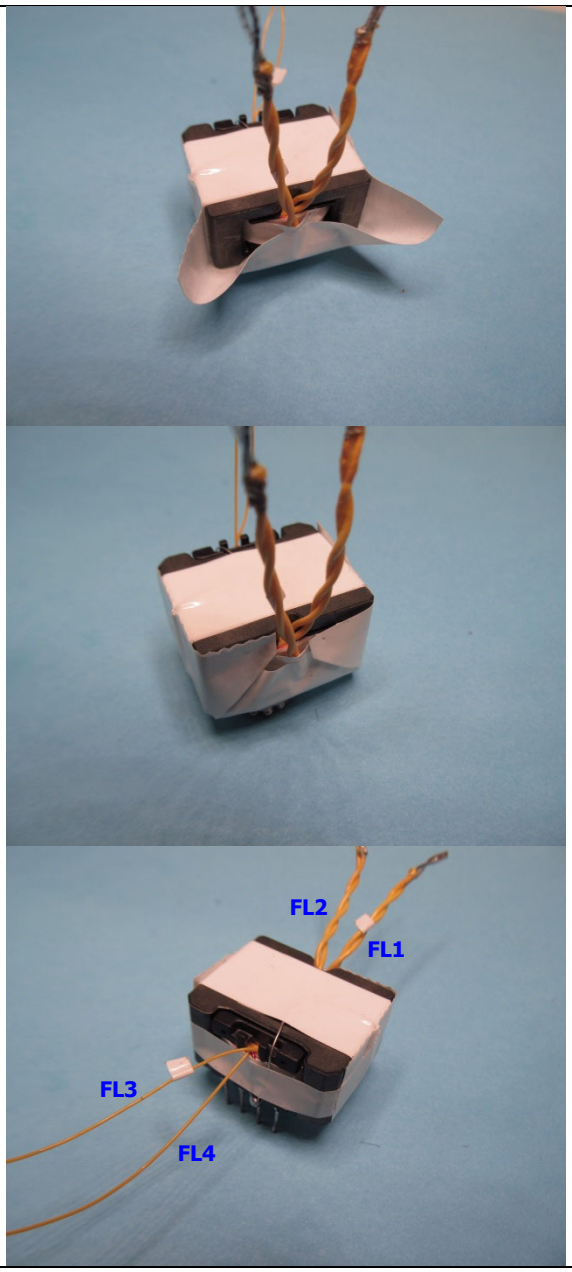
		
Insulation		2 layers of tape Item [9].
WD4 Secondary	 	Start at the slot on the left on secondary side of the bobbin, use 1 wire Item [6], leave ~40 mm floating, and mark as FL1, wind 5 turns in 1 layer. At the last turn, exit the wire at the slot on the right also leave ~30 mm floating and mark as FL2 for 1st halves of Secondary. Repeat another winding as above for 2nd halves of Secondary which is parallel with 1st halves Secondary.

	 	
WD5 **Secondary Bias**	 	Use wire Item [7], start from the right and on the primary side of bobbin, leaving ~30 mm and mark as FL3. Wind 2 turns and exit the wire also leaving 30 mm and mark as FL4.

Insulation		1 layer of tape Item [9].
WD6 **Shield2**		Start at pin 3, wind 11 tri-filar turns of wire Item [5]. At the last turn cut short the wires as No-Connect.

Insulation		1 layer of tape Item [9].
WD7 **2nd Primary**	  	Use wire floating from WD1, wind 12 turns from left to right. At the last turn, bring the wire back to the left to finish at pin 3.

Insulation	 	1 layer of tape Item [9] and bring the secondary wires FL1 to the right in between layers of tape.
Finish	 	Gap cores to get 530uH, solder bus wire Item [6] to pin 3which leans along with core halves, and secure with tape. Varnish Item [11]. Places 2 layers of tape Item [10] at the bottom of transformer and wrap up to cover secondary side of transformer. Wrap around the body of transformer 1 layer of tape Item [9], *(see illustration beside).*


FL2
FL1
FL3
FL4

8 CMC Specification

8.1 *Electrical Diagram*

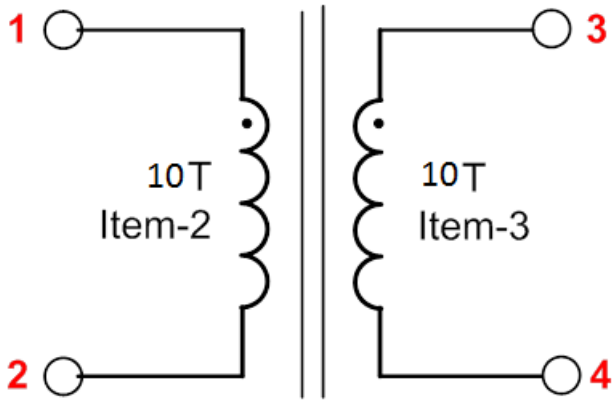


Figure 7 – Choke Electrical Diagram.

8.2 *Electrical Specifications*

Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	415 µH ±30%

8.3 *Material List*

Item	Description
[1]	Toroidal Core: T9*5*3C-JL12, PI#: 32-00330-00.
[2]	Triple Insulated Wire: #26 AWG, Triple Coated.
[3]	Magnet Wire: #26 AWG, Double Coated.

8.4 *Assembled Picture*

9 Transformer Design Spreadsheet

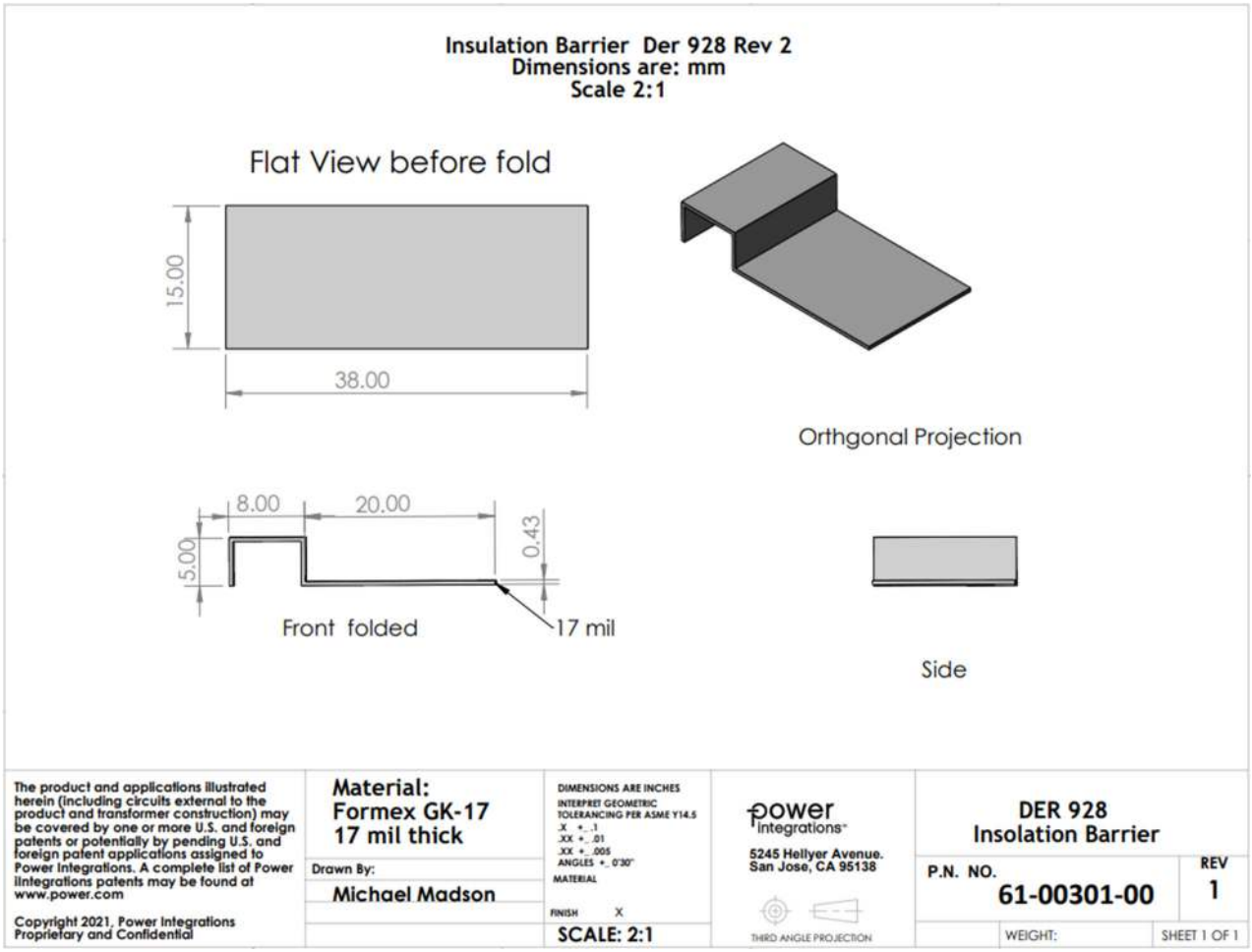
1	ACDC_InnoSwitch4-CZ USB-PD_Flyback_050321; Rev.0.4; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4-CZ USB-PD Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	90		90	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		AC line voltage range
7	FLINE			60	Hz	AC line voltage frequency
8	CAP_INPUT	130.0		130.0	uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	3.000		3.000	A	Output current 1
13	POUT1			60.00	W	Output power 1
14	EFFICIENCY1	0.92		0.92		Converter efficiency for output 1
15	Z_FACTOR1	0.50		0.50		Z-factor for output 1
24	**SET-POINT 2**					
25	VOUT2	15.00		15.00	V	Output voltage 2
26	IOUT2	3.000		3.000	A	Output current 2
27	POUT2			45.00	W	Output power 2
28	EFFICIENCY2	0.91		0.91		Converter efficiency for output 2
29	Z_FACTOR2	0.50		0.50		Z-factor for output 2
31	**SET-POINT 3**					
32	VOUT3	9.00		9.00	V	Output voltage 3
33	IOUT3	3.000		3.000	A	Output current 3
34	POUT3			27.00	W	Output power 3
35	EFFICIENCY3	0.90		0.90		Converter efficiency for output 3
36	Z_FACTOR3	0.50		0.50		Z-factor for output 3
38	**SET-POINT 4**					
39	VOUT4	5.00		5.00	V	Output voltage 4
40	IOUT4	3.000		3.000	A	Output current 4
41	POUT4			15.00	W	Output power 4
42	EFFICIENCY4	0.89		0.89		Converter efficiency for output 4
43	Z_FACTOR4	0.50		0.50		Z-factor for output 4
77	**PRIMARY CONTROLLER SELECTION**					
78	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
79	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
80	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
81	DEVICE_GENERIC	INN4X73		INN4X73		Device selection
82	DEVICE_CODE			INN4X73C		Device code
83	PDEVICE_MAX			60	W	Device maximum power capability
84	RDSON_25DEG			0.64	Ω	Primary switch on-time resistance at 25°C
85	RDSON_100DEG			0.96	Ω	Primary switch on-time resistance at 100°C
86	ILIMIT_MIN			1.581	A	Primary switch minimum current limit
87	ILIMIT_TYP			1.700	A	Primary switch typical current limit
88	ILIMIT_MAX			1.819	A	Primary switch maximum current limit
89	VDRAIN_ON_PRSW			0.61	V	Primary switch on-time voltage drop
90	VDRAIN_OFF_PRSW			583.31	V	Peak drain voltage on the primary switch during turn-off
94	**WORST CASE ELECTRICAL PARAMETERS**					
95	FSWITCHING_MAX	112000		112000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
96	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding

						to set-point 1) when the primary switch turns off
97	VMIN			98.52	V	Valley of the rectified minimum input AC voltage at full load
98	KP			0.630		Measure of continuous/discontinuous mode of operation
99	MODE_OPERATION			CCM		Mode of operation
100	DUTYCYCLE			0.588		Primary switch duty cycle
101	TIME_ON			9.21	us	Primary switch on-time
102	TIME_OFF			3.17	us	Primary switch off-time
103	LPRIMARY_MIN			503.3	uH	Minimum primary magnetizing inductance
104	LPRIMARY_TYP			529.8	uH	Typical primary magnetizing inductance
105	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
106	LPRIMARY_MAX			556.3	uH	Maximum primary magnetizing inductance
108	**PRIMARY CURRENT**					
109	IAVG_PRIMARY			0.639	A	Primary switch average current
110	IPEAK_PRIMARY			1.782	A	Primary switch peak current
111	IPEDESTAL_PRIMARY			0.587	A	Primary switch current pedestal
112	IRIPPLE_PRIMARY			1.641	A	Primary switch ripple current
113	IRMS_PRIMARY			0.889	A	Primary switch RMS current
115	**SECONDARY CURRENT**					
116	IPEAK_SECONDARY			12.475	A	Secondary winding peak current
117	IPEDESTAL_SECONDARY			4.106	A	Secondary winding pedestal current
118	IRMS_SECONDARY			5.202	A	Secondary winding RMS current
119	IRIPPLE_CAP_OUT			4.250	A	Output capacitor ripple current
123	**TRANSFORMER CONSTRUCTION PARAMETERS**					
124	**CORE SELECTION**					
125	CORE	CUSTOM		CUSTOM		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
126	CORE NAME	ATQ2311		ATQ2311		Core code
127	AE	81.0		81.0	mm^2	Core cross sectional area
128	LE	36.0		36.0	mm	Core magnetic path length
129	AL	7700		7700	nH	Ungapped core effective inductance per turns squared
130	VE	3920		3920	mm^3	Core volume
131	BOBBIN NAME	ATQ2311		ATQ2311		Bobbin name
132	AW	52.0		52.0	mm^2	Bobbin window area
133	BW	5.10		5.10	mm	Bobbin width
134	MARGIN			0.0	mm	Bobbin safety margin
136	**PRIMARY WINDING**					
137	NPRIMARY			35		Primary winding number of turns
138	BPEAK			3722	Gauss	Peak flux density
139	BMAX			3464	Gauss	Maximum flux density
140	BAC			1569	Gauss	AC flux density (0.5 x Peak to Peak)
141	ALG			432	nH	Typical gapped core effective inductance per turns squared
142	LG			0.222	mm	Core gap length
144	**PRIMARY BIAS WINDING**					
145	NBIAS_PRIMARY			9		Primary bias winding number of turns
147	**SECONDARY WINDING**					
148	NSECONDARY	5		5		Secondary winding number of turns
150	**SECONDARY BIAS WINDING**					
151	NBIAS_SECONDARY			2		Secondary bias winding number of turns
154	**PRIMARY COMPONENTS SELECTION**					
155	**CLAMPZERO**					
156	LLEAK	7.500		7.500	uH	Primary winding leakage inductance
157	CCLAMP	100.0		100.0	nF	Primary clamp capacitor
158	RD_CLAMPZERO	30		30	kΩ	HSD resistor
159	TDEL5_CLAMPZERO			120.0	ns	HSD resistor programmed delay

160	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			60.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
161	TIME_VDS_VALLEY			56.4	ns	Time taken by the VDS ring to reach its first valley
162	IPEAK_CLAMPZERO			1.732	A	Active clamp peak current
164	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
165	BROWN-IN REQURED			72.00	V	Required line brown-in threshold
166	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
167	BROWN-IN ACTUAL			71.40	V	Actual brown-in threshold using standard resistors
168	BROWN-OUT ACTUAL			64.58	V	Actual brown-out threshold using standard resistors
169	OVERVOLTAGE_LINE			297.50	V	Actual AC RMS line over-voltage threshold
171	**PRIMARY BIAS WINDING**					
172	VBIAS_PRIMARY	8.00	Info	8.00	V	The rectified primary bias voltage maybe too low to supply the BPP pin: Increase the rectified primary bias voltage to a value higher than 9V
173	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
174	VREVERSE_BIASDIODE_PRIMARY			103.99	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
175	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
176	CBPP			0.47	uF	BPP pin capacitor
180	**SECONDARY COMPONENTS SELECTION**					
181	**RECTIFIER**					
182	VDRAIN_OFF_SRFET			73.33	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
183	SRFET			0		Secondary rectifier (Logic MOSFET)
184	VBREAKDOWN_SRFET			150	V	Secondary rectifier breakdown voltage
185	RDSON_SRFET			0.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
187	**SECONDARY BIAS WINDING**					
188	VBIAS_SECONDARY	6.00		6.00	V	Rectified secondary bias voltage at full load
189	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
190	VREVERSE_BIASDIODE_SECONDARY			80.66	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
191	CBIAS_SECONDARY			22	uF	Secondary bias winding rectification capacitor
192	CBPS			2.20	uF	BPS pin capacitor
196	**SET-POINTS ANALYSIS**					
197	**TOLERANCE CORNER**					
198	VIN			90	V	Input AC RMS voltage to be evaluated
199	IOUT			3.00	A	Output current to be evaluated
200	ILIMIIT			1.700	A	Current limit to be evaluated
201	LPRIMARY			529.8	uH	Primary inductance to be evaluated
203	**SET-POINT SELECTION**					
204	SET-POINT	1		1		Select the set-point which needs to be evaluated
205	FSWITCHING			90969.7	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
206	VOR			140.0	V	Voltage reflected to the primary winding when the primary switch turns off
207	VMIN			98.52	V	Valley of the minimum input AC voltage
208	KP			0.710		Measure of continuous/discontinuous mode of operation
209	MODE_OPERATION			CCM		Mode of operation
210	DUTYCYCLE			0.588		Primary switch duty cycle
211	TIME_ON			8.25	us	Primary switch on-time
212	TIME_OFF			4.02	us	Primary switch off-time
214	**PRIMARY CURRENT**					
215	IAVG_PRIMARY			0.639	A	Primary switch average current
216	IPEAK_PRIMARY			1.684	A	Primary switch peak current
217	IPEDESTAL_PRIMARY			0.489	A	Primary switch current pedestal

218	IRIPPLE_PRIMARY			1.196	A	Primary switch ripple current
219	IRMS_PRIMARY			0.875	A	Primary switch RMS current
221	**SECONDARY CURRENT**					
222	IPEAK_SECONDARY			11.791	A	Secondary winding peak current
223	IPEDESTAL_SECONDARY			3.422	A	Secondary winding pedestal current
224	IRMS_SECONDARY			5.120	A	Secondary winding RMS current
225	IRIPPLE_CAP_OUT			4.149	A	Output capacitor ripple current
227	**MAGNETIC FLUX DENSITY**					
228	BPEAK			3313	Gauss	Peak flux density
229	BMAX			3148	Gauss	Maximum flux density
230	BAC			1117	Gauss	AC flux density (0.5 x Peak to Peak)

10 Isolation Barrier Insulator Drawings



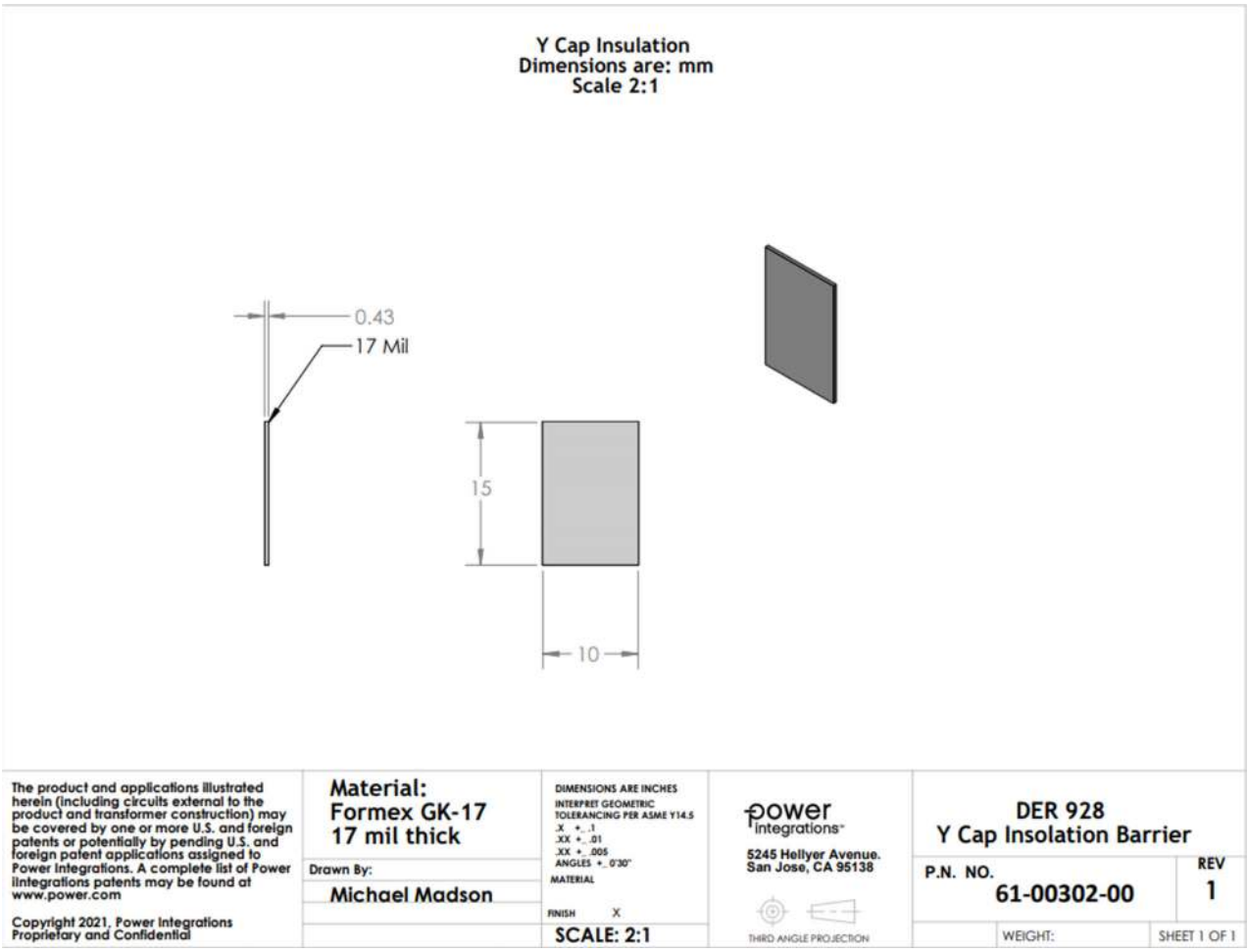
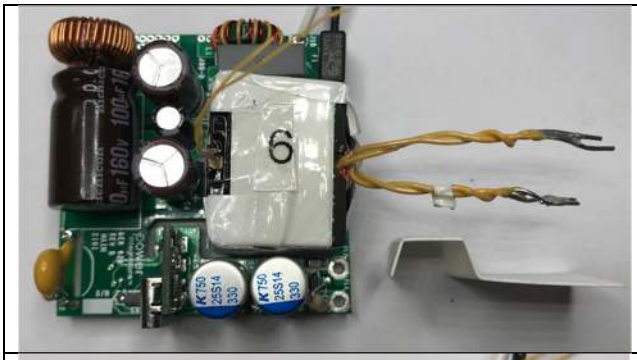
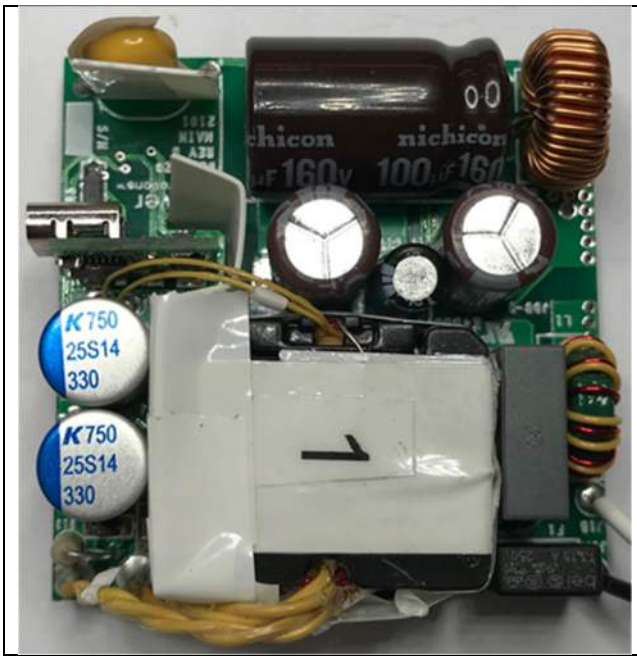


Figure 8 – Isolation barrier drawings.

11 Assembly Instructions

11.1 *Isolation Barrier Insulator Assembly Instructions*

	Prepare the isolation barrier insulator
	Insert the isolation barrier insulator into the dedicated slot
	Secure the isolation barrier insulator with a tape attaching to the transformer and the insulator. 10 mm wide 3M 13450-F polyester film 1mil thick tape was used.

	Secure the isolation barrier insulator with a tape attaching to the Y capacitor and the insulator. 10 mm wide 3M 13450-F polyester film 1mil thick tape was used.

12 Performance Data

Output voltages are measured at the PCB end and all the measurements are taken at room temperature unless otherwise specified.

12.1 *No-Load Input Power at 5 V_{OUT}*

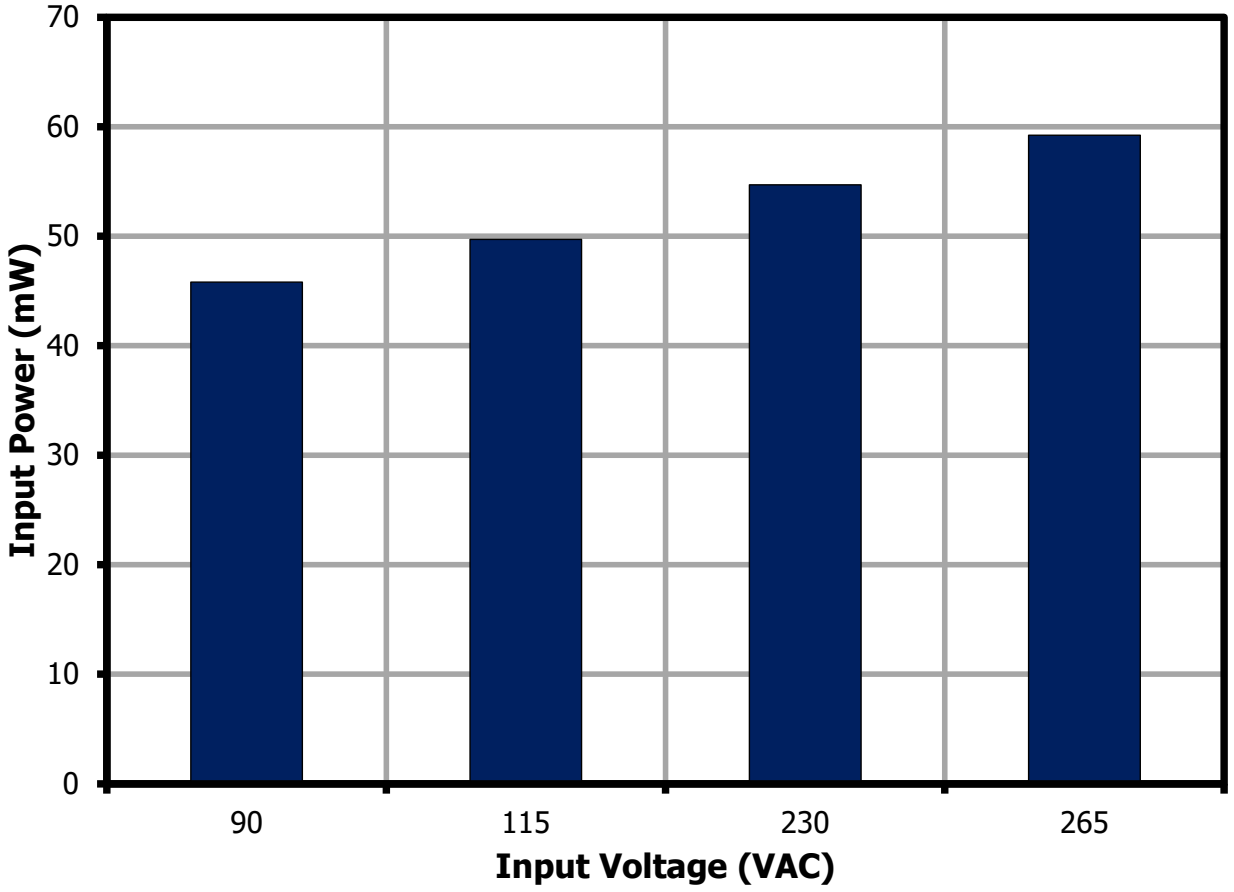


Figure 9 – No-Load Input Power vs. Input Line Voltage.

12.2 *Average and 10% Load Efficiency*

Note: Output voltage measured at the USB-PD connector on the board. Efficiency measured at room temperature after warming up the unit for 30min @ full load.

12.2.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.4%	81.8%	72.5%
9	>6	27	86.6%	87.3%	77.3%
15	>6	45	87.7%	88.9%	78.9%
20	>6	60	88.0%	89.0%	79.0%

12.2.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	90.29	89.51	85.38	82.48
9	27	91.27	91.62	84.46	84.21
15	45	91.59	92.83	85.07	85.94
20	60	91.47	93.15	85.24	86.58

12.2.3 Average and 10% Load Efficiency at 115 VAC

12.2.3.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.35	90.50	**90.29**
75	11.52	90.74	
50	7.68	90.85	
25	3.82	89.07	
10	1.52	85.38	

12.2.3.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.34	91.64	**91.27**
75	20.53	91.71	
50	13.68	91.56	
25	6.83	90.15	
10	2.72	84.46	

12.2.3.3 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	45.21	92.02	**91.59**
75	33.95	91.96	
50	22.67	91.81	
25	11.33	90.57	
10	4.51	85.07	

12.2.3.4 Output: 20 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	60.39	91.95	**91.47**
75	45.28	91.89	
50	30.21	91.68	
25	15.10	90.36	
10	6.01	85.24	

12.2.4 Average and 10% Load Efficiency at 230 VAC

12.2.4.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.41	90.57	**89.51**
75	11.55	90.51	
50	7.68	89.84	
25	3.82	87.14	
10	1.52	82.48	

12.2.4.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.43	92.53	**91.62**
75	20.57	92.41	
50	13.69	91.87	
25	6.83	89.66	
10	2.72	84.21	

12.2.4.3 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	45.30	93.53	**92.83**
75	34.00	93.35	
50	22.68	93.00	
25	11.33	91.45	
10	4.51	85.94	

12.2.4.4 Output: 20 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	60.35	93.82	**93.15**
75	45.30	93.67	
50	30.22	93.32	
25	15.10	91.80	
10	6.01	86.58	

12.3 *Efficiency Across Line (On Board)*

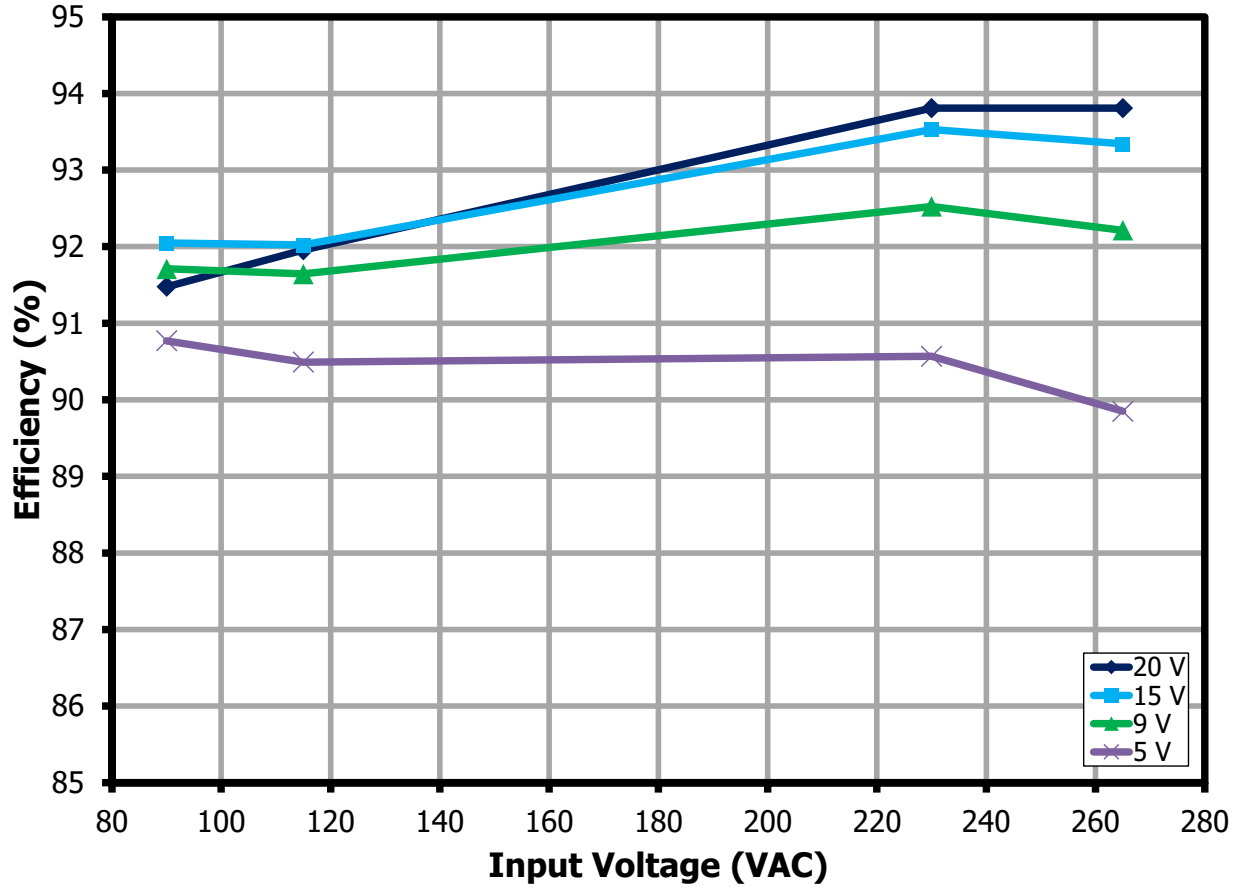


Figure 10 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

12.4 *Load Regulation (On Board)*

12.4.1 Output: 5 V / 3 A

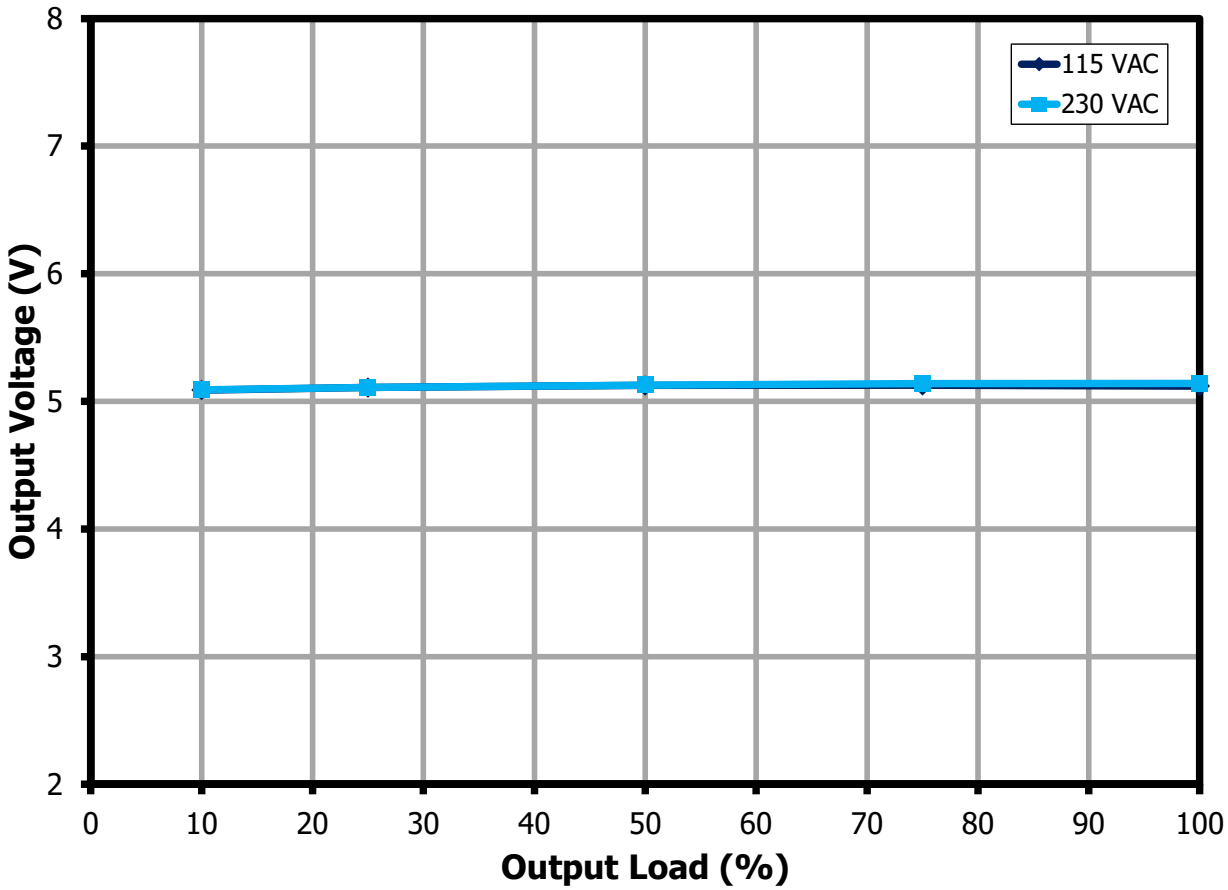


Figure 11 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

12.4.2 Output: 9 V / 3 A

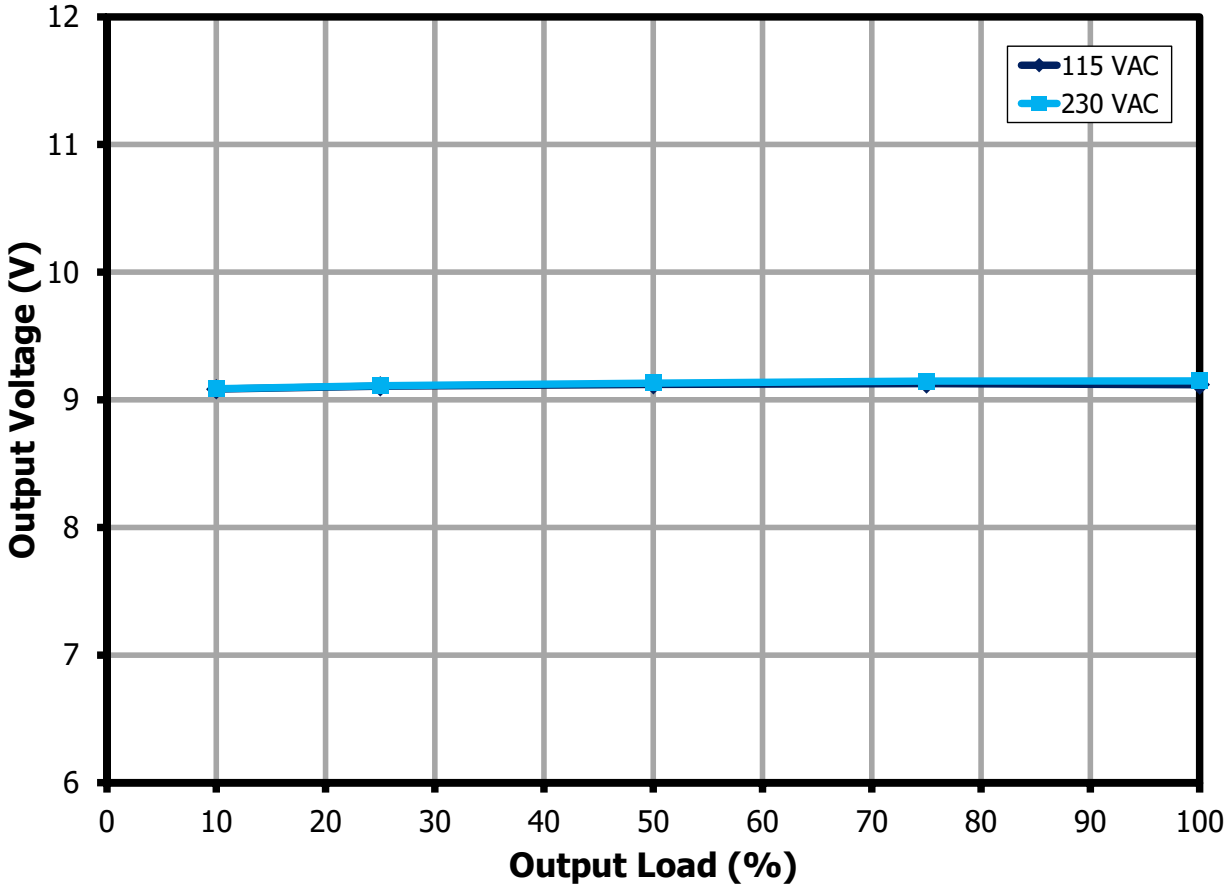


Figure 12 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

12.4.3 Output: 15 V / 3 A

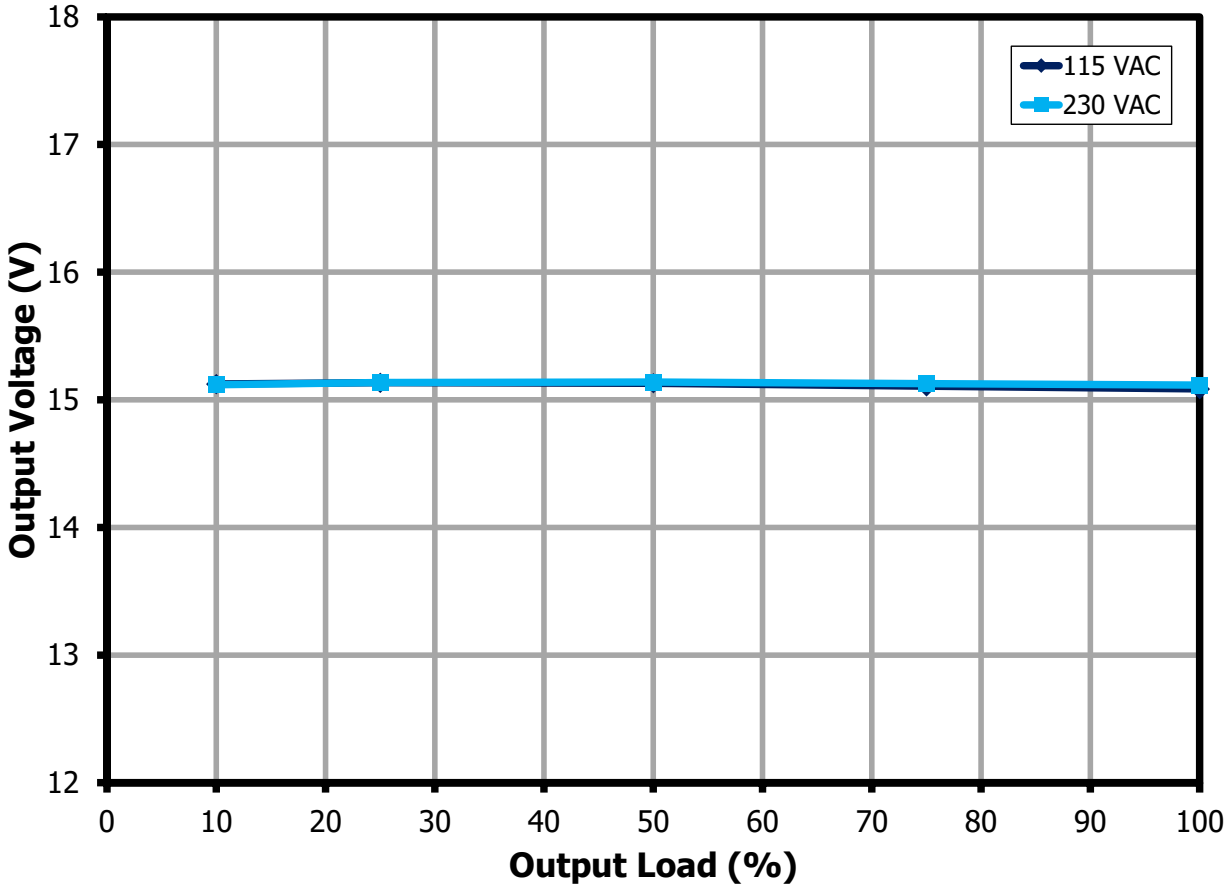


Figure 13 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

12.4.4 Output: 20 V / 3 A

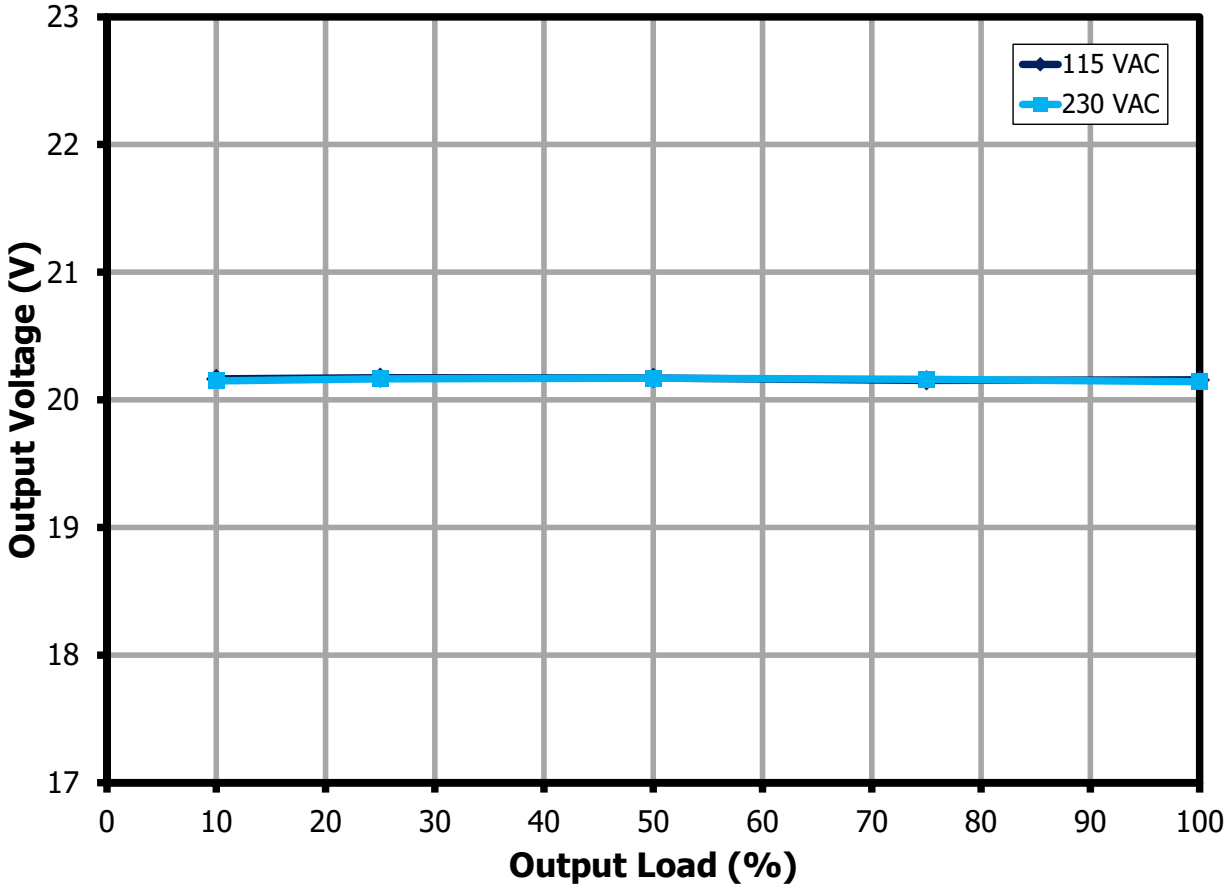


Figure 14 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

12.5 *Line Regulation (On Board)*

12.5.1 Output: 5 V / 3 A

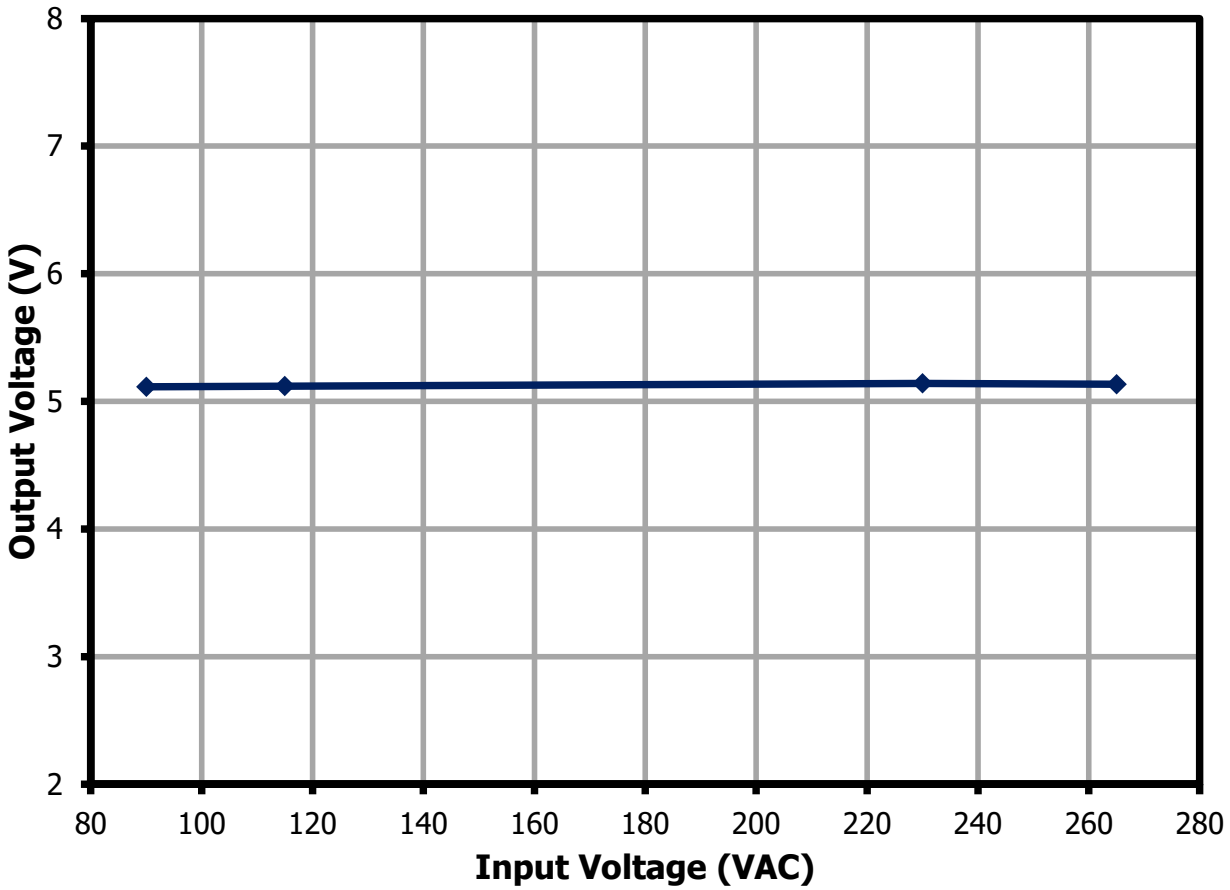


Figure 15 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

12.5.2 Output: 9 V / 3 A

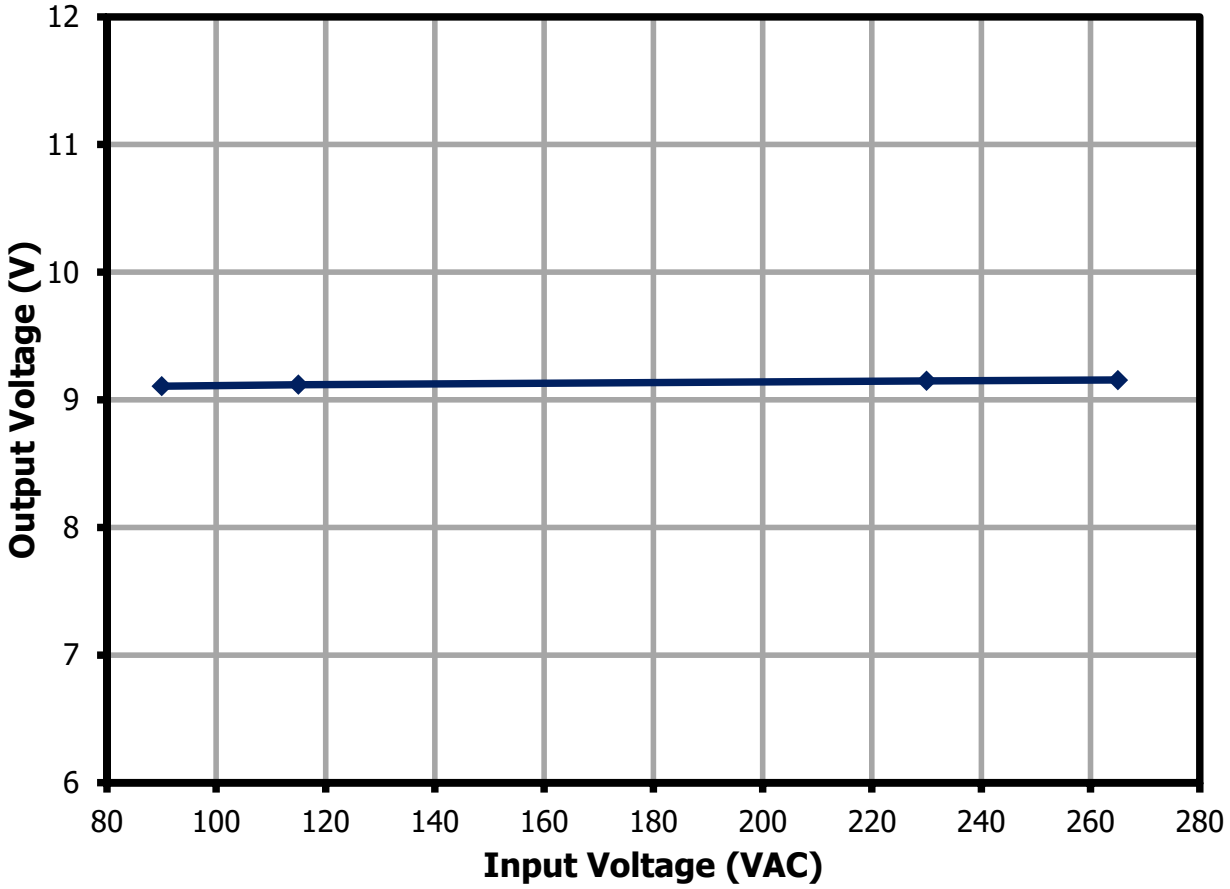


Figure 16 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

12.5.3 Output: 15 V / 3 A

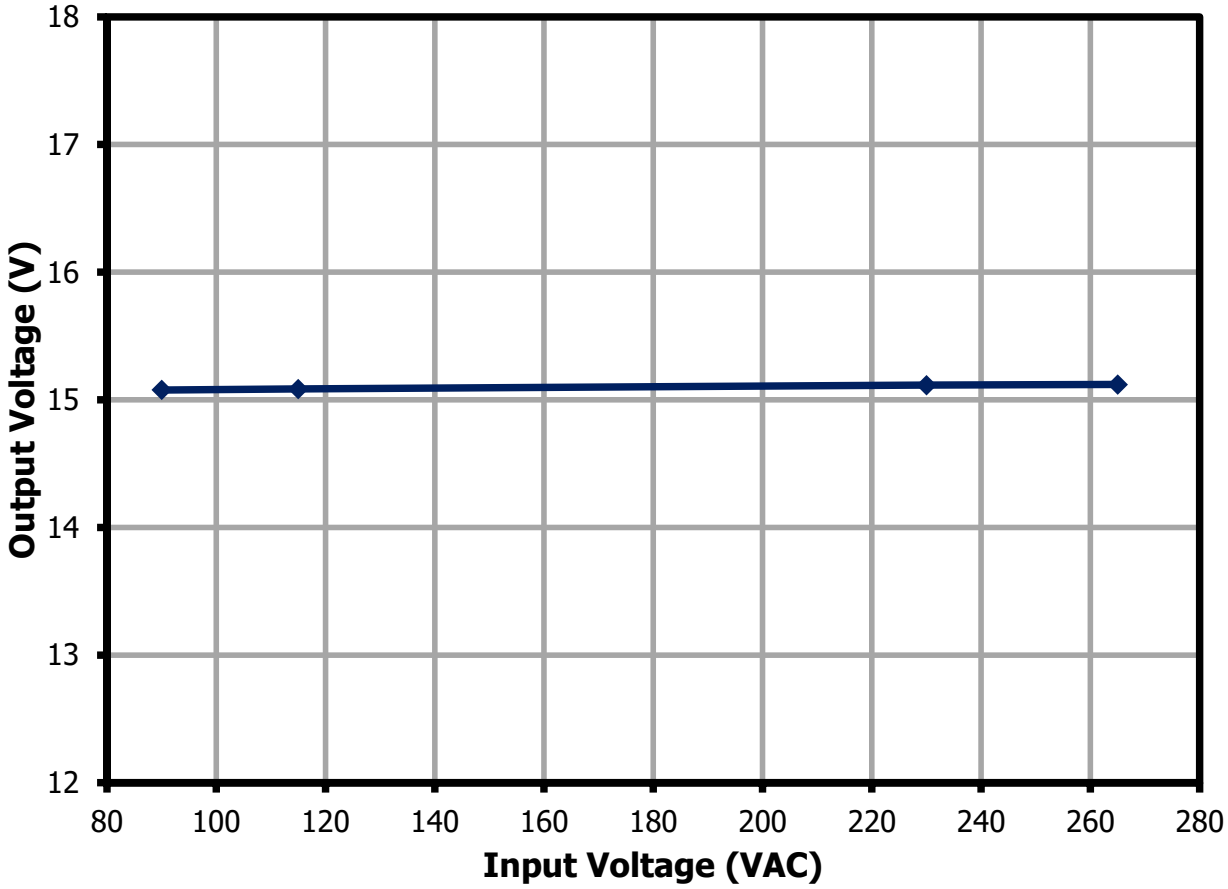


Figure 17 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

12.5.4 Output: 20 V / 3 A

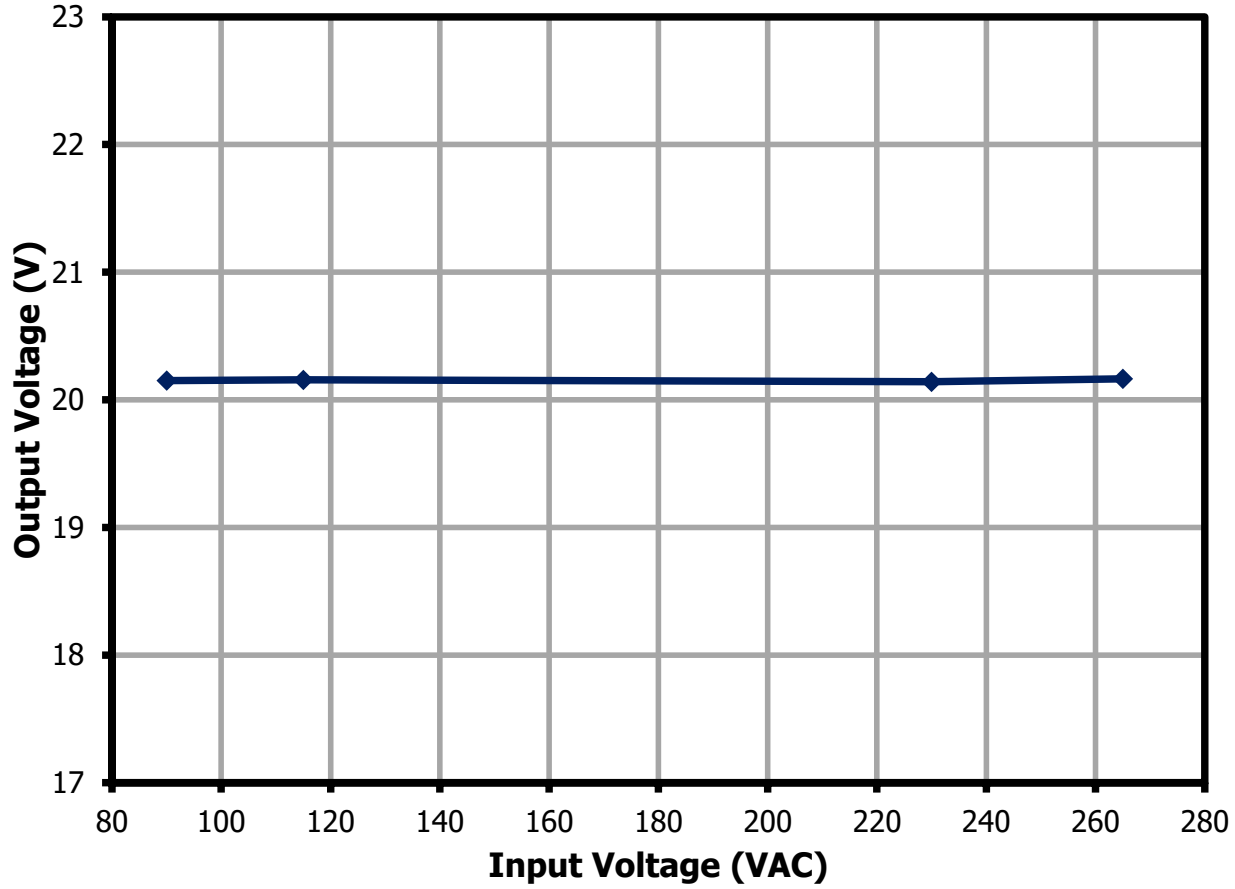


Figure 18 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

13 Thermal Performance

13.1 *Thermal Performance is Measured at Ambient Temperature*

Thermal performance is tested inside an acrylic box with natural convection

13.1.1 Output: 20 V / 3 A (90 VAC /265 VAC), Ambient Temperature: 25.4 °C

Component	Temperature (°C)	
	20 V / 3 A @ 90 VAC	**20 V / 3 A @ 265 VAC**
Bridge Rectifier, BR1	101.6	68.4
Bulk Capacitor, C4	90.7	75.7
Transformer, T1 - Core	92.7	88.6
Transformer, T1 - Winding	99.3	93
InnoSwitch4-CZ, U1	103.4	70.7
Clamp Zero, U3	89.1	86.7
SR FET, Q2	95	84.6
Secondary Rectifier Diode, D7	95.2	82.3
Secondary Snubber, R13	97.5	84.7
Output Capacitor, C14	80.8	71.1
Primary linear regulator transistor, Q1	100.7	89.4
Primary Clamp Diode, D1	89.8	81
MinE-CAP, U2	96.5	63.1

Figure 19 – Thermal Performance at 90 VAC / 265 VAC, Room Temperature.

14 Waveforms

Note: Measurements taken at room temperature

14.1 *Start-up Waveforms*

14.1.1 Output Voltage and Current

Note: Output voltages captured on the board at output connector

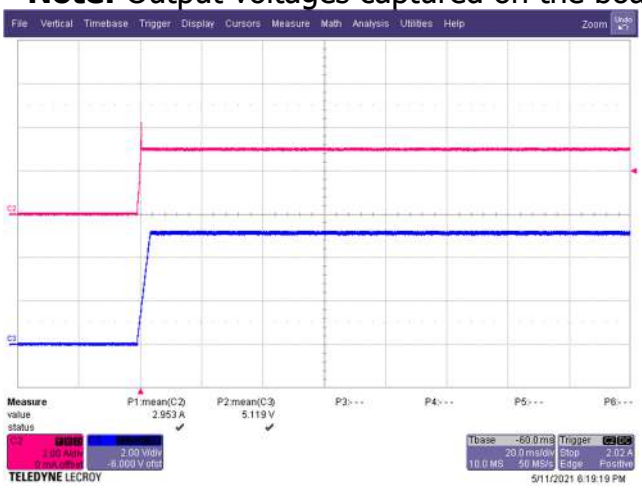


Figure 20 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load .
C2: I_{LOAD}, 2 A / div.
C3: V_{OUT}, 2 V / div.
Time: 20 ms / div.

Figure 21 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
C2: I_{LOAD}, 2 A / div.
C3: V_{OUT}, 2 V / div.
Time: 20 ms / div.

14.1.2 Primary Drain Voltage and Current

Figure 22 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (185 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 100 ms / div.

Figure 23 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (446 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 100 ms / div.

14.1.3 Primary Clamp Drain Voltage and Current

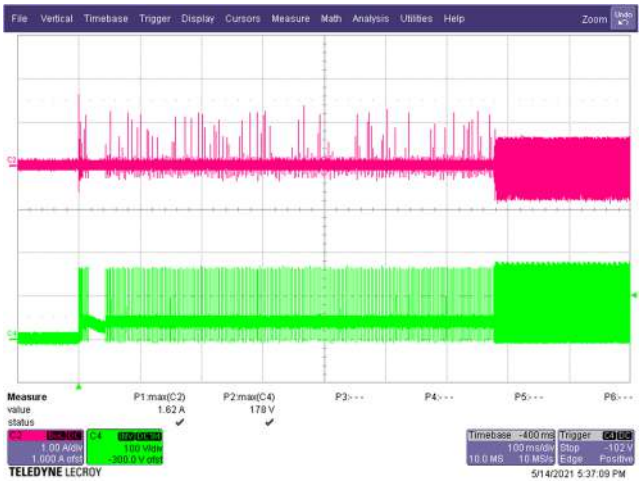


Figure 24 – Primary Clamp Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (178 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 100 ms / div.

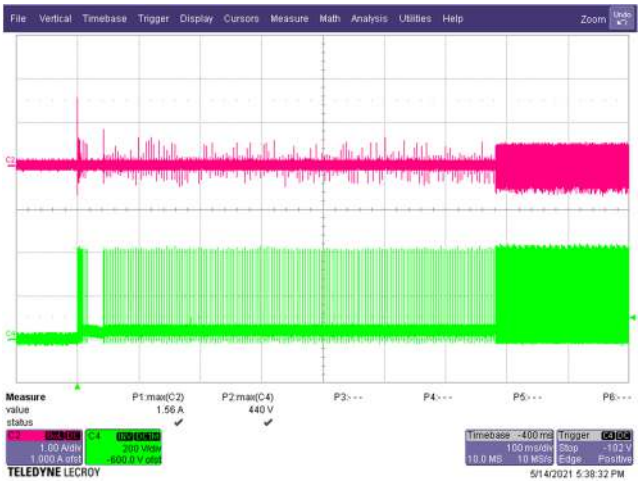


Figure 25 – Primary Clamp Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (440 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 100 ms / div.

14.1.4 SR FET Drain Voltage and Load Current

Figure 26 – SR FET Drain Voltage and Load Current.
90 VAC, 5.0 V, 3 A Load (33.1 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{Load}, 2 A / div.
Time: 100 ms / div.

Figure 27 – SR FET Drain Voltage and Load Current.
265 VAC, 5.0 V, 3 A Load (72.2 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{Load}, 2 A / div.
Time: 100 ms / div.

14.2 *Load Transient Response*

Note: Output voltage waveforms are captured at the end of the PC board

14.2.1 Output: 5 V / 3 A

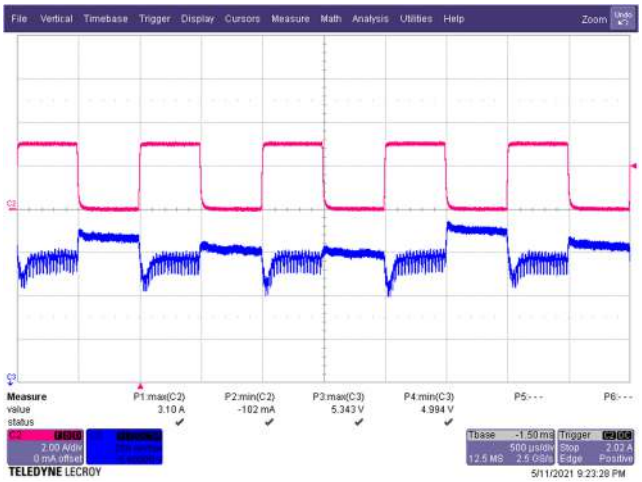


Figure 28 – Transient Response.
90 VAC, 5.0 V, 0 – 3 A Load Step.
V_{MIN}: 4.994 V, V_{MAX}: 5.343 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

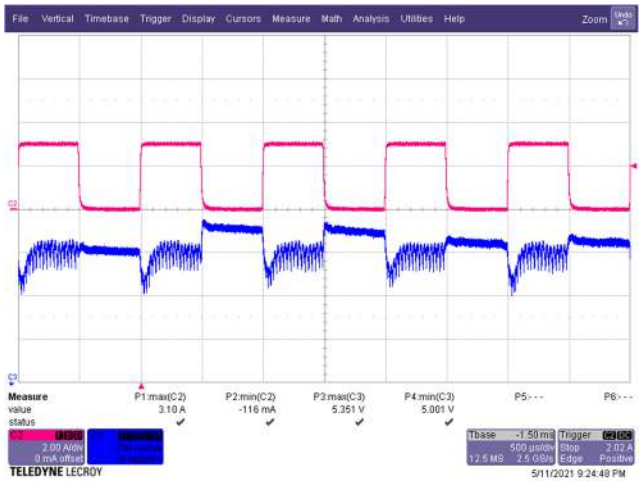


Figure 29 – Transient Response.
265 VAC, 5.0 V, 0 – 3 A Load Step.
V_{MIN}: 5.001 V, V_{MAX}: 5.351 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

14.2.2 Output: 9 V / 3 A

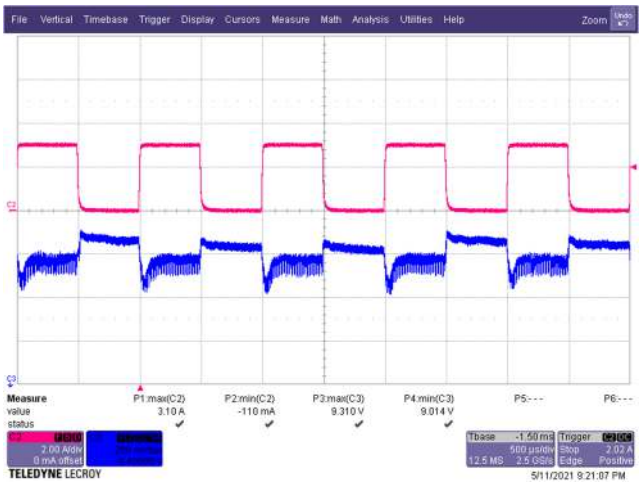


Figure 30 – Transient Response.
90 VAC, 9.0 V, 0 – 3 A Load Step.
V_{MIN}: 9.014 V, V_{MAX}: 9.310 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

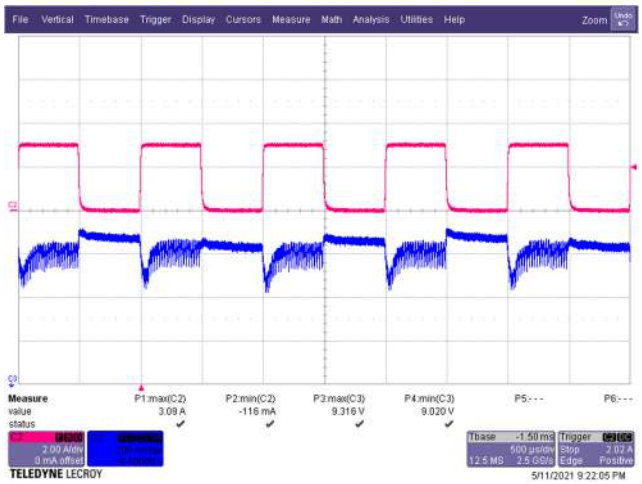


Figure 31 – Transient Response.
265 VAC, 9.0 V, 0 – 3 A Load Step.
V_{MIN}: 9.020 V, V_{MAX}: 9.316 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

14.2.3 Output: 15 V / 3 A

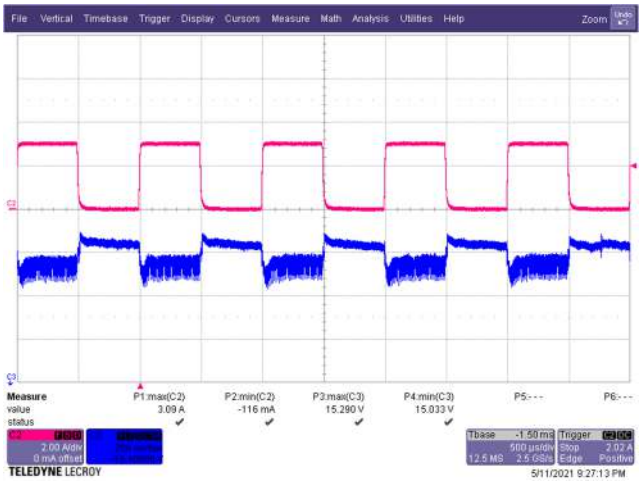


Figure 32 – Transient Response.
90 VAC, 15.0 V, 0 – 3 A Load Step.
V_{MIN}: 15.033 V, V_{MAX}: 15.29 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

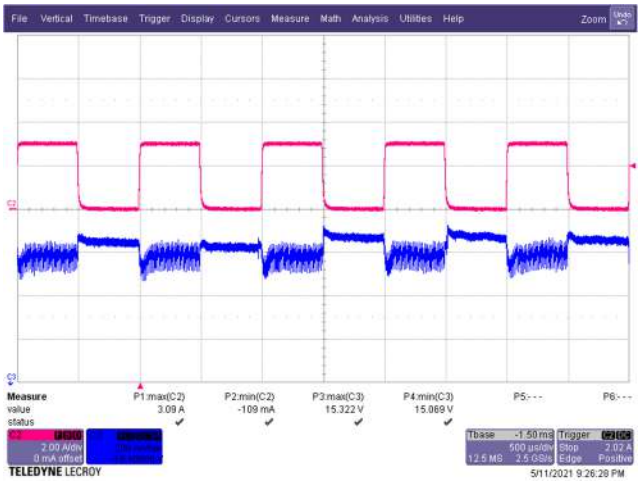


Figure 33 – Transient Response.
265 VAC, 15.0 V, 0 – 3 A Load Step.
V_{MIN}: 15.069 V, V_{MAX}: 15.322 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

14.2.4 Output: 20 V / 3 A

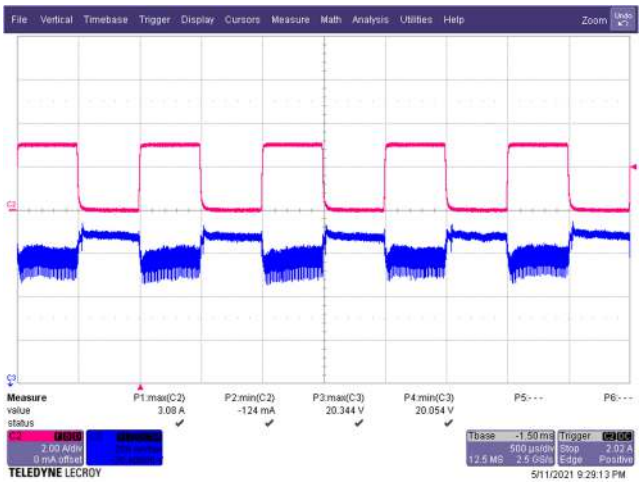


Figure 34 – Transient Response.
90 VAC, 20.0 V, 0 – 3 A Load Step.
V_{MIN}: 20.054 V, V_{MAX}: 20.344 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

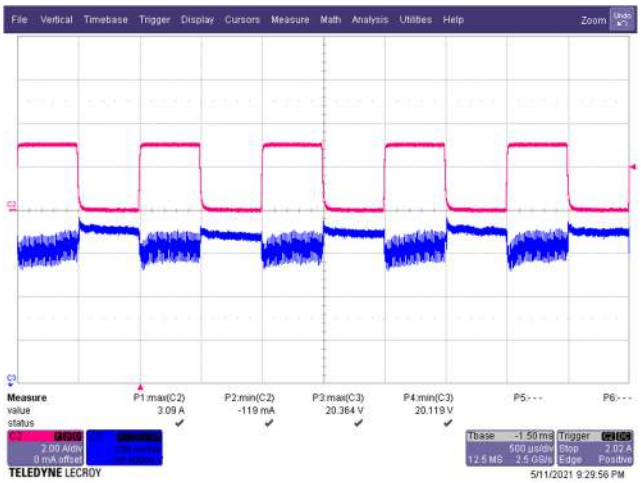


Figure 35 – Transient Response.
265 VAC, 20.0 V, 0 – 3 A Load Step.
V_{MIN}: 20.119 V, V_{MAX}: 20.364 V.
C3: V_{OUT}, 0.2 V / div.
C2: I_{LOAD}, 2 A / div.
Time: 0.5 ms / div.

14.3 *Primary Drain Voltage and Current (Steady-State)*

14.3.1 Output: 5 V / 3 A

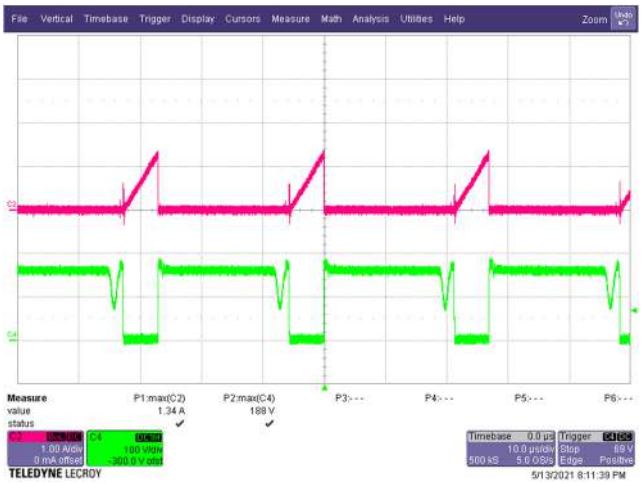


Figure 36 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (188 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

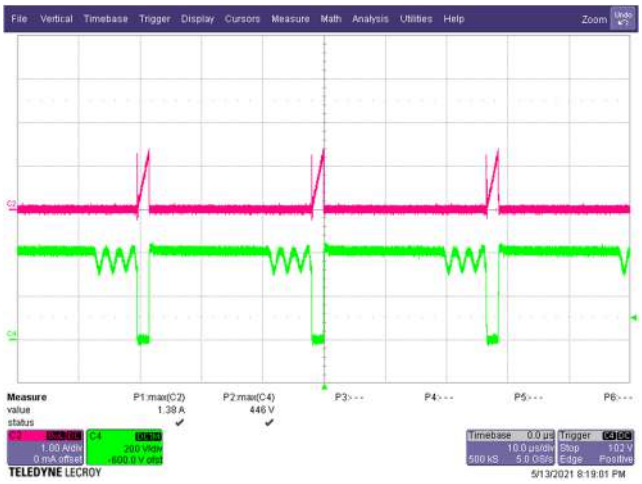


Figure 37 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (446 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

14.3.2 Output: 9 V / 3 A

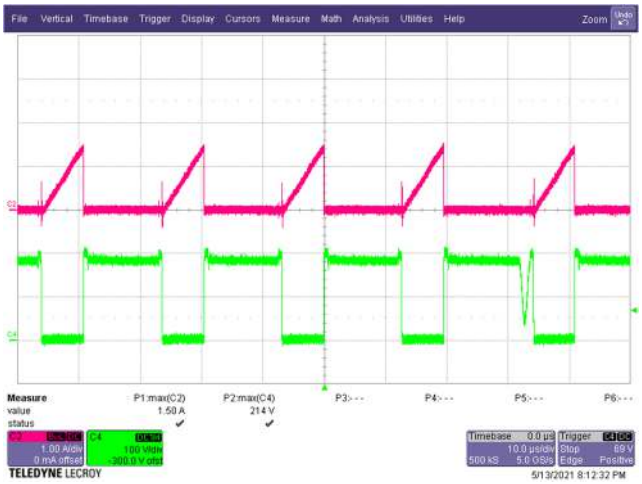


Figure 38 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load (214 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

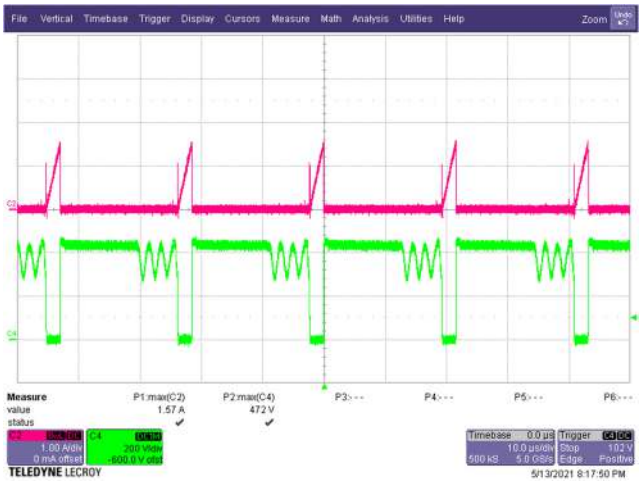


Figure 39 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load (472 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

14.3.3 Output: 15 V / 3 A

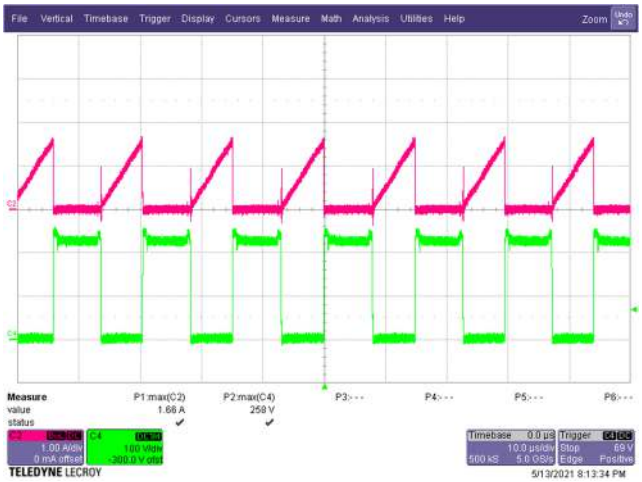


Figure 40 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load (258 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

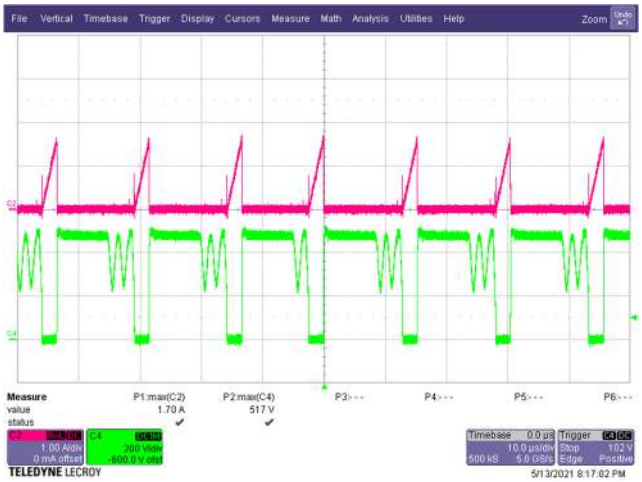


Figure 41 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load (517 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

14.3.4 Output: 20 V / 3 A

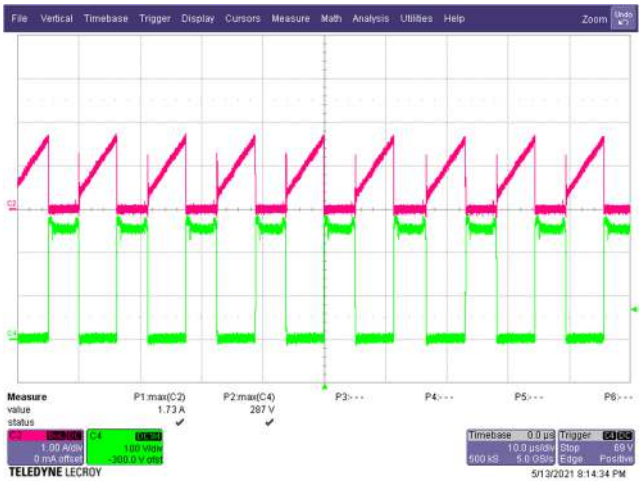


Figure 42 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load (287 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

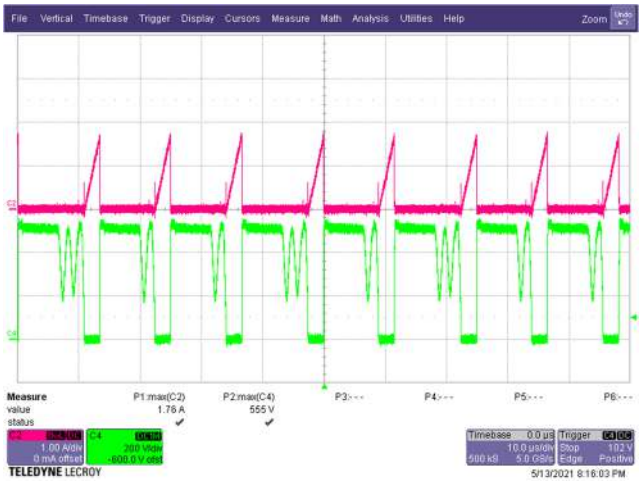


Figure 43 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 3 A Load (555 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 µs / div.

14.4 *Primary Clamp Drain Voltage and Current (Steady-State)*

14.4.1 Output: 5 V / 3 A

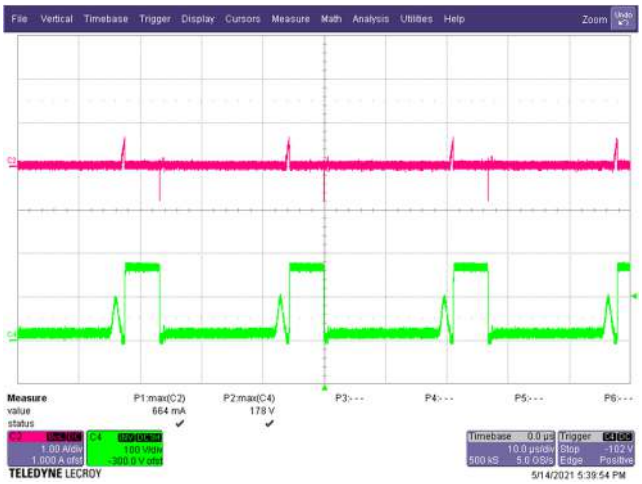


Figure 44 – Primary Clamp Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (178 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

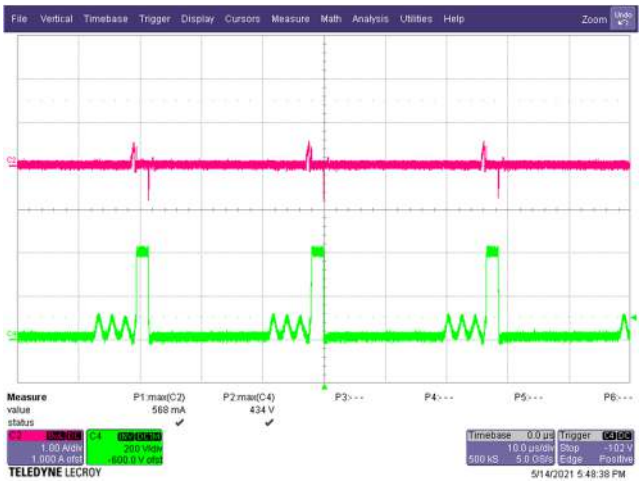


Figure 45 – Primary Clamp Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (434 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

14.4.2 Output: 9 V / 3 A

Figure 46 – Primary Clamp Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load (210 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

Figure 47 – Primary Clamp Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load (459 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

14.4.3 Output: 15 V / 3 A

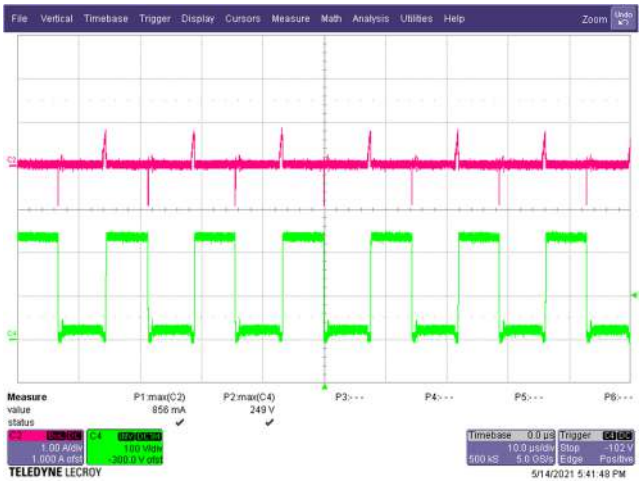


Figure 48 – Primary Clamp Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load (249 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

Figure 49 – Primary Clamp Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load (491 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

14.4.4 Output: 20 V / 3 A

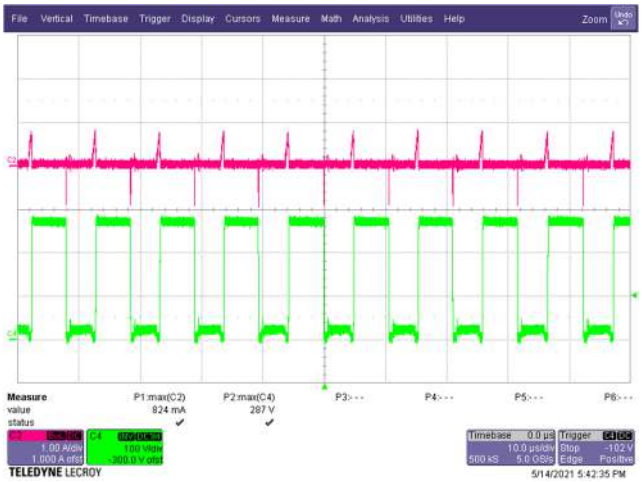


Figure 50 – Primary Clamp Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load (287 V_{MAX}).
C4: V_{DRAIN}, 100 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

Figure 51 – Primary Clamp Drain Voltage and Current.
265 VAC, 20.0 V, 3 A Load (536 V_{MAX}).
C4: V_{DRAIN}, 200 V / div.
C2: I_{DRAIN}, 1 A / div.
Time: 10 μs / div.

14.5 *SR FET Drain Voltage and Load Current (Steady-State)*

14.5.1 Output: 5 V / 3 A

Figure 52 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (33.5 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

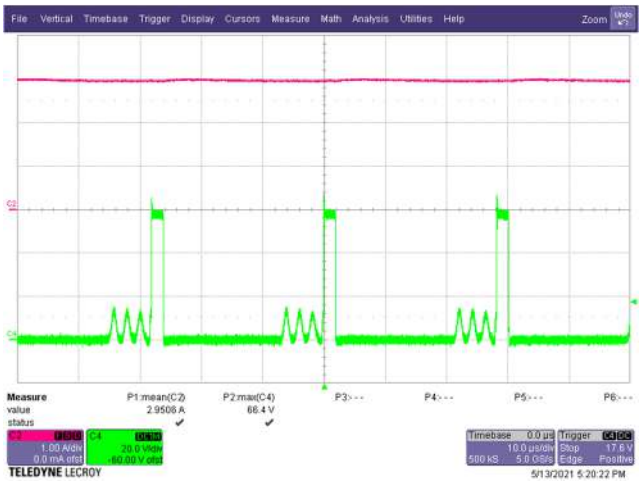


Figure 53 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (66.4 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

14.5.2 Output: 9 V / 3 A

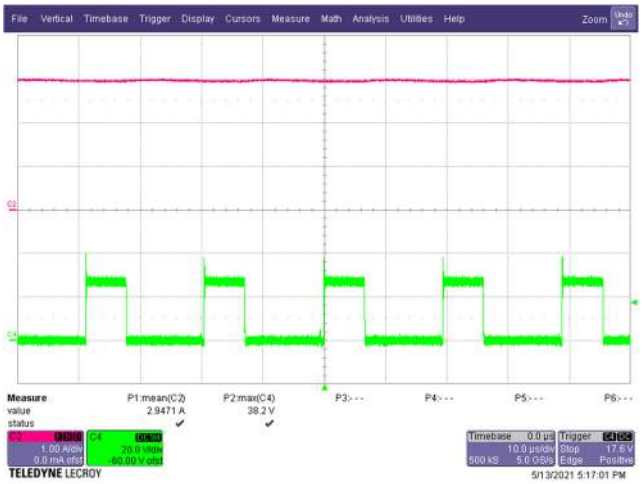


Figure 54 – SR FET Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load (38.2 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

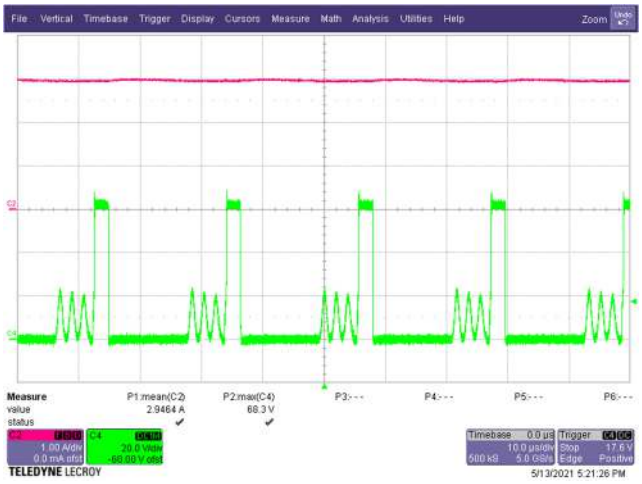


Figure 55 – SR FET Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load (68.3 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

14.5.3 Output: 15 V / 3 A

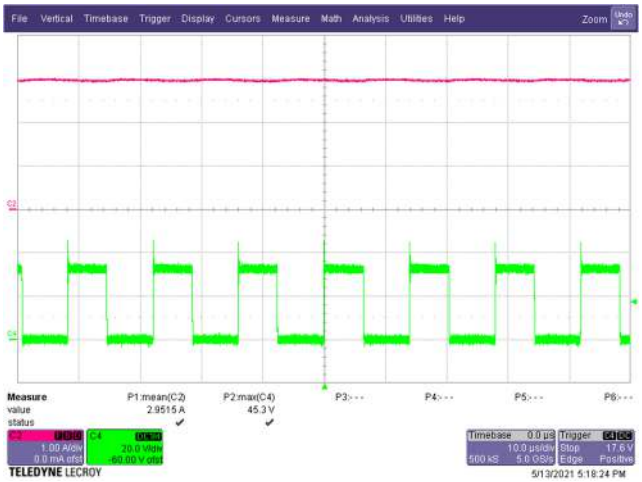


Figure 56 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load (45.3 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

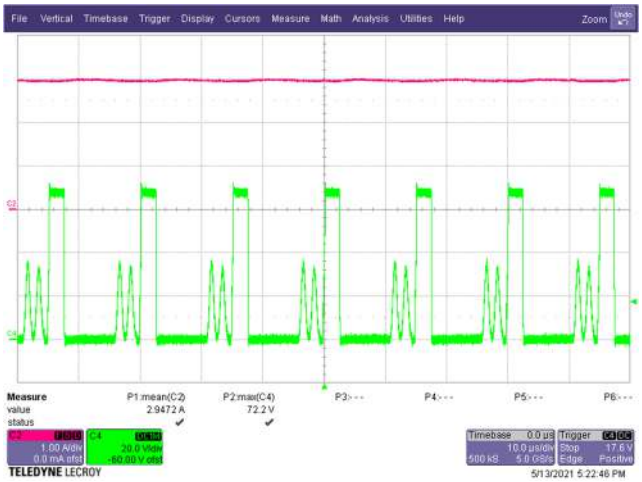


Figure 57 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load (72.2 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

14.5.4 Output: 20 V / 3 A

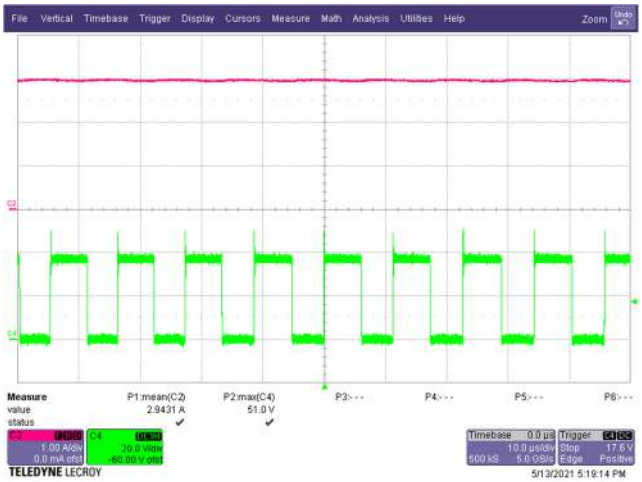


Figure 58 – SR FET Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load (51 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

Figure 59 – SR FET Drain Voltage and Current.
85 VAC, 20.0 V, 3 A Load (77.3 V_{MAX}).
C4: $V_{DRAIN(SR)}$, 20 V / div.
C2: I_{LOAD}, 1 A / div.
Time: 10 µs / div.

15 Output Ripple Measurements

15.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

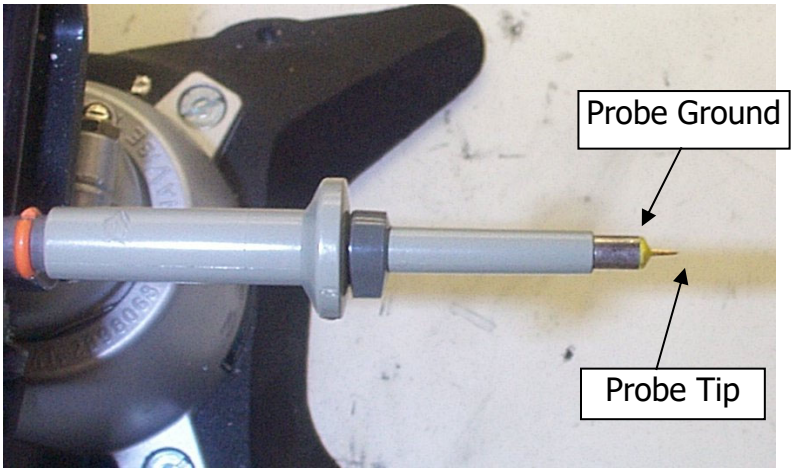


Figure 60 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

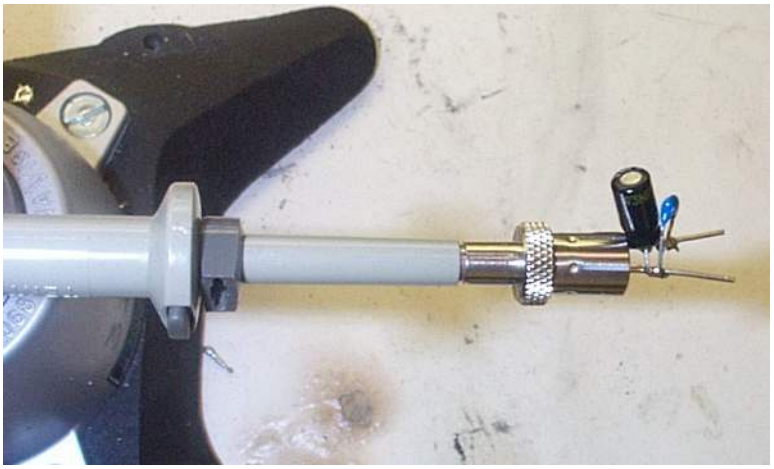


Figure 61 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added).

15.2 *Output Voltage Ripple Waveforms*

Note 1: Output voltage ripple waveforms are captured at the end of the PC board
2: Measurements taken at room temperature (approximately 24 °C)

15.2.1 Output: 5 V / 3 A

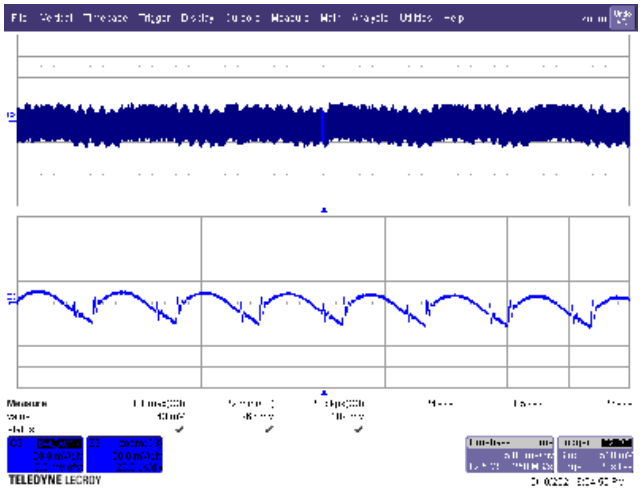


Figure 62 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load (109 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

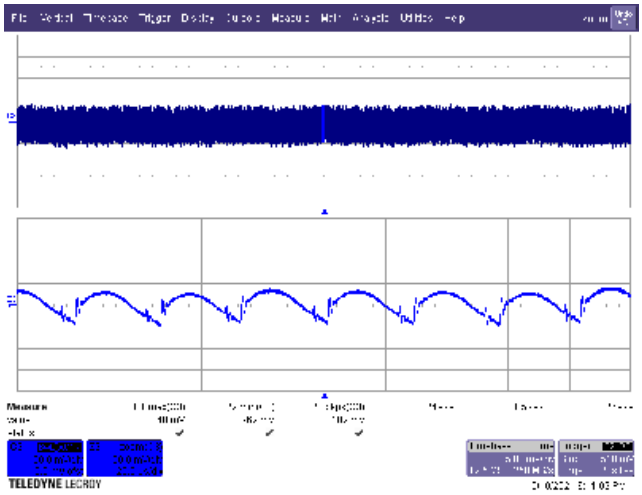


Figure 63 – Output Voltage Ripple.
115 VAC, 5.0 V, 3 A Load (102 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

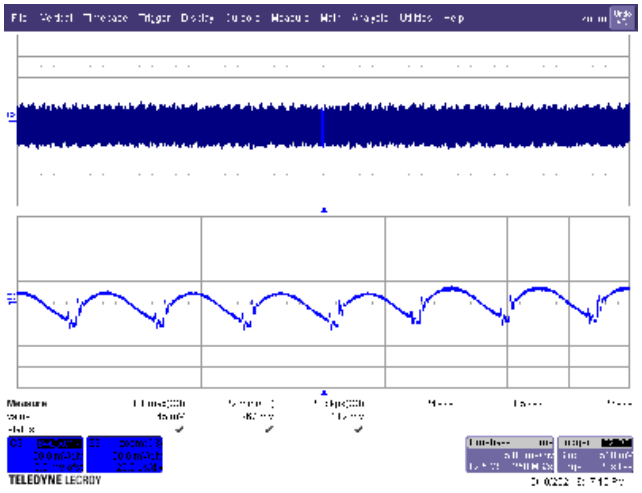


Figure 64 – Output Voltage Ripple.
230 VAC, 5.0 V, 3 A Load (112 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

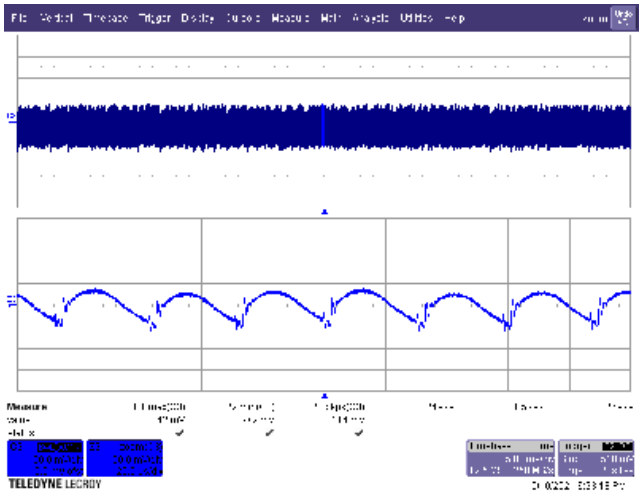


Figure 65 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load (114 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

15.2.2 Output: 9 V / 3 A

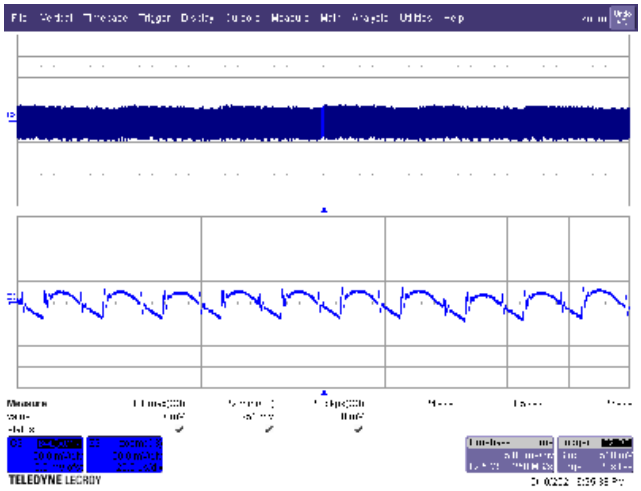


Figure 66 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load (88 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

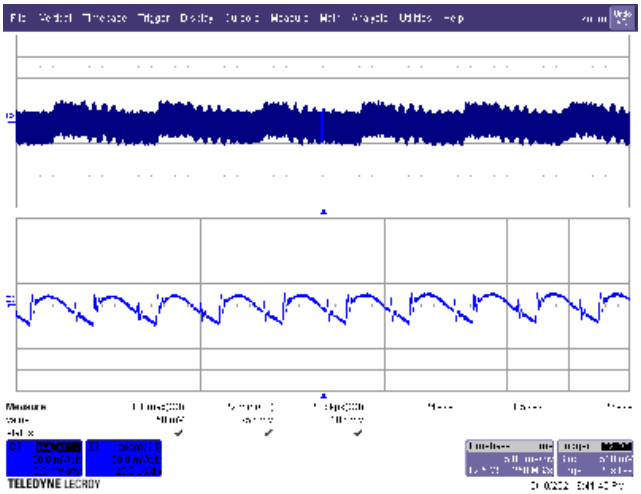


Figure 67 – Output Voltage Ripple.
115 VAC, 9.0 V, 3 A Load (106 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

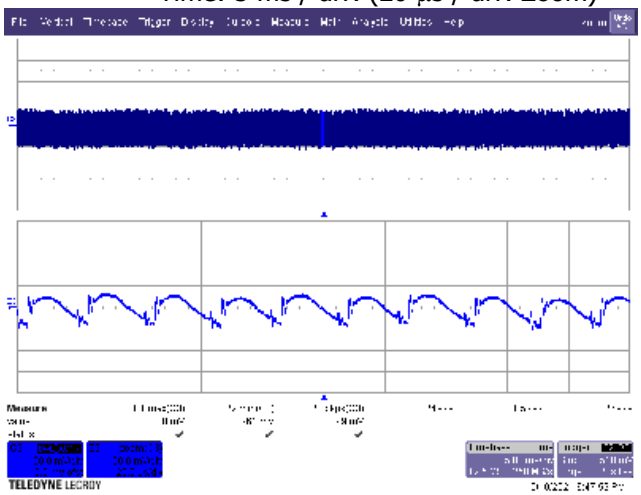


Figure 68 – Output Voltage Ripple.
230 VAC, 9.0 V, 3 A Load (99 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

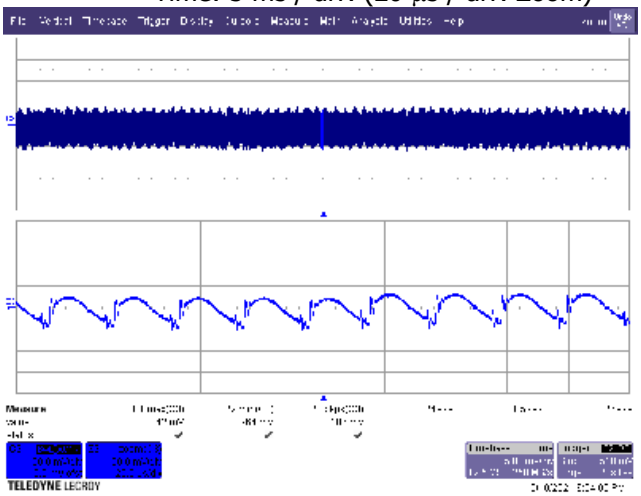


Figure 69 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load (106 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

15.2.3 Output: 15 V / 3 A

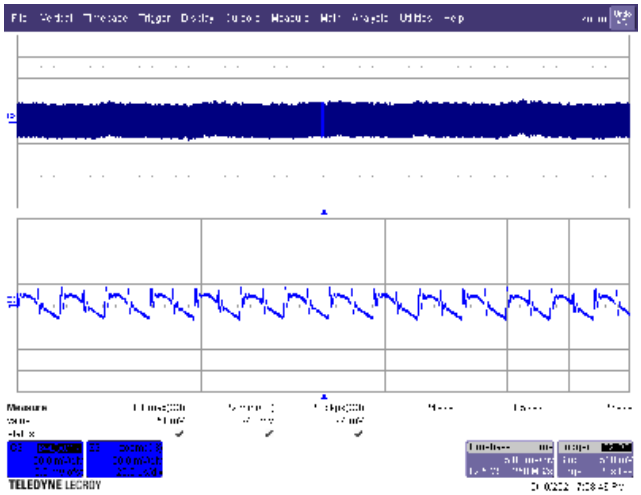


Figure 70 – Output Voltage Ripple.
90 VAC, 15.0 V, 3 A Load (94 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

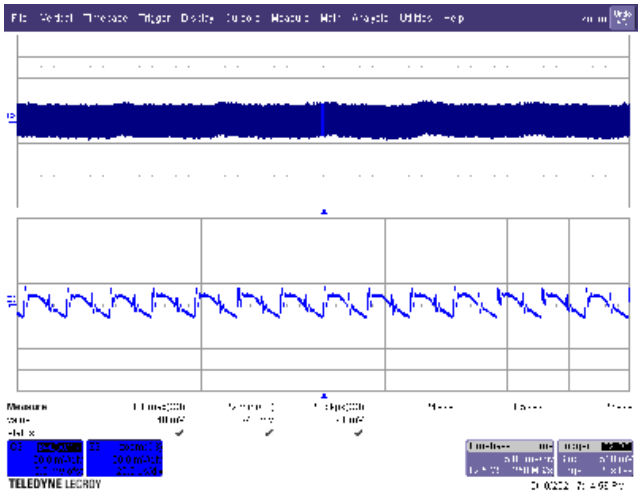


Figure 71 – Output Voltage Ripple.
115 VAC, 15.0 V, 3 A Load (91 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

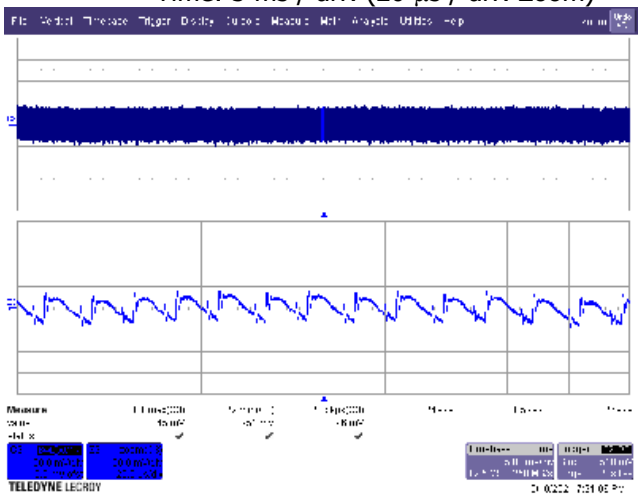


Figure 72 – Output Voltage Ripple.
230 VAC, 15.0 V, 3 A Load (96 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

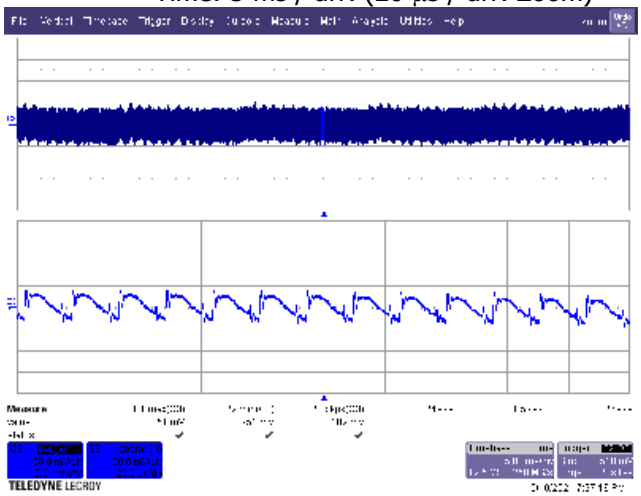


Figure 73 – Output Voltage Ripple.
265 VAC, 15.0 V, 3 A Load (102 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 μs / div. Zoom)

15.2.4 Output: 20 V / 3 A

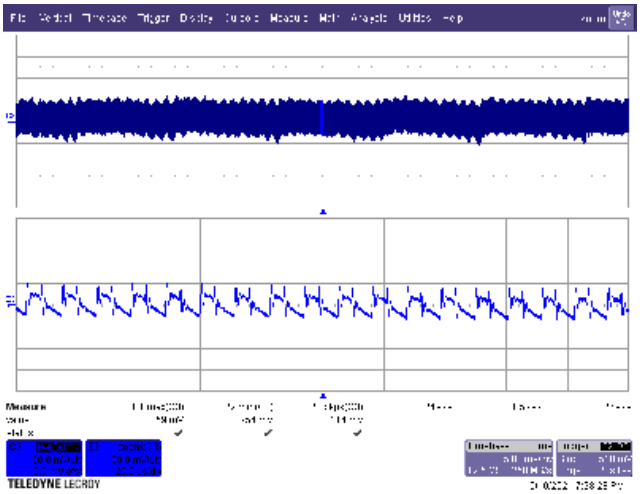


Figure 74 – Output Voltage Ripple.
90 VAC, 20.0 V, 3 A Load (114 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

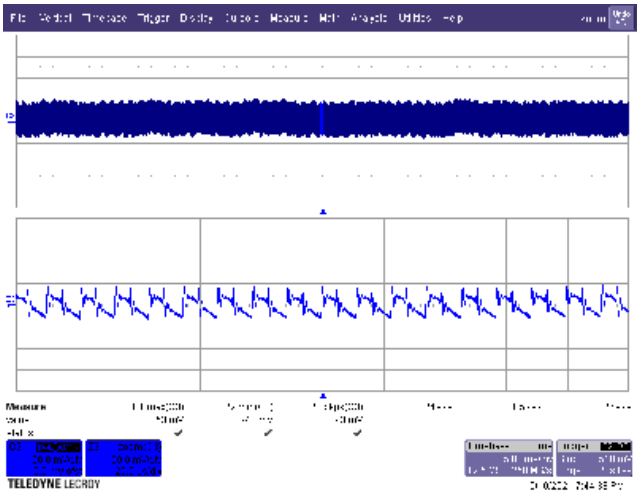


Figure 75 – Output Voltage Ripple.
115 VAC, 20.0 V, 3 A Load (123 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 100 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

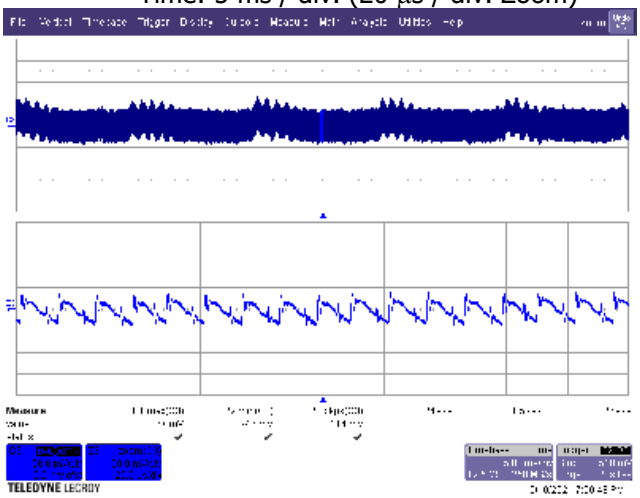


Figure 76 – Output Voltage Ripple.
230 VAC, 20.0 V, 3 A Load (114 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

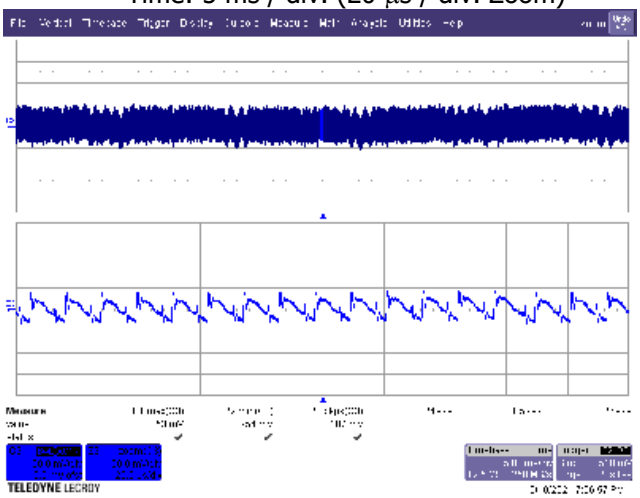


Figure 77 – Output Voltage Ripple.
265 VAC, 20.0 V, 3 A Load (107 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (20 µs / div. Zoom)

15.2.5 Output: 5 V / 0 A

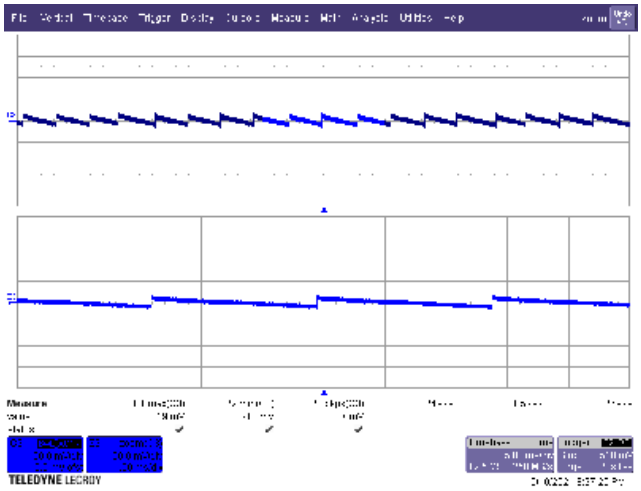


Figure 78 – Output Voltage Ripple.
90 VAC, 5.0 V, 0 A Load (37mV$_{PK-PK}$).
C3: V$_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

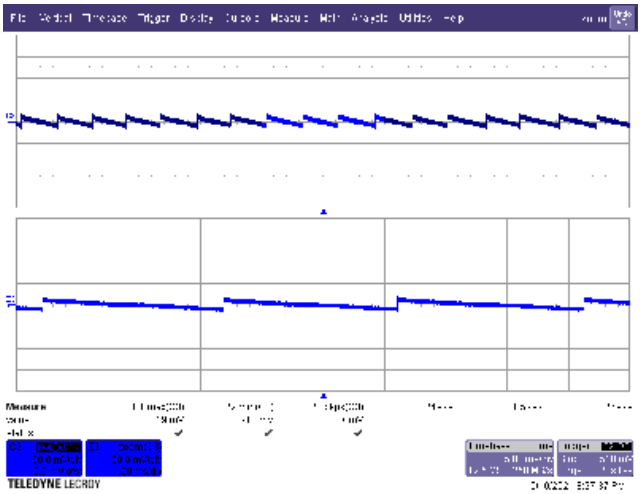


Figure 79 – Output Voltage Ripple.
115 VAC, 5.0 V, 0 A Load (37 mV$_{PK-PK}$).
C3: V$_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

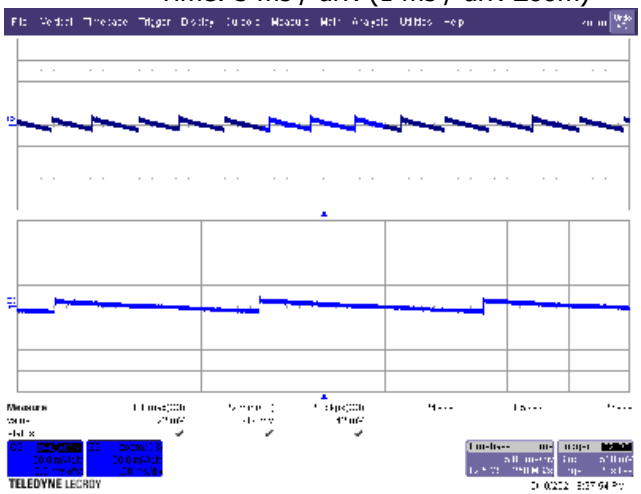


Figure 80 – Output Voltage Ripple.
230 VAC, 5.0 V, 0 A Load (42 mV$_{PK-PK}$).
C3: V$_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

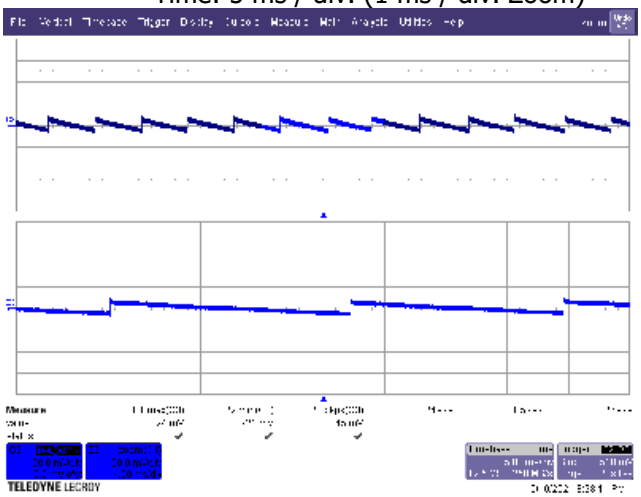


Figure 81 – Output Voltage Ripple.
265 VAC, 5.0 V, 0 A Load (45 mV$_{PK-PK}$).
C3: V$_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

15.2.6 Output: 9 V / 0 A

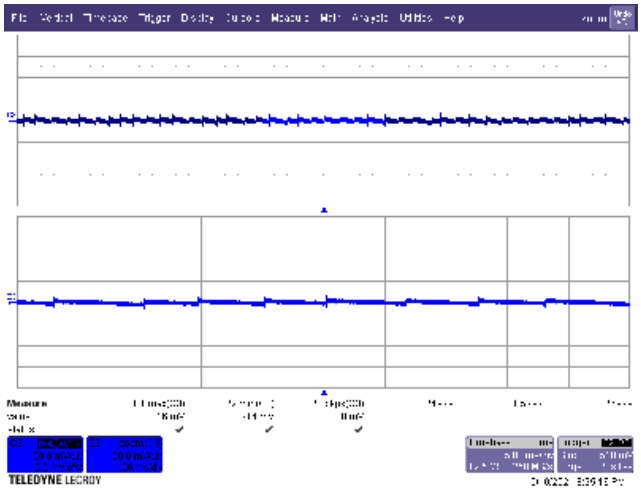


Figure 82 – Output Voltage Ripple.
90 VAC, 9.0 V, 0 A Load (30 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

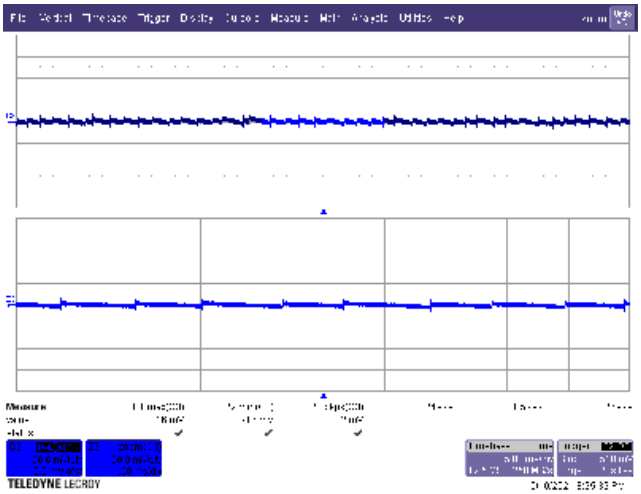


Figure 83 – Output Voltage Ripple.
115 VAC, 9.0 V, 0 A Load (32 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

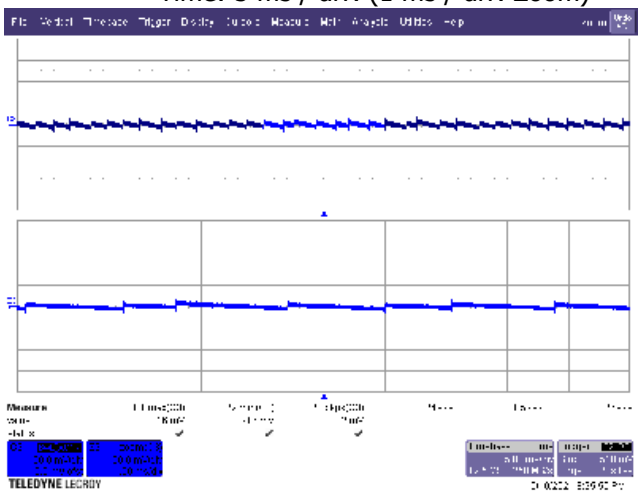


Figure 84 – Output Voltage Ripple.
230 VAC, 9.0 V, 0 A Load (32 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

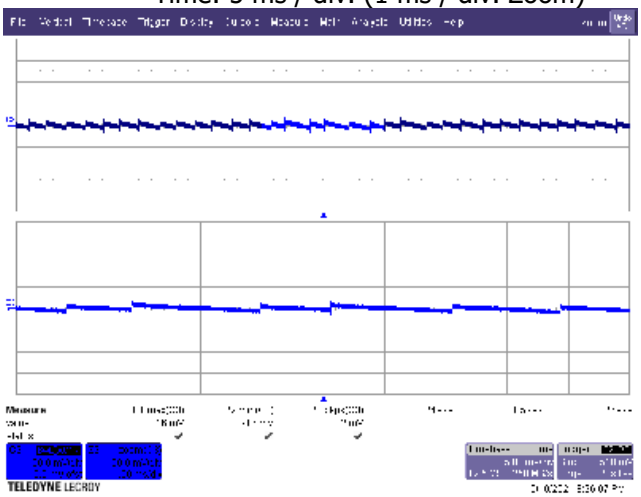


Figure 85 – Output Voltage Ripple.
265 VAC, 9.0 V, 0 A Load (32 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

15.2.7 Output: 15 V / 0 A

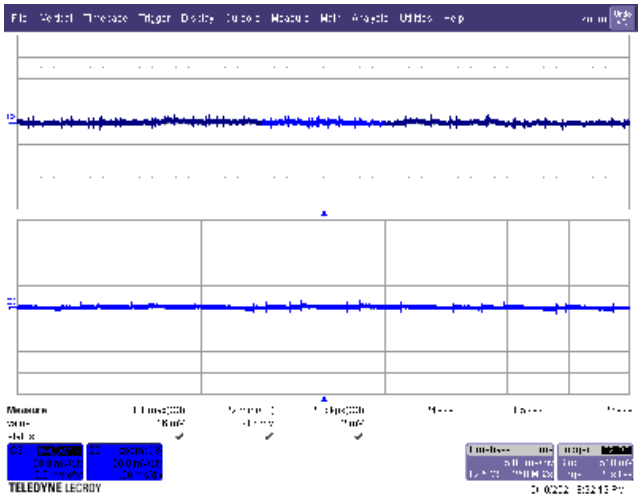


Figure 86 – Output Voltage Ripple.
90 VAC, 15.0 V, 0 A Load (32 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

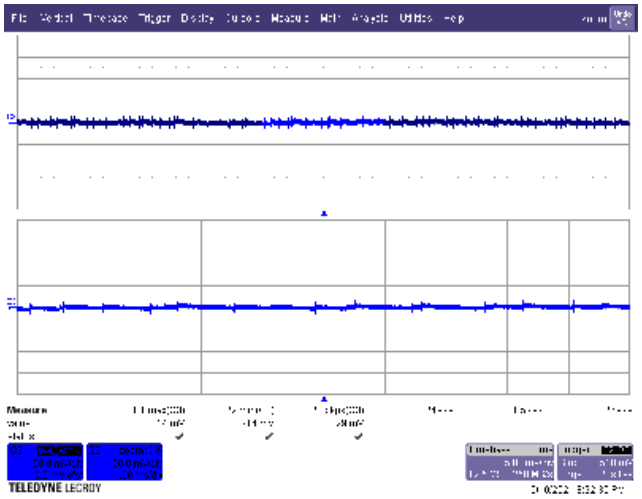


Figure 87 – Output Voltage Ripple.
115 VAC, 15.0 V, 0 A Load (29 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

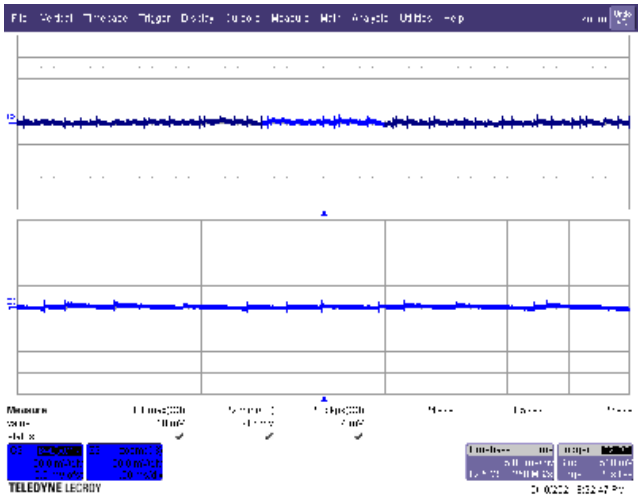


Figure 88 – Output Voltage Ripple.
230 VAC, 15.0 V, 0 A Load (34 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

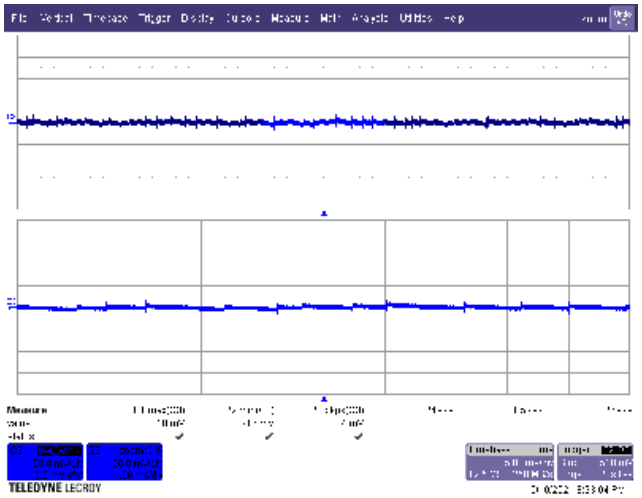


Figure 89 – Output Voltage Ripple.
265 VAC, 15.0 V, 0 A Load (34 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

15.2.8 Output: 20 V / 0 A

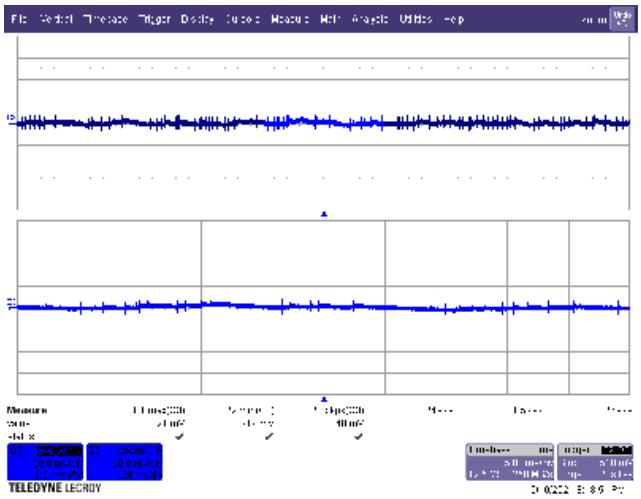


Figure 90 – Output Voltage Ripple.
90 VAC, 20.0 V, 0A Load (40 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

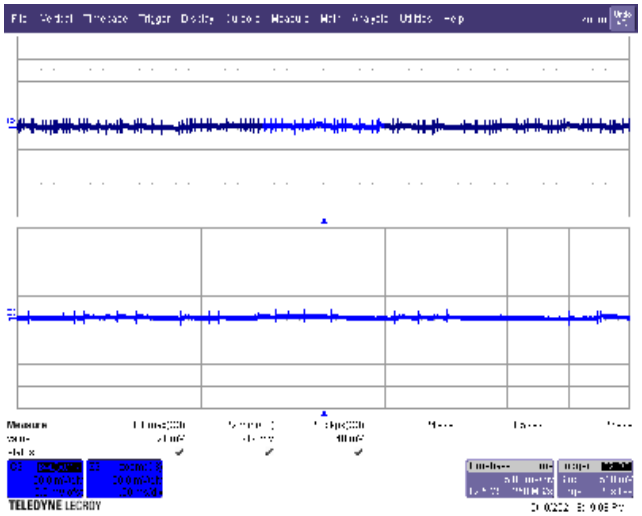


Figure 91 – Output Voltage Ripple.
115 VAC, 20.0 V, 0 A Load (40 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

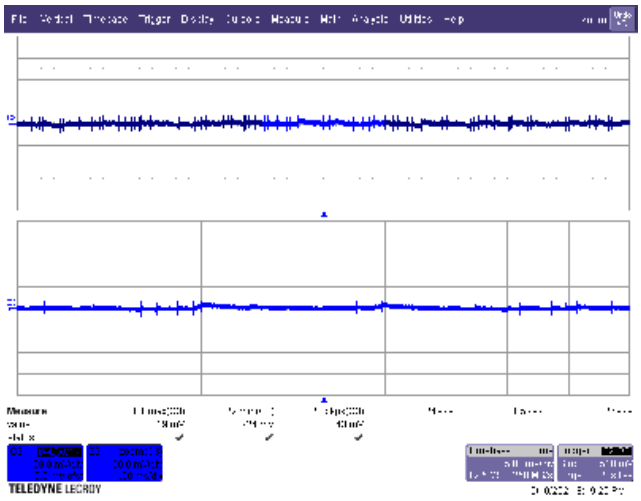


Figure 92 – Output Voltage Ripple.|
230 VAC, 20.0 V, 0 A Load (43 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

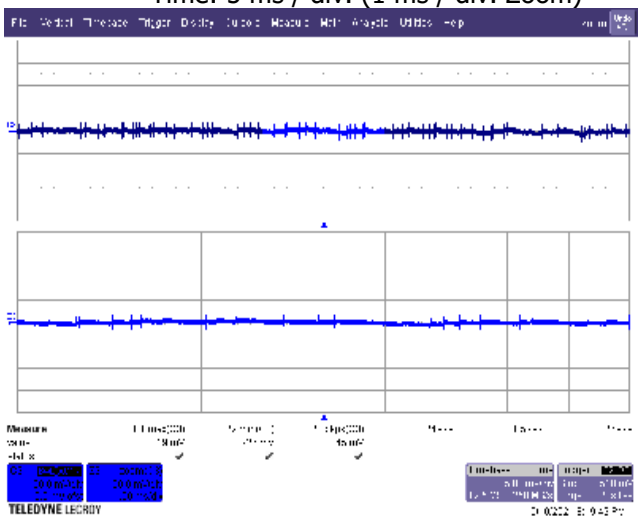
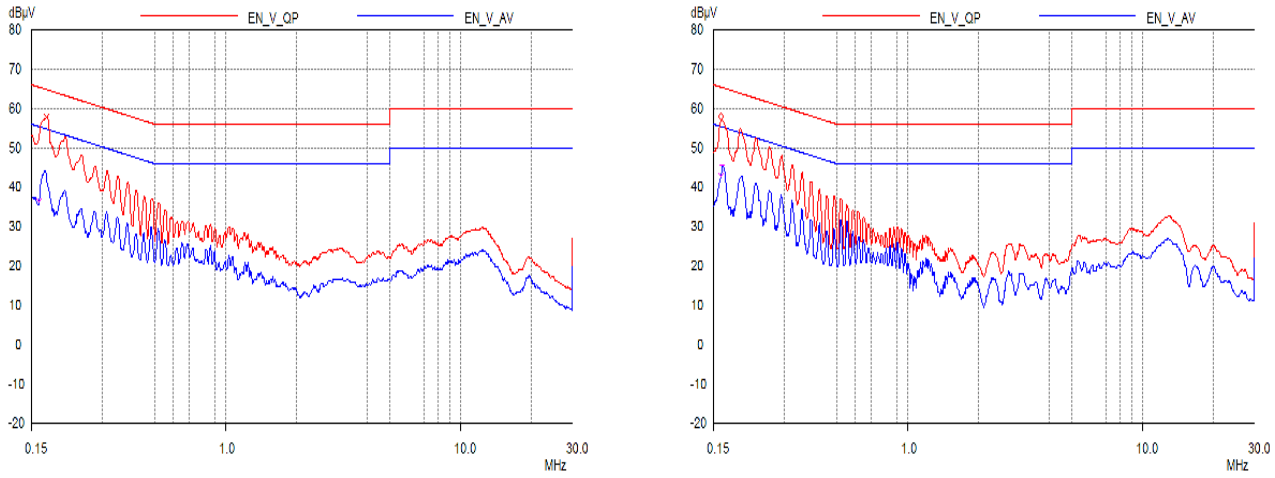


Figure 93 – Output Voltage Ripple.
265 VAC, 20.0 V, 0 A Load (45 mV_{PK-PK}).
C3: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (1 ms / div. Zoom)

16 Conducted EMI (QPK / AV)

16.1 *Line*

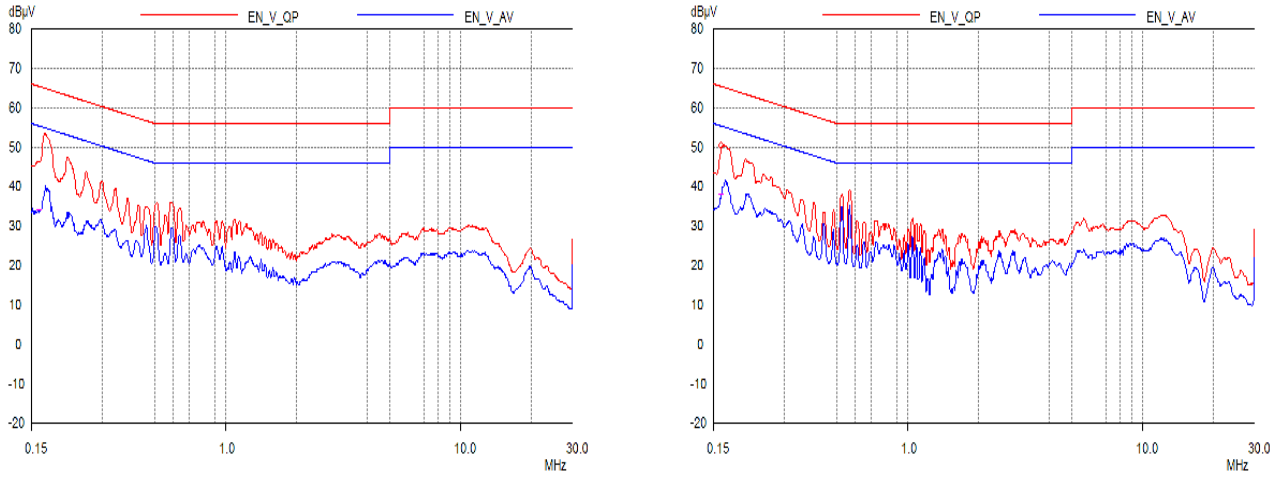
16.1.1 Output: 5 V / 3 A



115 VAC. 230 VAC.

Figure 94 – Floating Ground EMI, 5 V / 3 A Load.

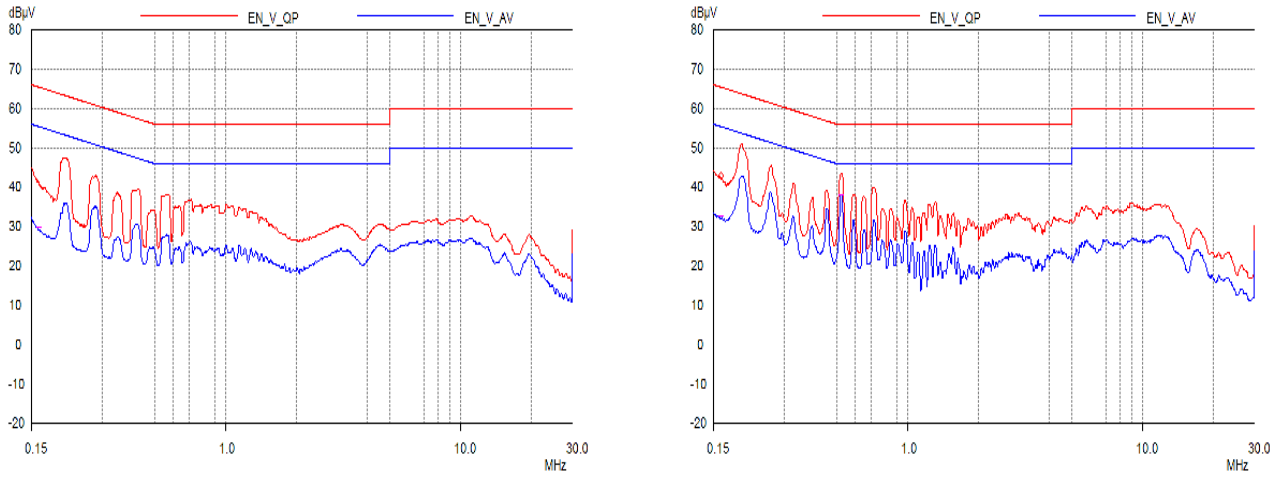
16.1.2 Output: 9 V / 3 A



115 VAC. 230 VAC.

Figure 95 – Floating Ground EMI, 9 V / 3 A Load.

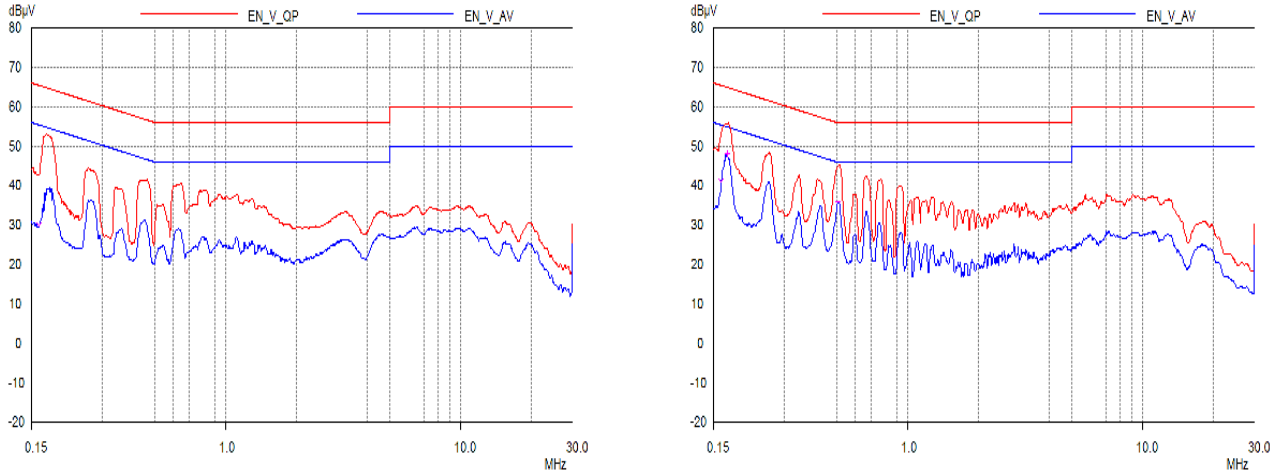
16.1.3 Output: 15 V / 3 A



115 VAC. 230 VAC.

Figure 96 – Floating Ground EMI, 15 V / 3 A Load.

16.1.4 Output: 20 V / 3 A

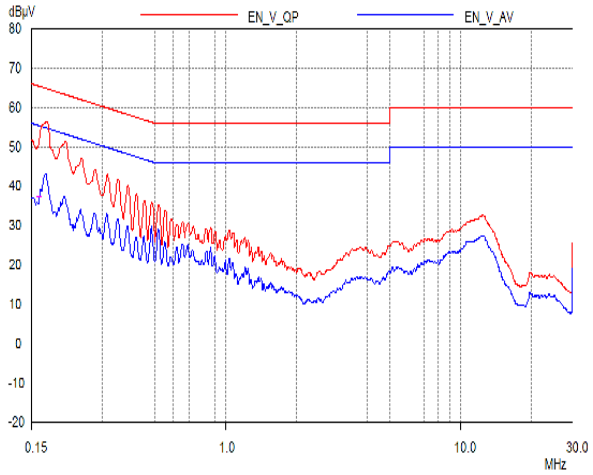


115 VAC. 230 VAC.

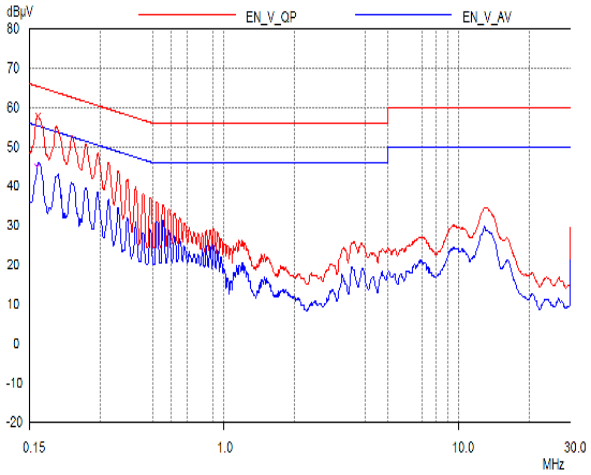
Figure 97 – Floating Ground EMI, 20 V / 3 A Load.

16.2 *Neutral*

16.2.1 Output: 5 V / 3 A



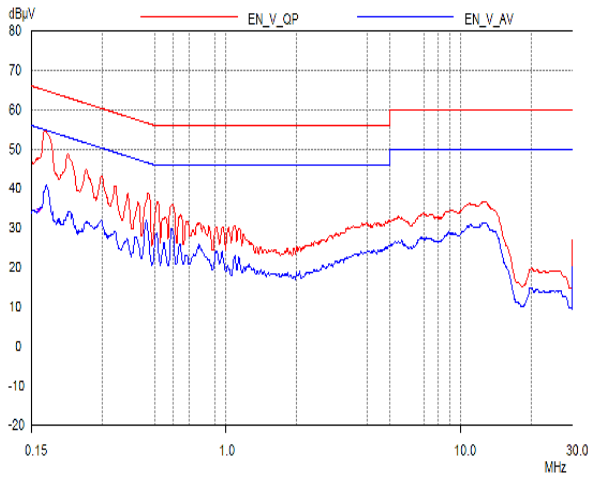
115 VAC.



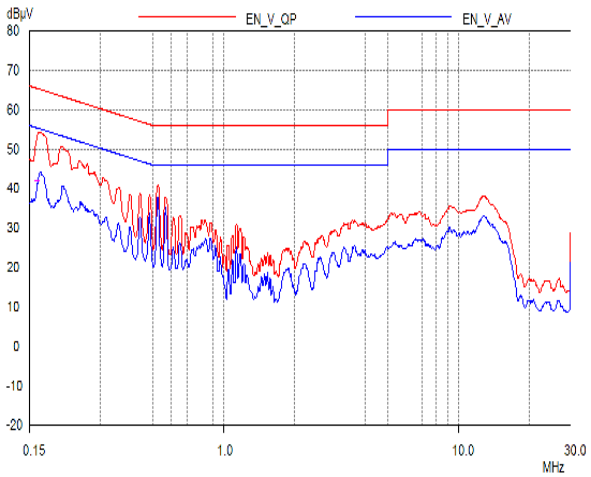
230 VAC.

Figure 98 – Floating Ground EMI, 5 V / 3 A Load.

16.2.2 Output: 9 V / 3 A



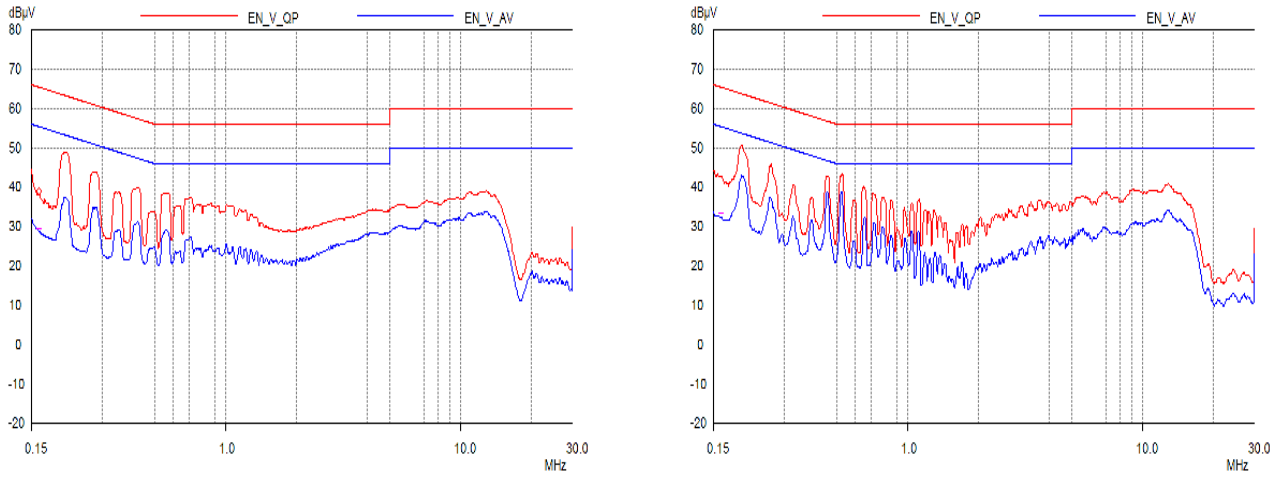
115 VAC.



230 VAC.

Figure 99 – Floating Ground EMI, 9 V / 3 A Load.

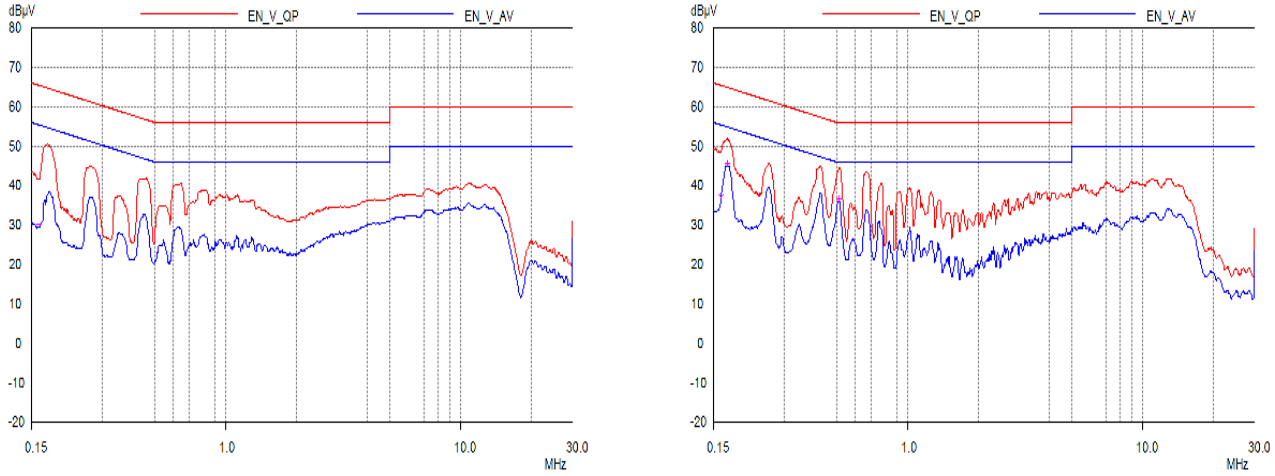
16.2.3 Output: 15 V / 3 A



115 VAC. 230 VAC.

Figure 100 – Floating Ground EMI, 15 V / 3 A Load.

16.2.4 Output: 20 V / 3 A



115 VAC. 230 VAC.

Figure 101 – Floating Ground EMI, 20 V / 3 A Load.

17 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

17.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 3 A (Pass/Fail)
+1000	L1 to L2	0	Pass
-1000	L1 to L2	0	Pass
+1000	L1 to L2	90	Pass*
-1000	L1 to L2	90	Pass*
+1000	L1 to L2	180	Pass
-1000	L1 to L2	180	Pass
+1000	L1 to L2	270	Pass*
-1000	L1 to L2	270	Pass*

17.2 *Common Mode Surge (L1 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass	Pass*
-2000	L1 to PE	90	Pass	Pass
+2000	L1 to PE	180	Pass	Pass
-2000	L1 to PE	180	Pass	Pass
+2000	L1 to PE	270	Pass	Pass
-2000	L1 to PE	270	Pass	Pass*

17.3 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass	Pass
-2000	L2 to PE	90	Pass	Pass*
+2000	L2 to PE	180	Pass	Pass
-2000	L2 to PE	180	Pass	Pass
+2000	L2 to PE	270	Pass	Pass*
-2000	L2 to PE	270	Pass	Pass

17.4 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	180	Pass	Pass
-2000	L1, L2 to PE	180	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

Pass* - Unit was restarting during some strikes due to line overvoltage protection.

18 Electrostatic Discharge

The unit was tested at the USB Type-C connector with ±16.5 kV air discharge and ±8.8 kV contact discharge at the positive and negative nodes of the output with 10 strikes for each condition.

A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

18.1 *Contact Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location On Board	Test Result 20 V / 3 A
+8.8	GND	Pass
-8.8	GND	Pass

18.2 *Air Discharge, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 20 V / 3 A
+16.5	GND	Pass
-16.5	GND	Pass

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
11-Oct-21	Km	1.3	Converted to RDR	Apps & Mktg

For the latest updates, visit our website: www.power.com

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