HV2605/HV2705

16-Channel Low Harmonic Distortion High-Voltage Analog Switches

Features

- 16-channel High-voltage Analog Switch
- Low Harmonic Distortion
- Integrated Bleed Resistors on the Outputs for HV2705
- 3.3V Input Logic Level Compatible
- –60 dB typical OFF-isolation at 5 MHz
- 20 MHz Data Shift Clock Frequency
- 10 µA Low-quiescent Power Dissipation
- Low Parasitic Capacitance
- DC to 50 MHz Small-signal Frequency Response
- CMOS logic Circuitry for Low Power
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltages

Applications

- Medical Ultrasound Imaging
- Non-destructive Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Optical MEMS Modules

Description

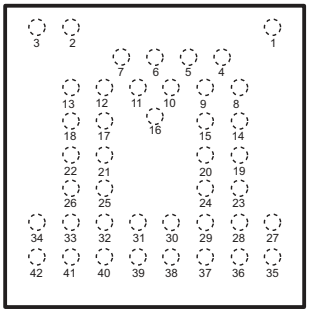
The HV2605 and HV2705 are 16-channel low harmonic distortion high-voltage analog switch integrated circuits (ICs). These devices are designed for applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers. The HV2705 has integrated bleed resistors which eliminate voltage build-up on capacitive loads such as piezoelectric transducers.

These ICs shift input data into a 16-bit Shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. This device combines high-voltage, bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

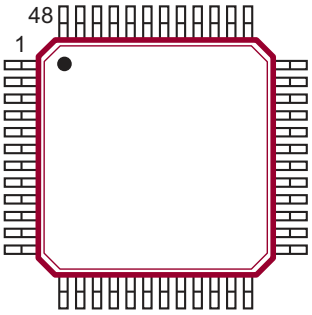
The device is suitable for various combinations of high-voltage supplies, e.g., V_{PP}/V_{NN}: +40V/–160V, +100V/–100V and +160V/–40V.

Package Types†

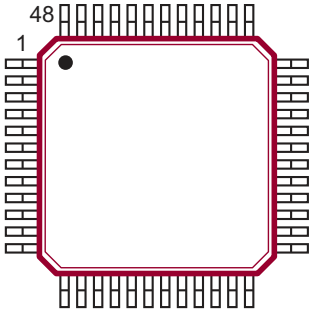
42-Ball Bumped Die
(Top view)



48-lead TQFP
(Top view)



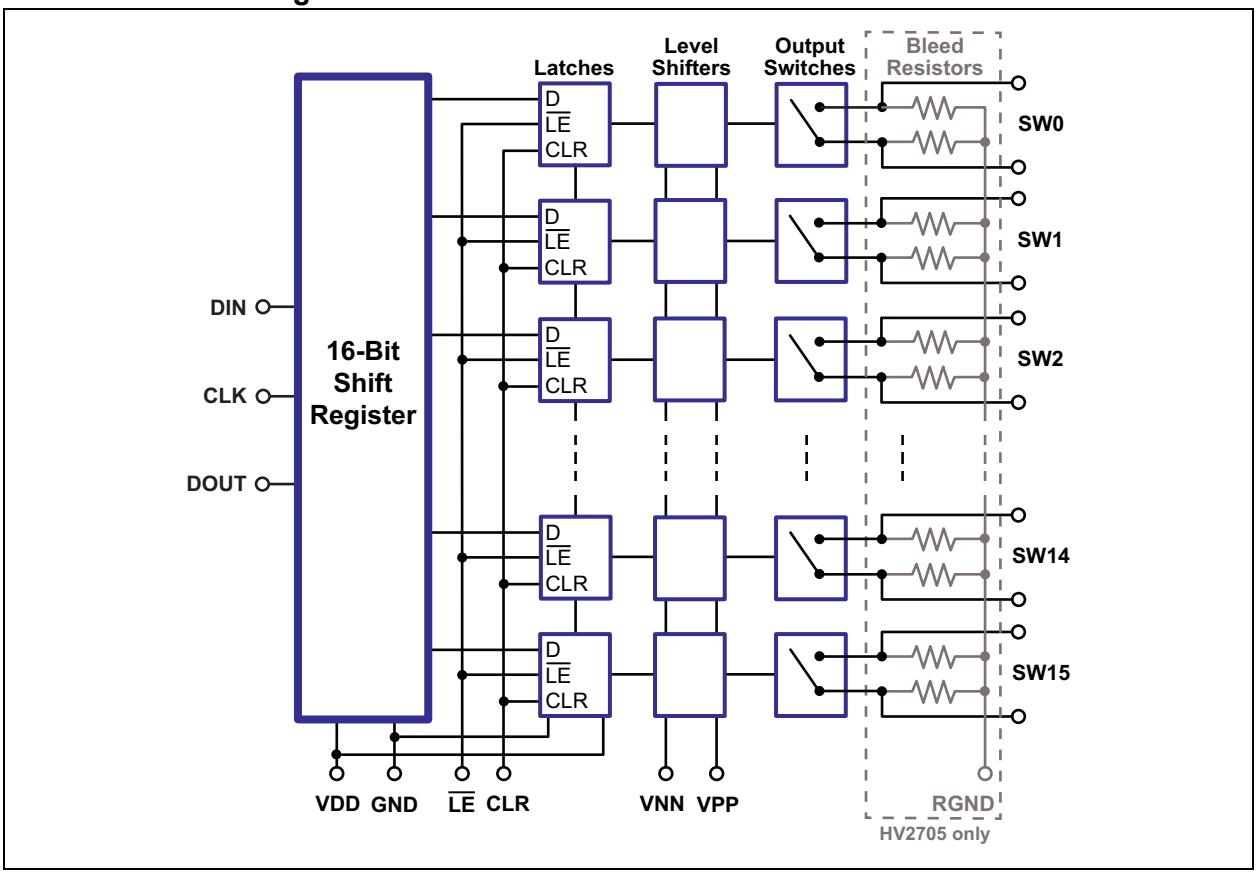
48-lead LQFP
(Top view)



See Table 2-1 and Table 2-2 for pin information.

† **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Logic Supply, V_{DD} ..... –0.5V to +7V
Differential Supply, V_{PP}–V_{NN} 220V
Positive Supply, V_{PP} ..... –0.5V to V_{NN} +200V
Negative Supply, V_{NN} ..... +0.5V to –200V
Logic Input Voltage ..... –0.5V to V_{DD} +0.3V
Analog Signal Range ..... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel 3A
Storage Temperature, T_S ..... –65°C to 150°C
Power Dissipation:
42-Ball Bumped Die 1.5W
48-Lead TQFP/LQFP 1W

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Power Supply Voltage	V_{DD}	3	—	5.5	V	**Note 1, Note 3**
Positive High-voltage Supply	V_{PP}	40	—	V_{NN}+200V	V	**Note 1, Note 3**
Negative High-voltage Supply	V_{NN}	–40	—	–160	V	**Note 1, Note 3**
High-level Input Voltage	V_{IH}	0.9 V_{DD}	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	0.1 V_{DD}	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	V_{NN} +10V	—	V_{PP}–10V	V	**Note 2**

Note 1: Power-up/power-down sequence is arbitrary except GND must be powered up first and powered down last.
2: V_{SIG} must be within $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power-up/power-down transition.
3: Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1 millisecond.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch ON-resistance	R_{ONS}	—	30	—	26	38	—	48	Ω	I_{SIG} = 5 mA	V_{PP} = +40V, V_{NN} = –160V
		—	25	—	22	27	—	32	Ω	I_{SIG} = 200 mA	
		—	25	—	22	27	—	30	Ω	I_{SIG} = 5 mA	V_{PP} = +100V, V_{NN}= –100V
		—	18	—	18	24	—	27	Ω	I_{SIG} = 200 mA	
		—	23	—	20	25	—	30	Ω	I_{SIG} = 5 mA	V_{PP} = +160V, V_{NN} = –40V
		—	22	—	16	25	—	27	Ω	I_{SIG} = 200 mA	
Small Signal Switch ON-resistance Matching	ΔR_{ONS}	—	20	—	5	20	—	20	%	I_{SIG} = 5 mA, V_{PP} = +100V, V_{NN} = –100V	
Large Signal Switch ON-resistance	R_{ONL}	—	—	—	15	—	—	—	Ω	V_{SIG} = V_{PP}–10V, I_{SIG} = 1A	
Output Bleed Resistor (HV2705 only)	R_{INT}	—	—	20	35	50	—	—	kΩ	Output Switch to R_{GND} I_{RINT} = 0.5 mA	
Switch OFF Leakage per Switch	I_{SOL}	—	5	—	1	10	—	15	µA	V_{SIG} = V_{PP}–10V and V_{NN}+10V (See **Section 3.1 "Test Circuits"**.)	
DC Offset Switch OFF	V_{OS}	—	300	—	100	300	—	300	mV	HV2605:100 kΩ load HV2705: No load (See **Section 3.1 "Test Circuits"**.)	
DC Offset Switch ON		—	500	—	100	500	—	500	mV		
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches off	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches off	
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches on, I_{SW} = 5 mA	
Quiescent V_{NN} Supply Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches on, I_{SW} = 5 mA	
Switch Output Peak Current	I_{SW}	—	3	—	3	2	—	2	A	V_{SIG} duty cycle < 0.1%	
Output Switching Frequency	f_{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V_{PP} Supply Current	I_{PP}	—	6.5	—	—	7	—	8	mA	V_{PP} = +40V, V_{NN} = –160V	50 kHz output switching frequency with no load
		—	4	—	—	5.5	—	5.5	mA	V_{PP} = +100V, V_{NN} = –100V	
		—	4	—	—	5	—	5.5	mA	V_{PP} = +160V, V_{NN} = –40V	
Average V_{NN} Supply Current	I_{NN}	—	6.5	—	—	7	—	8	mA	V_{PP} = +40V, V_{NN} = –160V	50 kHz output switching frequency with no load
		—	4	—	—	5	—	5.5	mA	V_{PP} = +100V, V_{NN} = –100V	
		—	4	—	—	5	—	5.5	mA	V_{PP} = +160V, V_{NN} = –40V	
Average V_{DD} Supply Current	I_{DD}	—	4	—	—	4	—	4	mA	f_{CLK} = 5 MHz, V_{DD} = 5V	
Quiescent V_{DD} Supply Current	I_{DDQ}	—	10	—	—	10	—	10	µA	All logic inputs are static.	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Data Out Source Current	I_{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	$V_{OUT} = V_{DD}–0.7V$
Data Out Sink Current	I_{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	$V_{OUT} = 0.7V$
Logic Input Capacitance	C_{IN}	—	10	—	—	10	—	10	pF	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 5V, $t_r = t_f \leq 5$ ns, 50% duty cycle and C_{LOAD} = 20 pF unless otherwise noted.

Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Set-up Time before Latch Enable Rises	t_{SD}	25	—	25	—	—	25	—	ns	
Time Width of $\overline{LE}$	t_{WLE}	56	—	—	56	—	56	—	ns	V_{DD} = 3V
		12	—	—	12	—	12	—	ns	V_{DD} = 5V
Clock Delay Time to Data Out	t_{DO}	50	100	50	78	100	50	100	ns	V_{DD} = 3V
		15	40	15	30	40	15	40	ns	V_{DD} = 5V
Time Width of CLR	t_{WCLR}	55	—	55	—	—	55	—	ns	
Set-up Time Data to Clock	t_{SU}	21	—	—	21	—	21	—	ns	V_{DD} = 3V
		7	—	—	7	—	7	—	ns	V_{DD} = 5V
Hold Time Data from Clock	t_H	2	—	2	—	—	2	—	ns	V_{DD} = 3V or 5V
Clock Frequency	f_{CLK}	—	10	—	—	10	—	10	MHz	V_{DD} = 3V
		—	20	—	—	20	—	20	MHz	V_{DD} = 5V
Clock Rise and Fall Times	t_r, t_f	—	50	—	—	50	—	50	ns	
Turn ON Time	T_{ON}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP}–10V$, R_{LOAD} = 10 kΩ (See **Section 3.1 "Test Circuits"**.)
Turn OFF Time	T_{OFF}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP}–10V$, R_{LOAD} = 10 kΩ (See **Section 3.1 "Test Circuits"**.)
Maximum V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	V_{PP} = +40V, V_{NN} = –160V
		—	20	—	—	20	—	20	V/ns	V_{PP} = +100V, V_{NN} = –100V
		—	20	—	—	20	—	20	V/ns	V_{PP} = +160V, V_{NN} = –40V
OFF Isolation	K_O	–30	—	–30	–33	—	–30	—	dB	f = 5 MHz, 1 kΩ//15 pF load (See **Section 3.1 "Test Circuits"**.)
		–58	—	–58	—	—	–58	—	dB	f = 5 MHz, 50Ω load (See **Section 3.1 "Test Circuits"**.)
Switch Crosstalk	K_{CR}	–60	—	–60	–70	—	–60	—	dB	f = 5 MHz, 50Ω load (See **Section 3.1 "Test Circuits"**.)

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{DD} = 5V, $t_r = t_f \leq 5$ ns, 50% duty cycle and C_{LOAD} = 20 pF unless otherwise noted.

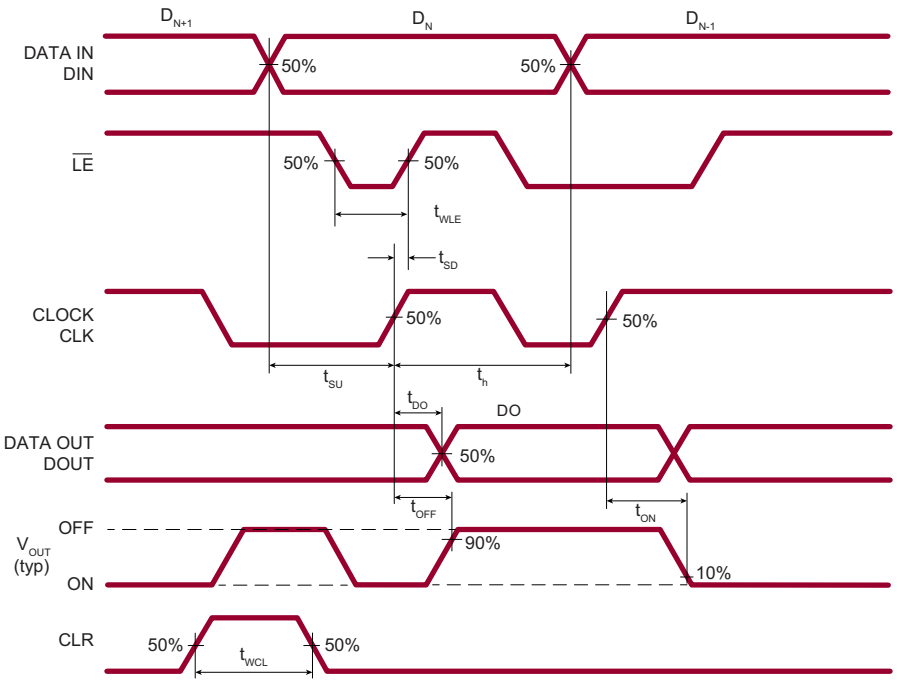
Parameter	Sym.	0°C		25°C			70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle (See **Section 3.1 "Test Circuits"**.)
OFF Capacitance SW to GND	$C_{SG(OFF)}$	—	15	—	10	15	—	15	pF	0V, f = 1 MHz
ON Capacitance SW to GND	$C_{SG(ON)}$	—	18	—	13	18	—	18	pF	0V, f = 1 MHz
Output Voltage Spike	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +40V, V_{NN} = –160V, R_{LOAD} = 50Ω (See **Section 3.1 "Test Circuits"**.)
	$-V_{SPK}$	—	—	—	—		—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +100V, V_{NN} = –100V, R_{LOAD} = 50Ω (See **Section 3.1 "Test Circuits"**.)
	$-V_{SPK}$	—	—	—	—		—	—	mV	
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +160V, V_{NN} = –40V, R_{LOAD} = 50Ω (See **Section 3.1 "Test Circuits"**.)
	$-V_{SPK}$	—	—	—	—		—	—	mV	
Charge Injection	QC	—	—	—	820	—	—	—	pC	V_{PP} = +40V, V_{NN} = –160V, V_{SIG} = 0V (See **Section 3.1 "Test Circuits"**.)
		—	—	—	600	—	—	—	pC	V_{PP} = +100V, V_{NN} = –100V, V_{SIG} = 0V (See **Section 3.1 "Test Circuits"**.)
		—	—	—	350	—	—	—	pC	V_{PP} = +160V, V_{NN} = –40V, V_{SIG} = 0V (See **Section 3.1 "Test Circuits"**.)

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	70	°C	
Storage Temperature	T_S	–65	—	150	°C	
PACKAGE THERMAL RESITANCE						
48-lead LQFP	θ_{JA}	—	52	—	°C/W	**Note 1**

Note 1: Mounted on an FR-4 board, 25 mm x 25 mm x 1.57 mm

Timing Waveforms



2.0 PIN DESCRIPTION

The description of pins in the 42-ball bumped die, 48-lead TQFP and 48-lead LQFP packages are listed on Table 2-1 and Table 2-2, respectively. The locations of the pads/balls are listed in **Package Types†**.

TABLE 2-1: 42-BALL BUMPED DIE PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
1	NC	—	No connection
	—	RGND	Ground for bleed resistor
2	VPP	VPP	Positive supply voltage
3	VNN	VNN	Negative supply voltage
4	DOUT	DOUT	Data out logic output
5	CLR	CLR	Latch clear logic input
6	CLK	CLK	Clock logic input for Shift register
7	GND	GND	Ground
8	SW15A	SW15A	Analog Switch 15 Terminal A
9	SW15B	SW15B	Analog Switch 15 Terminal B
10	$\overline{LE}$	$\overline{LE}$	Latch enable logic input, low active
11	VDD	VDD	Logic supply voltage
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	SW0B	SW0B	Analog Switch 0 Terminal B
14	SW14A	SW14A	Analog Switch 14 Terminal A
15	SW14B	SW14B	Analog Switch 14 Terminal B
16	DIN	DIN	Data in logic input
17	SW1A	SW1A	Analog Switch 1 Terminal A
18	SW1B	SW1B	Analog Switch 1 Terminal B
19	SW13A	SW13A	Analog Switch 13 Terminal A
20	SW13B	SW13B	Analog Switch 13 Terminal B
21	SW2A	SW2A	Analog Switch 2 Terminal A
22	SW2B	SW2B	Analog Switch 2 Terminal B
23	SW12A	SW12A	Analog Switch 12 Terminal A
24	SW12B	SW12B	Analog Switch 12 Terminal B
25	SW3A	SW3A	Analog Switch 3 Terminal A
26	SW3B	SW3B	Analog Switch 3 Terminal B
27	SW11A	SW11A	Analog Switch 11 Terminal A
28	SW11B	SW11B	Analog Switch 11 Terminal B
29	SW9B	SW9B	Analog Switch 9 Terminal B
30	SW8B	SW8B	Analog Switch 8 Terminal B
31	SW7A	SW7A	Analog Switch 7 Terminal A
32	SW6A	SW6A	Analog Switch 6 Terminal A
33	SW4A	SW4A	Analog Switch 4 Terminal A
34	SW4B	SW4B	Analog Switch 4 Terminal B
35	SW10B	SW10B	Analog Switch 10 Terminal B
36	SW10A	SW10A	Analog Switch 10 Terminal A
37	SW9A	SW9A	Analog Switch 9 Terminal A
38	SW8A	SW8A	Analog Switch 8 terminal A

TABLE 2-1: 42-BALL BUMPED DIE PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
39	SW7B	SW7B	Analog Switch 7 Terminal B
40	SW6B	SW6B	Analog Switch 6 Terminal B
41	SW5B	SW5B	Analog Switch 5 Terminal B
42	SW5A	SW5A	Analog Switch 5 Terminal A

TABLE 2-2: 48-LEAD TQFP/LQFP PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
1	NC	NC	No connection
2	NC	NC	No connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	SW3B	SW3B	Analog Switch 3 Terminal B
6	SW3A	SW3A	Analog Switch 3 Terminal A
7	SW2B	SW2B	Analog Switch 2 Terminal B
8	SW2A	SW2A	Analog Switch 2 Terminal A
9	SW1B	SW1B	Analog Switch 1 Terminal B
10	SW1A	SW1A	Analog Switch 1 Terminal A
11	SW0B	SW0B	Analog Switch 0 Terminal B
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	VNN	VNN	Negative supply voltage
14	NC	NC	No connection
15	VPP	VPP	Positive supply voltage
16	NC	NC	No connection
17	GND	GND	Ground
18	VDD	VDD	Logic supply voltage
19	DIN	DIN	Data in logic input
20	CLK	CLK	Clock logic input for Shift register
21	$\overline{LE}$	$\overline{LE}$	Latch-enable logic input, low active
22	CLR	CLR	Latch clear logic input
23	DOUT	DOUT	Data out logic output
24	NC	—	No connection
	—	RGND	Ground for bleed resistor
25	SW15B	SW15B	Analog Switch 15 Terminal B
26	SW15A	SW15A	Analog Switch 15 Terminal A
27	SW14B	SW14B	Analog Switch 14 Terminal B
28	SW14A	SW14A	Analog Switch 14 Terminal A
29	SW13B	SW13B	Analog Switch 13 Terminal B
30	SW13A	SW13A	Analog Switch 13 Terminal A
31	SW12B	SW12B	Analog Switch 12 Terminal B
32	SW12A	SW12A	Analog Switch 12 Terminal A
33	SW11B	SW11B	Analog Switch 11 Terminal B
34	SW11A	SW11A	Analog Switch 11 Terminal A

TABLE 2-2: 48-LEAD TQFP/LQFP PIN FUNCTION TABLE

Pin Number	HV2605 Pin Name	HV2705 Pin Name	Description
35	NC	NC	No connection
36	NC	NC	No connection
37	SW10B	SW10B	Analog Switch 10 Terminal B
38	SW10A	SW10A	Analog Switch 10 Terminal A
39	SW9B	SW9B	Analog Switch 9 Terminal B
40	SW9A	SW9A	Analog Switch 9 Terminal A
41	SW8B	SW8B	Analog Switch 8 Terminal B
42	SW8A	SW8A	Analog Switch 8 Terminal A
43	SW7B	SW7B	Analog Switch 7 Terminal B
44	SW7A	SW7A	Analog Switch 7 Terminal A
45	SW6B	SW6B	Analog Switch 6 Terminal B
46	SW6A	SW6A	Analog Switch 6 Terminal A
47	SW5B	SW5B	Analog Switch 5 Terminal B
48	SW5A	SW5A	Analog Switch 5 Terminal A

3.0 FUNCTIONAL DESCRIPTION

3.1 Test Circuits

Figure 3-1 to Figure 3-8 show the test circuits for HV2605/HV2705.

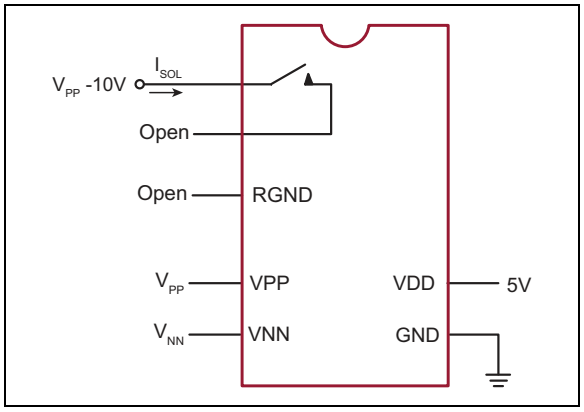


FIGURE 3-1: *Switch Off Leakage per Switch.*

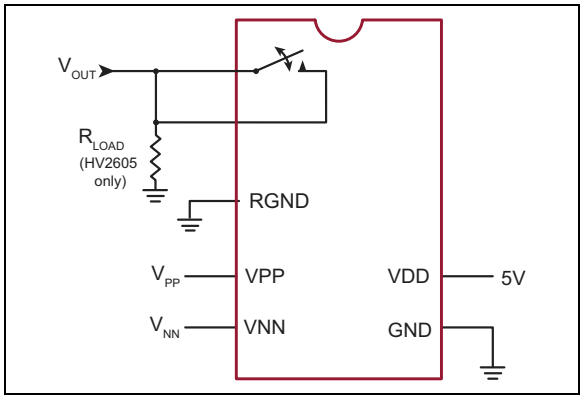


FIGURE 3-2: *Switch DC Offset.*

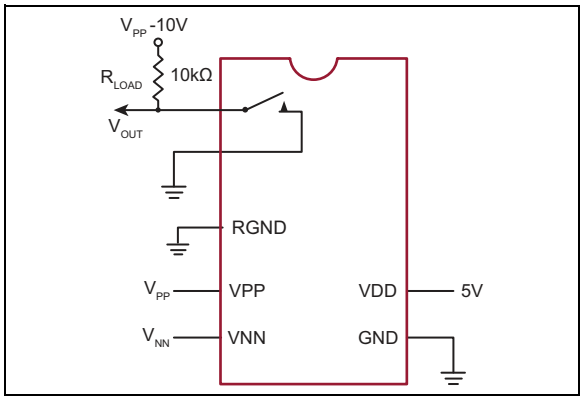


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

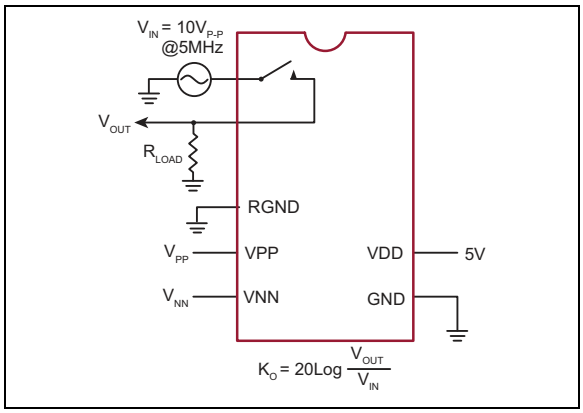


FIGURE 3-4: *Off Isolation.*

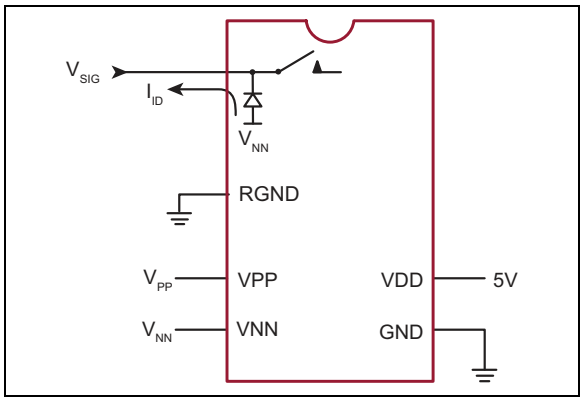


FIGURE 3-5: *Output Switch Isolation Diode Current.*

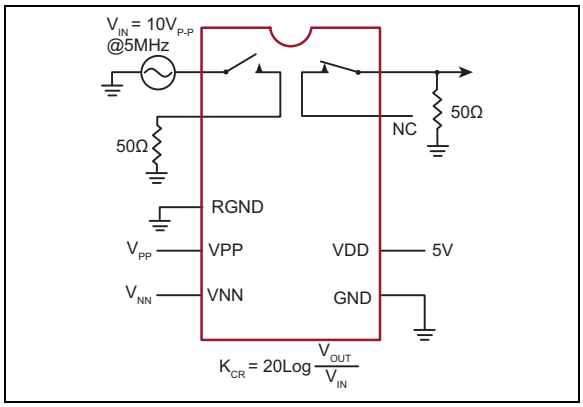


FIGURE 3-6: *Switch Crosstalk.*

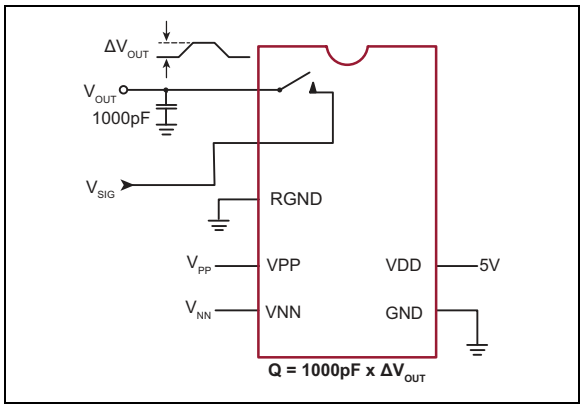


FIGURE 3-7: *Charge Injection.*

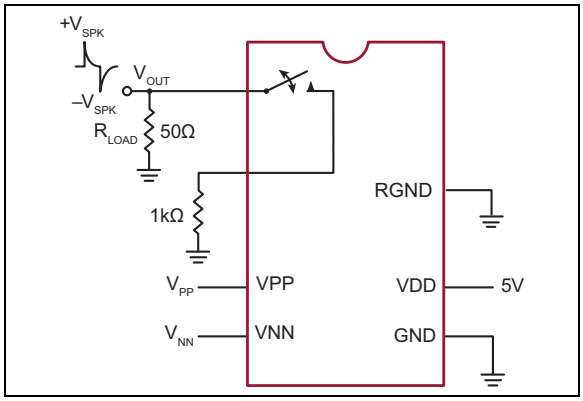


FIGURE 3-8: *Output Voltage Spike.*

TABLE 3-1: TRUTH FUNCTION TABLE

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	—		—	—		—	L	L	OFF	—		—	—		—
H	—		—	—		—	L	L	ON	—		—	—		—
—	L		—	—		—	L	L	—	OFF		—	—		—
—	H		—	—		—	L	L	—	ON		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		L	—		—	L	L	—	—		OFF	—		—
—	—		H	—		—	L	L	—	—		ON	—		—
—	—	...	—	L	...	—	L	L	—	—	...	—	OFF	...	—
—	—		—	H		—	L	L	—	—		—	ON		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		L	L	L	—	—		—	—		OFF
—	—		—	—		H	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 16 switches operate independently.

2: Serial data is clocked in on the low-to-high transition of the clock.

3: All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the Shift registers data flow through the latch.

4: D_{OUT} is high when data in the Shift register 15 is high.

5: Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.

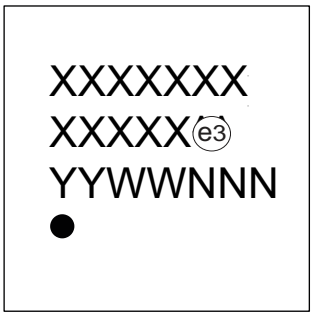
6: The CLR clear input overrides all other inputs.

4.0 PACKAGING INFORMATION†

4.1 Package Marking Information

† **Notice:** The LQFP package is not recommended for new designs. Please use TQFP package as an alternative.

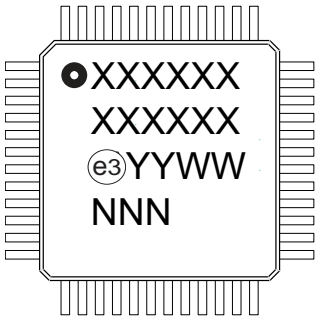
42-Ball Bumped Die



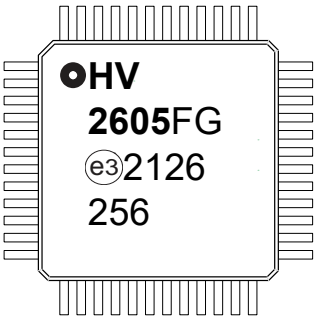
Example

Example

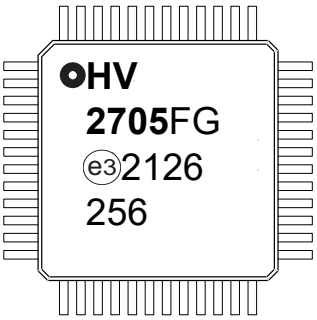
48-Lead LQFP



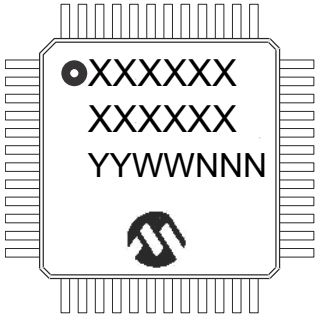
Example



Example

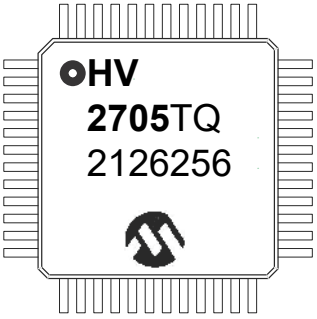


48-Lead TQFP



Example

Example

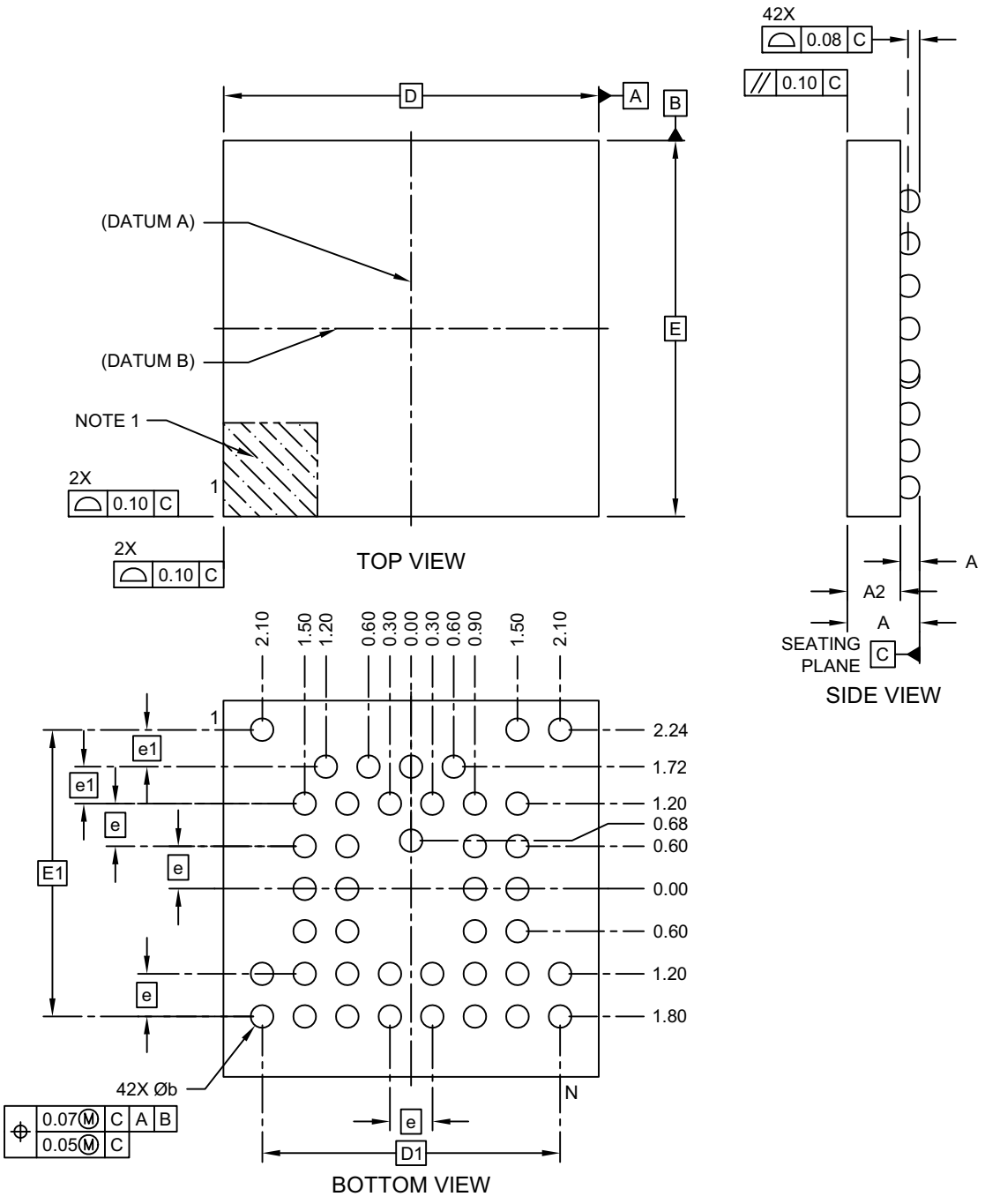


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

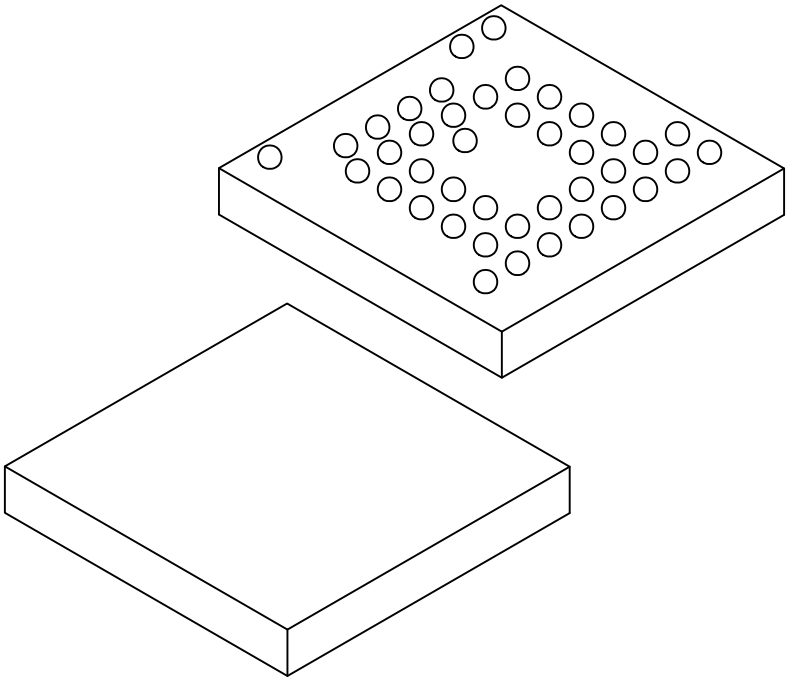
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-533-75X Rev B Sheet 1 of 2

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		42	
Terminal Pitch	e		0.60 BSC	
Terminal Pitch	e1		0.52 BSC	
Overall Height	A	0.91	0.965	1.02
Standoff	A1	0.21	0.24	0.27
Terminal Thickness	A2	0.70	0.725	0.75
Overall Length	D		5.29 BSC	
Exposed Pad Length	D1		4.20 BSC	
Overall Width	E		5.30 BSC	
Exposed Pad Width	E1		4.04 BSC	
Terminal Width	b	0.29	0.32	0.35

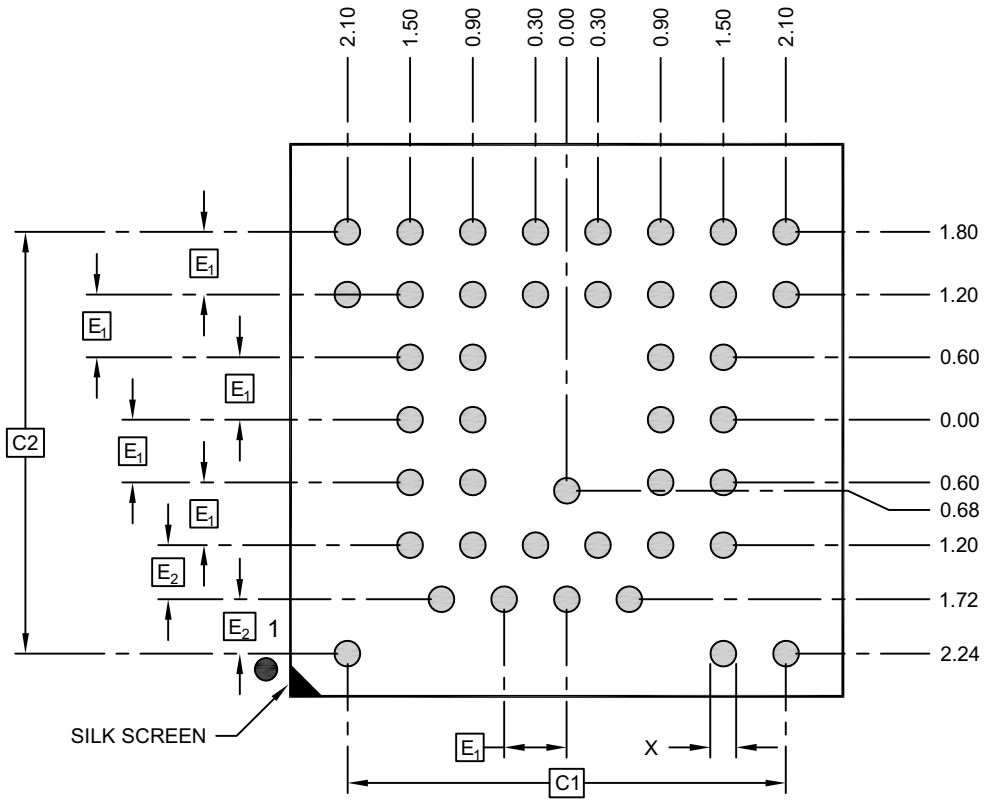
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-533-75X Rev B Sheet 2 of 2

42-Ball Chip Scale Package (75X) - 5.29x5.30x1.02 mm Body [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E_1		0.60 BSC	
Contact Pitch	E_2		0.52 BSC	
Contact Pad Spacing	C1		4.20 BSC	
Contact Pad Spacing	C2		4.04 BSC	
Contact Pad Width (Xnn)	X			0.25

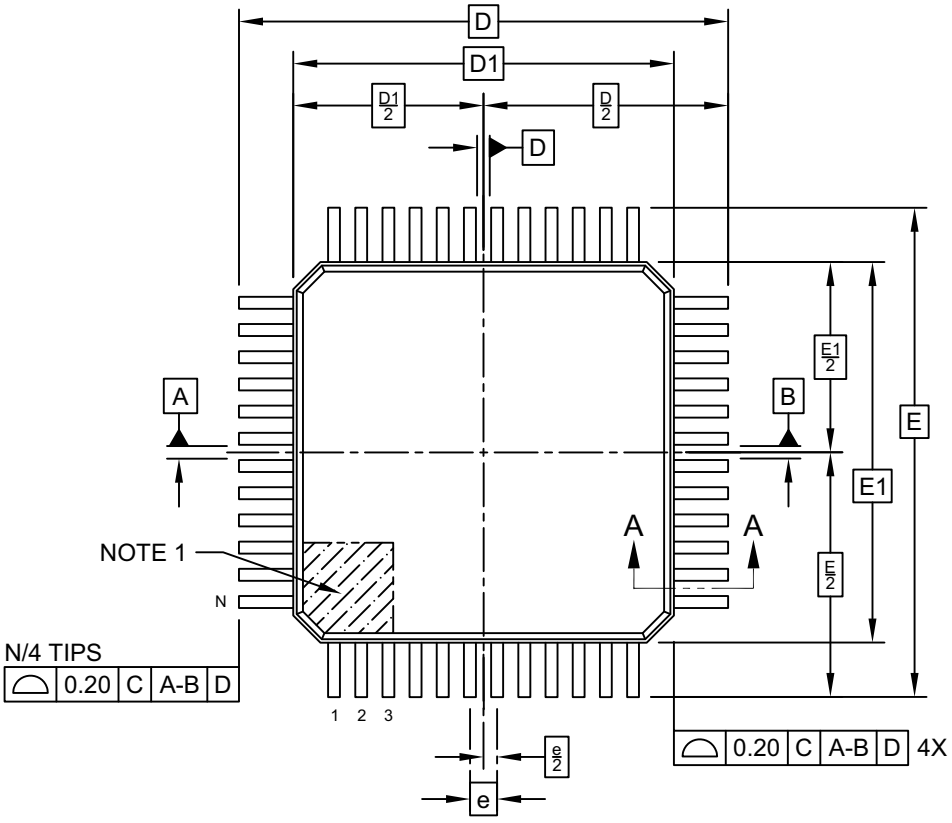
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

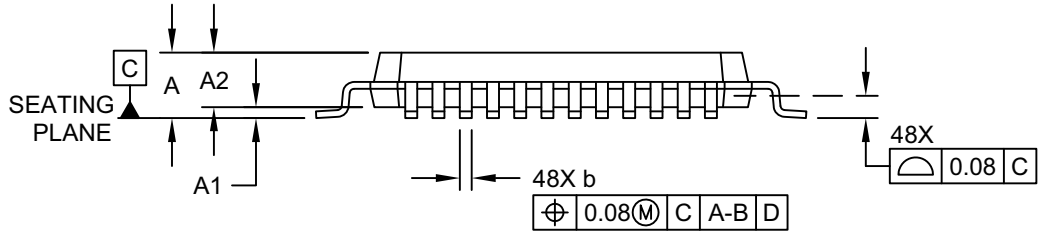
Microchip Technology Drawing C04-2533-75X Rev B

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

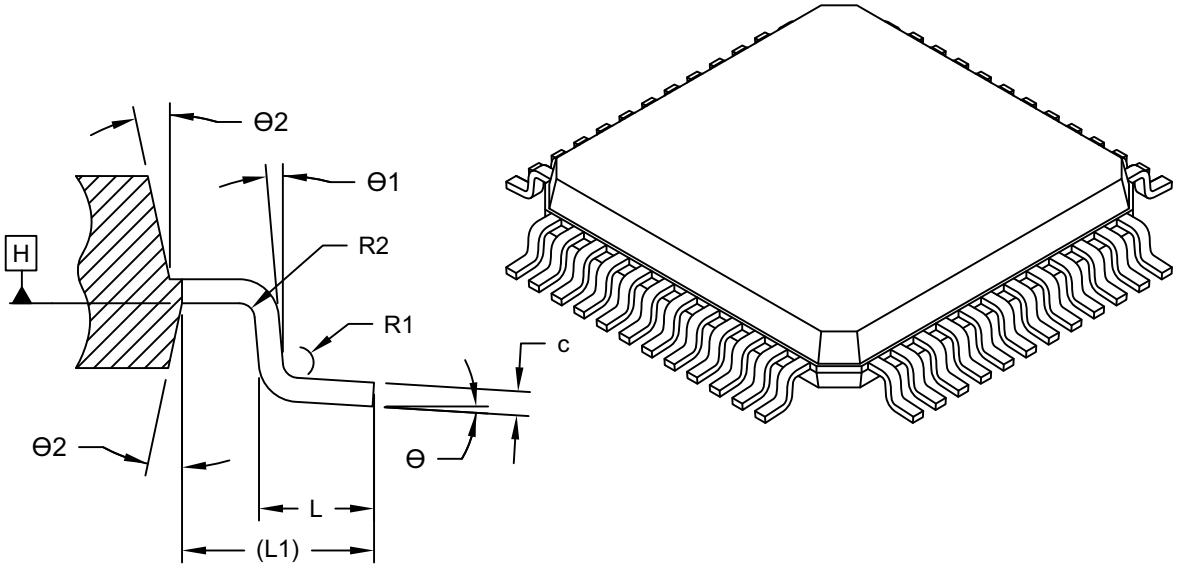


SIDE VIEW

Microchip Technology Drawing C04-300-Y8X Rev D Sheet 1 of 2

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

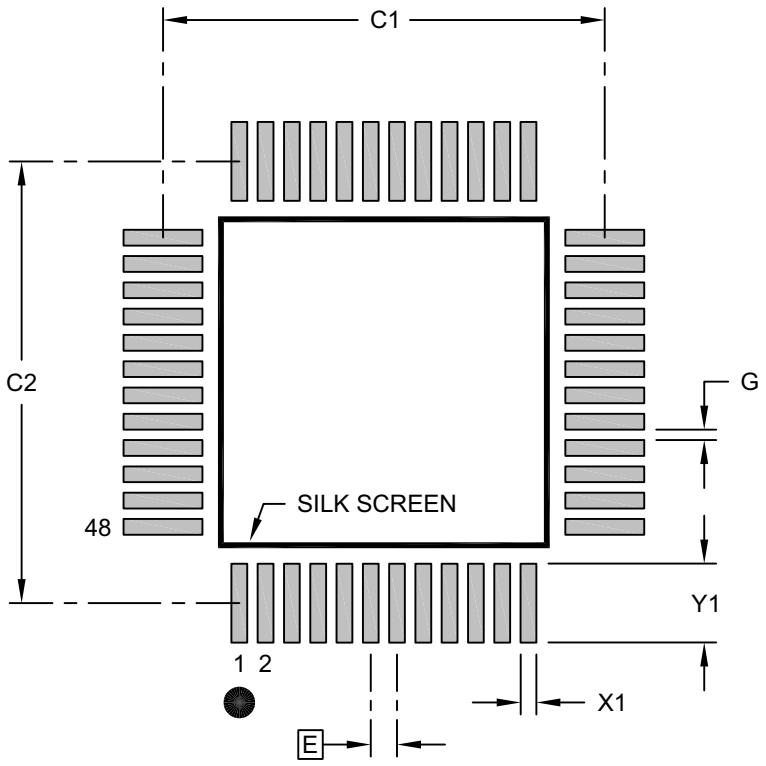
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-300-Y8X Rev D Sheet 2 of 2

48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

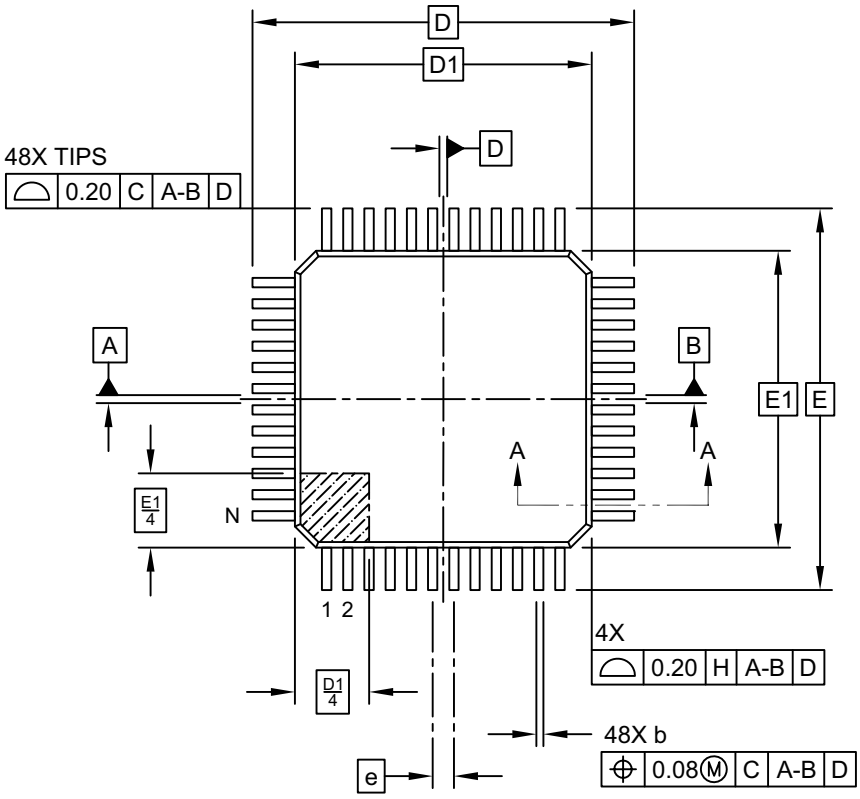
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

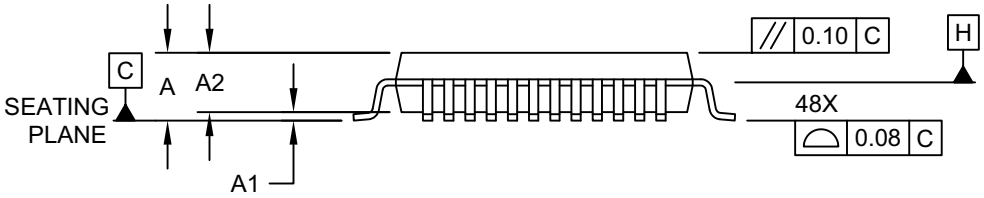
Microchip Technology Drawing C04-2300-Y8X Rev D

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

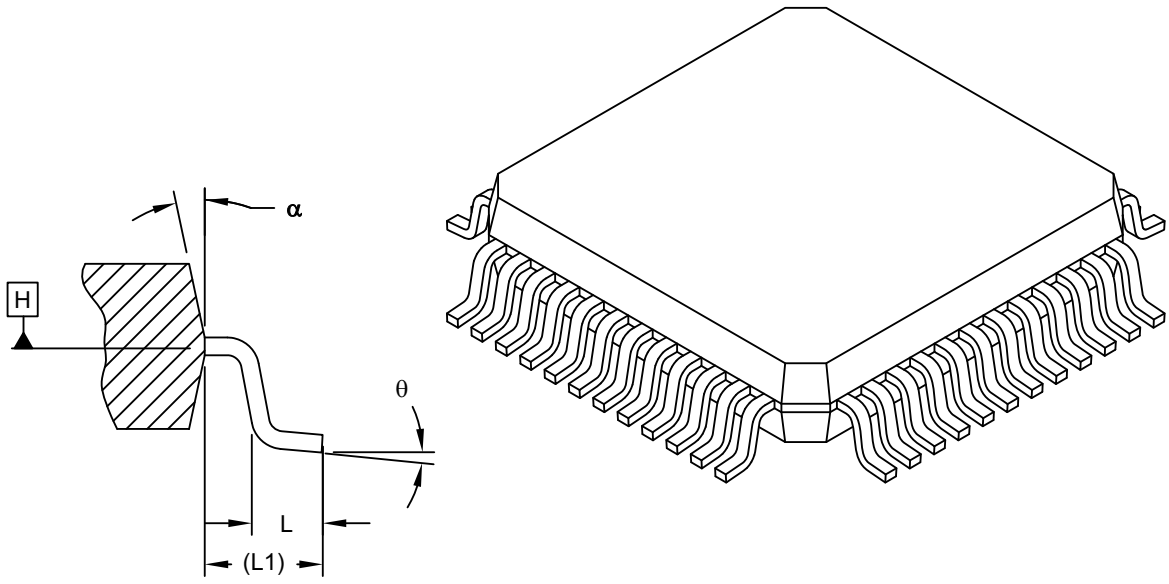


SIDE VIEW

Microchip Technology Drawing C04-278A Sheet 1 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

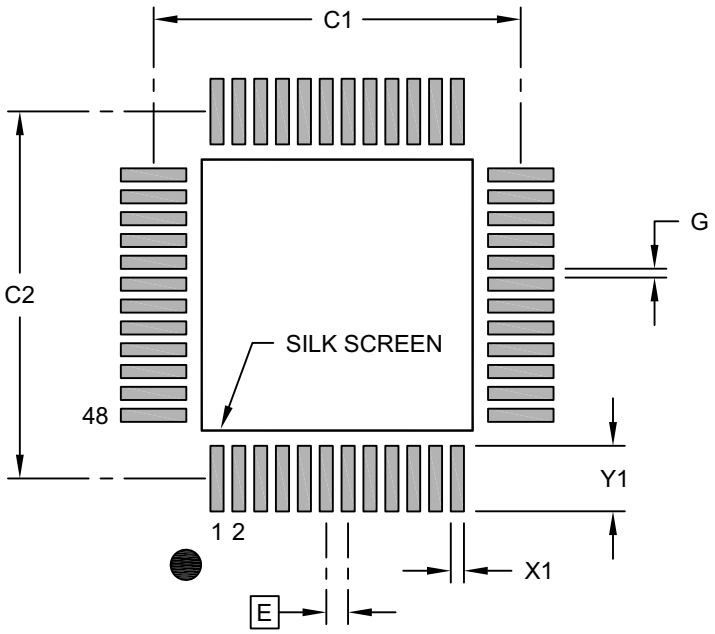
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-278A

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (May 2022)

- Minor layout changes.
- Added 48-Lead LQFP package notice to Package Types† and Packaging Information†.

Revision B (August 2021)

- Added 48-Lead TQFP Package
- Updated table Recommended Operating Conditions
- Updated **Section 1.0 "Electrical Characteristics"**
- Updated **Section 4.0 "Packaging Information†"**

Revision A (November 2017)

- Converted Supertex Doc # DSFP-HV2605 and Doc # DSFP-HV2705-HV2706 to Microchip DS20005498C
- Removed HV2706 from the document. HV2706 is EOL.
- Combined HV2605 and HV2705 into one document
- Changed the package marking format
- Added information for 42-Ball Bumped Die package
- Removed the "HVCMOS technology for high performance" in the Features section
- Made minor text changes throughout the document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-X	-XXXX
Device	Package	Environmental	Media Type

Devices:
- HV2605 = 16-Channel Low Harmonic Distortion High-Voltage Analog Switch
- HV2705 = 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors

Packages:
- BD = 42-Ball Bumped Die
- FG = 48-lead LQFP
- TQ = 48-lead TQFP

Environmental:
- G = Lead (Pb)-free/RoHS-compliant package (not used for BD packages)

Media Types:
- (blank) = 250/Tray for FG package
- (blank) = 250/Tray for TQ package
- M931 = 1000/Reel for FG package
- M931 = 1600/Reel for TQ package
- M936 = 2500/Reel for BD package

Examples:

a) HV2605FG-G: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch, 48-lead LQFP Package, 250/Tray

b) HV2605BD-M936: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch, 42-ball Bumped Die, 2500/Reel

c) HV2705TQ-G: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors, 48-lead TQFP Package, 250 Tray

d) HV2705FG-G-M931: 16-Channel Low Harmonic Distortion High-Voltage Analog Switch with Bleed Resistors, 48-lead LQFP Package, 1000/Reel

Note: HV2605BD and HV2705BD are RoHS-compliant products.

NOTES:

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