Texas Instruments

ADS5553 EVM User Guide

User's Guide

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Overview

This User's Guide document gives a general overview of the ADS5553 evaluation module (EVM), and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The ADS5553 EVM provides a platform for evaluating the ADS5553 dual 14 bit analog-to-digital converter (ADC) under various signals, references, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog inputs to the ADC are provided via external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device for both channels. Both analog input channels of the ADS5553 EVM have two independent paths. One input path uses a differential amplifier, while the other path is transformer coupled.

The EVM provides an external SMA connector for input of the ADC clock. The single-ended input the user provides is transformer coupled to provide a differential signal at both clock inputs of the device. The EVM also allows the user to send a single-ended or true differential clock if desired.

Digital output from the EVM are via two 40-pin connectors. The digital outputs from the ADC are buffered before going to the connectors.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and output driver supplies, external buffers supply, and differential amplifiers supply.

1.3 Power Requirements

The EVM can be powered directly with only a single +3.3V supply if using the module with transformer coupled input and internal reference mode. ±5V is required if using the differential amplifier input. Provision has also been made to allow the EVM to be powered with independent supplies to provide higher performance.

1.3.1 Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

1.4 ADS5553 EVM Operational Procedure

The ADS5553 EVM provides a flexible means of evaluating the ADS5553 in a number of modes of operation. A basic set-up procedure that can be used as a board confidence check is as follows:

1. Verify all jumper settings against the schematic jumper list in the following tables:

Table 1-1. Two Pin Jumper List

JUMPER	FUNCTION	INSTALLED	REMOVED	DEFAULT
SJP4	N/A			Removed
SJP5	N/A			Installed
W3	Reserved	N/A	N/A	Installed
W6	Reserved	N/A	N/A	Removed
W7	Reserved	N/A	N/A	Installed

Table 1-2. Three Pin Jumper List

JUMPER	FUNCTION	LOCATION: PINS 1-2	LOCATION: PINS 2-3	DEFAULT
SJP1	Common mode voltage path	Provide Common mode voltage to CHA Differential Amplifier	Provide Common mode voltage to Transformer T1	2-3
SJP3	Common mode voltage path	Provide Common mode voltage to CHB Differential Amplifier	Provide Common mode voltage to Transformer T2	2-3
W2	Channel A output enable	Outputs enabled	Outputs disabled	1-2
W10	Channel B output enable	Outputs enabled	Outputs disabled	1-2
W8	Common mode source	Selects ADS5553 channel A common mode source	Selects External common mode source	1-2
W9	Common mode source	Selects ADS5553 channel B common mode source	Selects External common mode source	1-2
SJP6	Reset polarity select	Used with active low ADC reset	Used with active high ADC reset	2-3
SJP8	U7 operation	Register	Buffer	2-3
SJP9	CLKOUTA path	Series resistor	Input to U7	2-3
SJP10	U10 operation	Register	Buffer	2-3
SJP11	CLKOUTB path	Series resistor	Input to U10	2-3

2. Connect supplies to the EVM as follows:
   +3.3V ADC output buffer supply to J17 and return to J18.
   +3.3V ADC analog supply to J11 and return to J10.
3. Switch power supplies on.
4. Use a function generator with 50-Ω output to input a 65-MHz, 0-V offset, 1-Vrms sine wave signal into J3. The frequency of the clock must be within the specification for the device speed grade.
5. Use frequency generators with a 50-Ω output to provide a 30-MHz, 0-V offset, -1-dBFS amplitude sine wave signals into J15 and J16. This will provide a transformer coupled differential input signal to both channels of the ADC. A full scale input tone into channel A or channel B is 2.2Vpp and dBFS can be calculated by using the following formula:

$$-\text{dBFS} = 20\log\frac{\text{captured max code} - \text{captured min code}}{2^N}, \text{ where N is the number of bits.}$$

6. The digital patterns on output connectors J8 and J21 should now represent a 2's compliment sine wave and can be monitored using a logic analyzer.

Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is attached to the end of this document.

2.2 Circuit Function

The following paragraphs describe the function of individual circuits. Refer to the relevant data sheet for device operating characteristics.

2.2.1 Analog Inputs

The EVM can be configured to provide the ADC with either transformer-coupled or differential amplifier inputs from a single-ended source. The inputs are provided via SMA connectors J15 and J16 for transformer coupled input, and J1, J2, J7 and J9 for differential amplifier input. To setup for one of these options, the EVM must be configured as follows:

1. For a 1:1 transformer coupled input to the ADC, a single ended source is connected to J15 for channel A and J16 for channel B. R43, R45, R49, and R61 must be removed. C107, C108, R80, and R81 provide the user with the option to add filters if desired. This is the default configuration for the EVM.
2. For single-ended inputs into the differential amplifiers, sources are connected to J2 for channel A and J9 for channel B. R43, R45, R49, and R61 must be installed. Surface mount jumpers, SPJ1 and SPJ2 must be configured such that pins 1 and 2 are shorted. Supply power to the differential amplifiers by connecting +5V to J14, -5V to J13 and connect the return to J12.
3. For a differential input into the amplifiers, the positive source of channel A is connected to J2 and the negative source to J1. The positive source of channel B is connected to J9 and the negative source to J7. R43, R45, R49, and R61 must be installed, and R74, R75, R78 and R79 removed. R19 and R22 must be replaced with 383 Ohm resistors, and R12 and R14 must be replaced with 54.9 Ohm resistors for proper termination. Surface mount jumpers, SPJ1 and SPJ2 must be configured such that pins 1 and 2 are shorted. Supply power to the differential amplifiers by connecting +5V to J14, -5V to J13 and connect the return to J12.

2.2.2 Clock Inputs

The EVM provides the clock inputs for both channels using a single-ended source. To provide a transformer-coupled differential clock to both channel clock inputs, simply provide a clock source to SMA J3.

2.2.2.1 True Differential ADC Clock

To provide a true differential ADC clock input, install J4, R11 and R25, and replace R31 with a 49.9 Ohm resistor, and remove T3. The positive source should be connected to J3 and the negative source to J4.

2.2.3 Control Inputs

The EVM has two discrete inputs to control the operation of the device:

2.2.3.1 Output Enables

With jumper W2 installed between pins 1 and 2, channel A of the ADC is enabled. This channel is disabled with the jumper installed between pins 2 and 3. With jumper W10 installed between pins 1 and 2, channel B of the ADC is enabled. This channel is disabled with the jump installed between pins 2 and 3.

2.2.3.2 IREF Control

By adjusting the resistance on R4, the user can adjust the bias current used by the ADS5553 device. The default value for the EVM is 56.2 kΩ. Care must be taken when changing this value. See the relevant data sheet for more information.

2.2.4 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a +3.3V analog supply (J11 and J10), +3.3V driver supply and external buffer supply (J17 and J18), and ±5V amplifier supply (J14, J13, and J12).

2.2.5 Outputs

The data outputs from the ADC are buffered using two Texas Instrument's SN74AVC16244s. Output data headers J8 and J21 are standard 40-pin headers on a 100-mil grid, and allow easy connection to a logic analyzer. The connector pinout is listed in Table 2-1.

Table 2-1. Output Connector J8/J21

J8 PIN	DESCRIPTION	J8 PIN	DESCRIPTION
1	OUTPUT CLOCK	21	DATA BIT 6
2	GND	22	GND
3	NC	23	DATA BIT 7
4	GND	24	GND
5	NC	25	DATA BIT 8
6	GND	26	GND
7	NC	27	DATA BIT 9
8	GND	28	GND
9	DATA BIT 0 (LSB)	29	DATA BIT 10
10	GND	30	GND
11	DATA BIT 1	31	DATA BIT 11
12	GND	32	GND
13	DATA BIT 2	33	DATA BIT 12
14	GND	34	GND
15	DATA BIT 3	35	DATA BIT 13 (MSB)
16	GND	36	GND
17	DATA BIT 4	37	OVERFLOW
18	GND	38	GND
19	DATA BIT 5	39	NC
20	GND	40	GND

Parts List

Table 3-1 lists the parts used in constructing the EVM

Table 3-1. Bill of Materials for ADS5553

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT INSTALLED
CAPACITORS					
47 uF, tantalum, 20%, 10V	5	ECS-T1AD476R	Panasonic	C19 C21 C75 C81 C82	
10 uF, 10V, 20% Capacitor	5	ECS-T1AX106R	Panasonic	C23 C27 C83 C87 C88	C46 C47 C48
10 uF, 10V, 10% Capacitor	4	T491A106K010AS	KEMET	C12 C20 C22 C26	
6.8pF,50V, +/- .25pF Capacitor	0	08055A6R8CAT2A	AVX		C98 C99 C100 C101
470 pF,100V, 10% Capacitor	8	ECJ-1VB2A471K	Panasonic	C57 C59 C61 C63 C109 C110 C111 C112	C33 C34
0.047uF,16V, 10% Capacitor	0	ECJ-1VB1C473K	Panasonic		C50 C51
10 pF, 50V, +/- .5pF Capacitor	0	ECJ-1VC1H100D	Panasonic		C102 C103
0.01uF, 50V,10% Capacitor	6	ECJ-1VB1C103K	Panasonic	C94 C95 C96 C97 C104 C105	C55
0.1uF,16V, 10% Capacitor	24	ECJ-1VB1C104K	Panasonic	C1 C13 C14 C15 C25 C30 C40 C58 C60 C62 C64 C65 C66 C70 C73 C74 C80 C84 C85 C86 C89 C91 C92 C93	C24 C29 C41-C44 C67 C113
1uF, 6.3V,10% Capacitor	4	ECJ-1VB0J105K	Panasonic	C78 C79 C114 C115	C53
2.2uF, 6.3V,+/- 80%/-20% Capacitor	0	ECJ-1VF0J225Z	Panasonic		C56
2 pF, 25V, +/-0.25 pF Capacitor	2	ECJ-1VC1H020C	Panasonic	C16 C17	
0.1uF,16V, +/- 80%/-20% Capacitor	11	ECJ-0EF1C104Z	Panasonic	C2-C11 C28	
10 pF, 50V, +/- 0.5pF Capacitor	2	ECJ-0EC1H100D	Panasonic		C107 C108
RESISTORS					
0 Ohm resistor, 1/16 W, 1 %	2	ERJ-6ENF0R00V	Panasonic	R12 R14	R11 R25
54.9 Ohm resistor, 1/16 W, 1 %	2	ERJ-6ENF54R9V	Panasonic	R82 R83	
383 Ohm resistor, 1/16 W, 1 %	2	ERJ-6ENF3830V	Panasonic	R28 R33	
392 Ohm resistor, 1/16 W, 1 %	4	ERJ-6ENF3920V	Panasonic	R35 R36 R40 R41	
412 Ohm resistor, 1/16 W, 1 %	2	ERJ-6ENF4120V	Panasonic	R19 R22	
0 Ohm resistor, 1/16 W, 1 %	5		Panasonic	R31 R42 R59 R94 R102	R38 R39 R56 R57 R58 R65
1 Ohm resistor, 1/16 W, 5 %	4	9C0603A1 JLHFT	Panasonic	R10 R37 R55 R93	
100 Ohm resistor, 1/16 W, 1%	0	ERJ-3EKF1000V	Panasonic		R23 R24

Table 3-1. Bill of Materials for ADS5553 (continued)

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT IN-STALLED
36.5 Ohm resistor, 1/16 W, 1%	4	ERJ-3EKF36R5V	Panasonic	R72 R73 R76 R77	
49.9 Ohm resistor, 1/16 W, 1%	1	ERJ-3EKF49R9V	Panasonic	R30	R7 R13
200 Ohm resistor, 1/16 W, 1%	0	ERJ-3EKF200V	Panasonic		R32
1K Ohm resistor, 1/16 W, 1%	0	ERJ-3EKF1001V	Panasonic		R95 R96 R97 R98
10K Ohm resistor, 1/16 W, 1%	1	ERJ-3EKF1002V	Panasonic	R99	R20 R21 R60
2K Ohm resistor, 1/16 W, 1%	0	ERJ-3EKF2001V	Panasonic		R15 R26 R27 R29
49.9K Ohm resistor, 1/16 W, 1%	1	ERJ-3EKF4992V	Panasonic	R51	R50 R52
4.99K Ohm resistor, 1/16 W, 1%	0		Panasonic		R16 R34
56.2K Ohm resistor, 1/16 W, 1%	1	ERJ-3EKF5622V	Panasonic	R4	
174 Ohm resistor, 1/16 W, 1 %	0	ERJ-2RFK1740X	Panasonic		R80 R81
1K VARIABLE RESISTOR	0	CT94W102	CERMET		R17 R18
0 Ohm R-Pack	4	742C163000JCT	CTS	RP7 RP8 RP9 RP10	RP1 RP2 RP3 RP6
CONNECTORS, JUMPERS, HEADERS, FERRITE BEADS, TRANSFORMERS, ICS					
Ferrite Bead	5	EXC-ML32A680U		FB1 FB2 FB3 FB5 FB6	FB4
Transformer	2	ADT1-1W T	Mini-Circuits	T1 T2	
Transformer	1	ADT4-1WT	Mini-Circuits	T3	
SMA connectors	7	2262-0000-09	NEWARK	J1 J2 J3 J7 J9 J15 J16	J4 J5
Black test point	3	5011K-ND	Keystone	TP1 TP3 TP4	
RED test point	0	5010K-ND	Keystone		TP6 TP7
2POS_header	3	TSW-150-07-L-S	Samtec	W3 W6 W7	
3POS_header	4	TSW-150-07-L-S	Samtec	W2 W8 W9 W10	
SWITCH	1	EVQ-PJX04M	Panasonic	S1	
40 pin IDC Connector	1	TSW-120-07-L-D	Samtec	J8 J21	
10 pin IDC Connector	0	TSW-120-07-L-D	Samtec		J6
Red Banana Jacks	4	ST-351A	ALLIED	J11 J13 J14 J17	
Black Banana Jacks	3	ST351B	ALLIED	J10 J12 J18	
ADS5553	1	ADS5553	Texas Instruments	U1	
THS4503	2	THS4503	Texas Instruments	U2 U9	
OPA2227UA	0	OPA2227UA	Texas Instruments		U3
TPS79225	0	TPS79225	Texas Instruments		U4
SN74AVC16244	2	SN74AVC16244DGG	Texas Instruments	U7 U10	
SCREWS	4				
Plastic Stand Off Hex (1/4 x .5")	4	1902CK-ND	ALLIED		

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

4.1 PCB Layout

The EVM is constructed on a 6-layer, 6.0-inch x 5.1-inch, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in the diagrams attached to the end of this document.

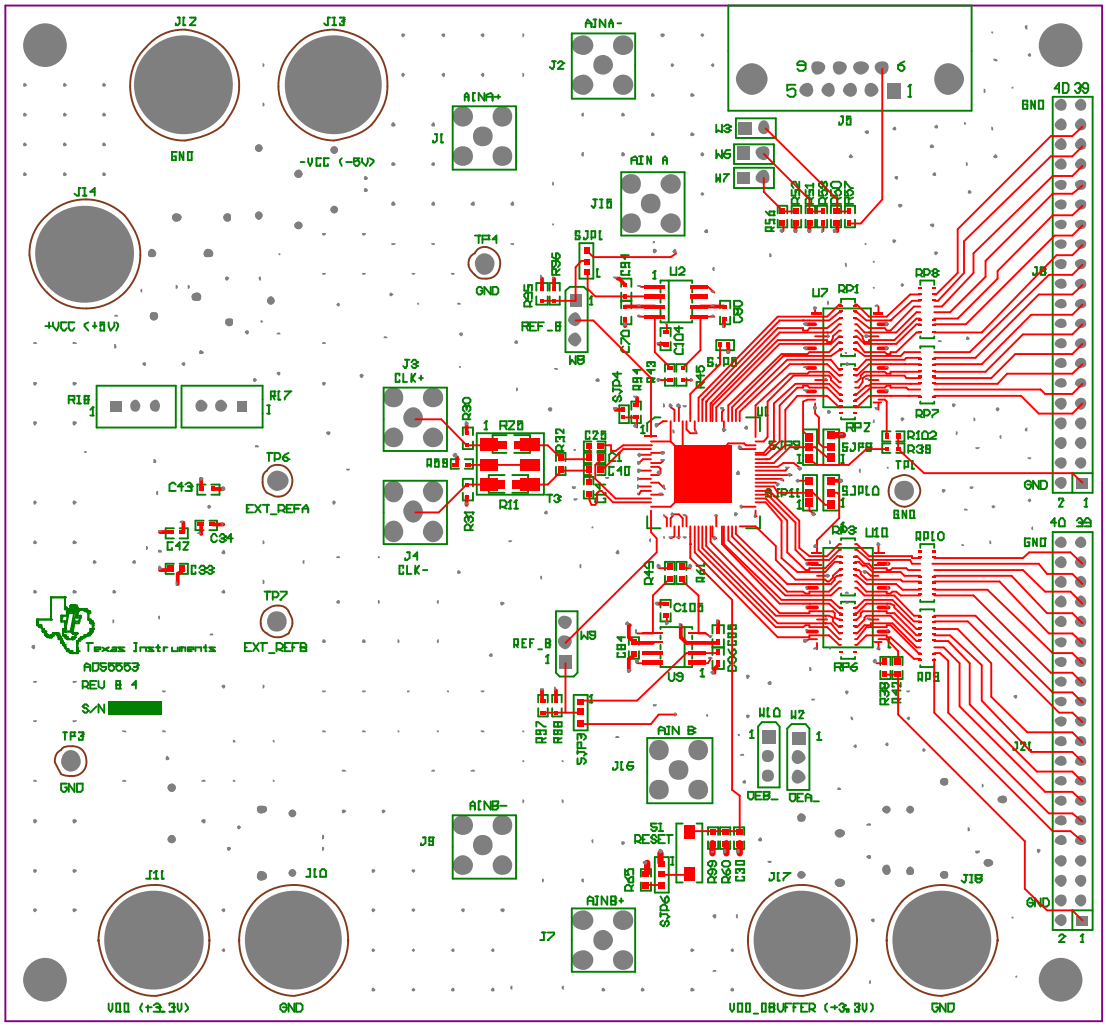


Figure 4-1. Top Layer

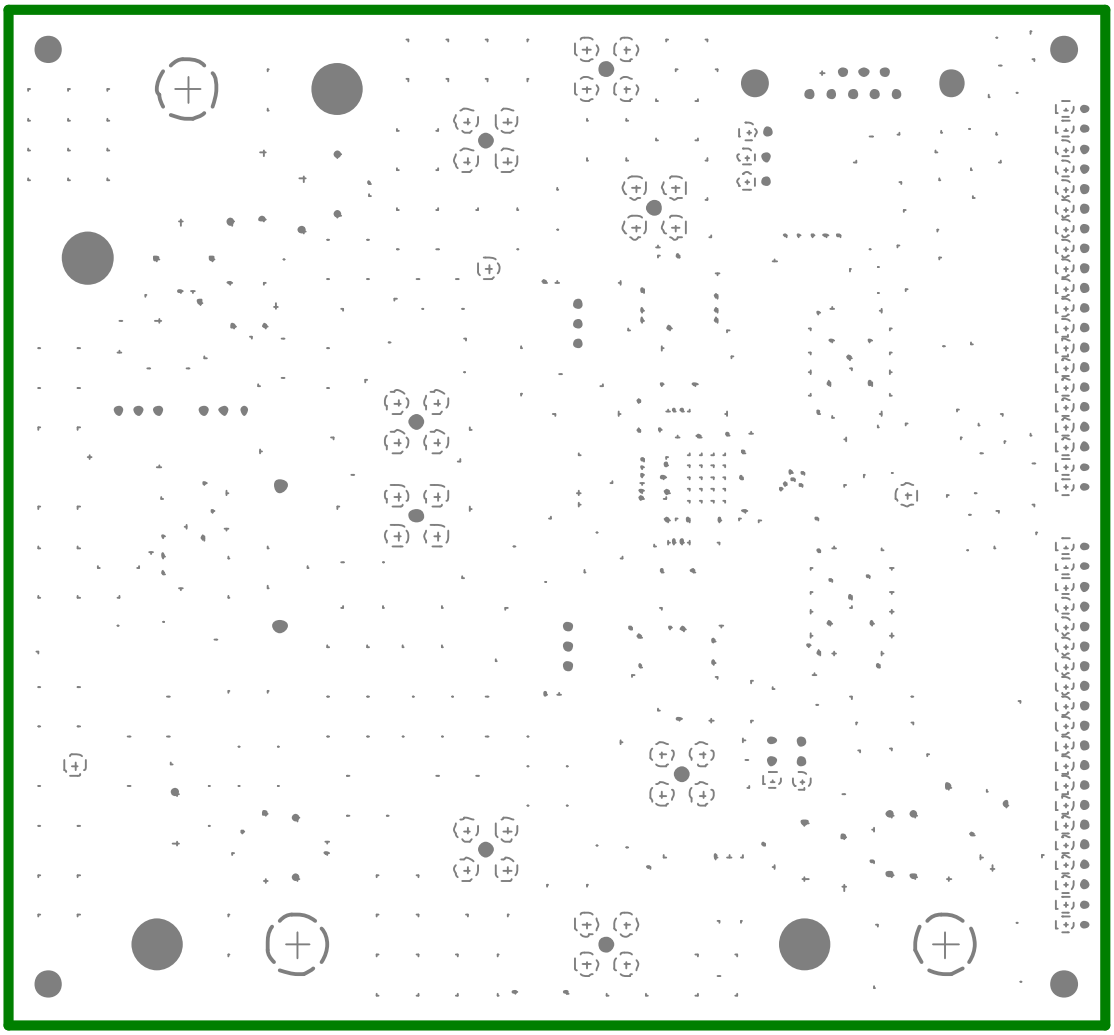


Figure 4-2. Layer 2, Ground Plane

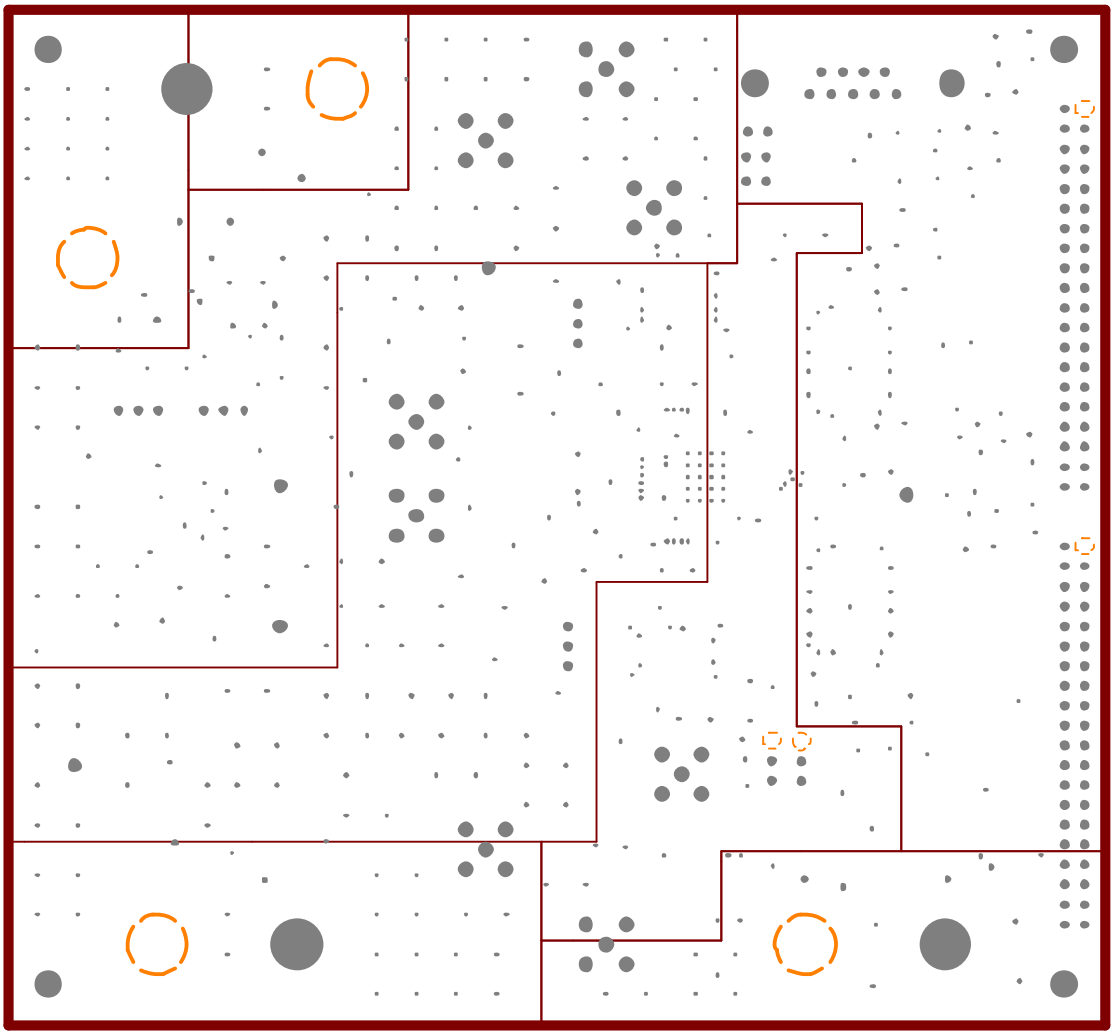


Figure 4-3. Layer 3, Power Plane #1

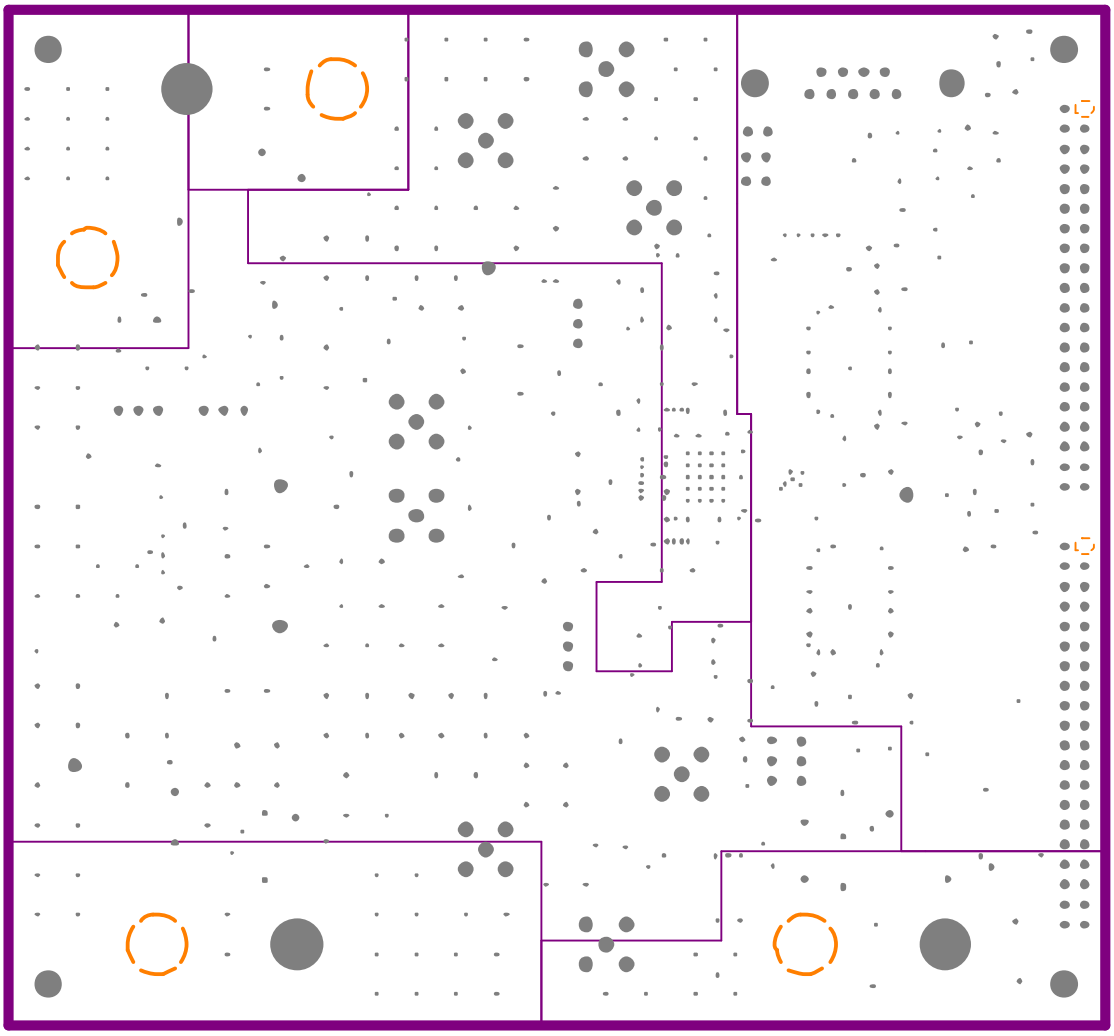


Figure 4-4. Layer 4, Power Plane #2

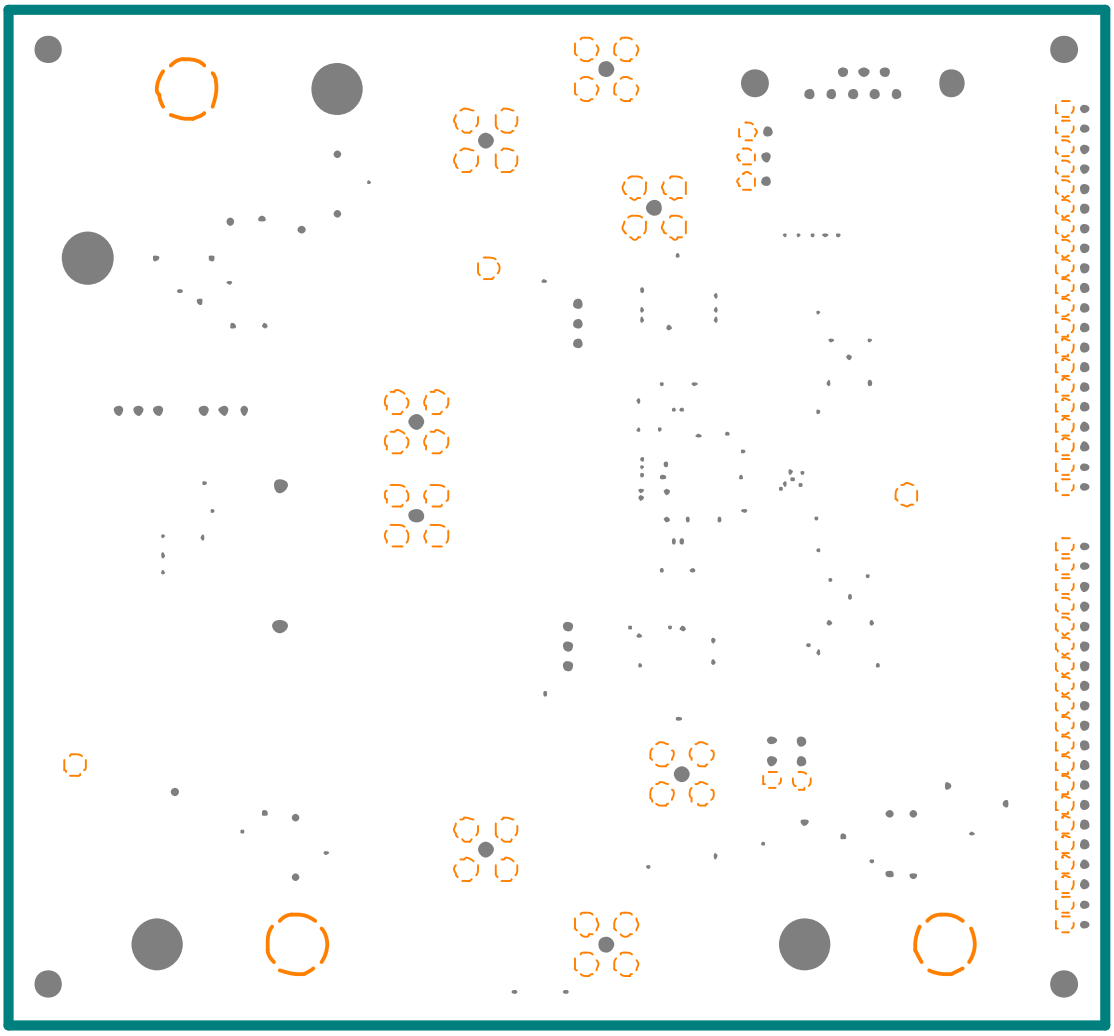


Figure 4-5. Layer 5, Ground Plane

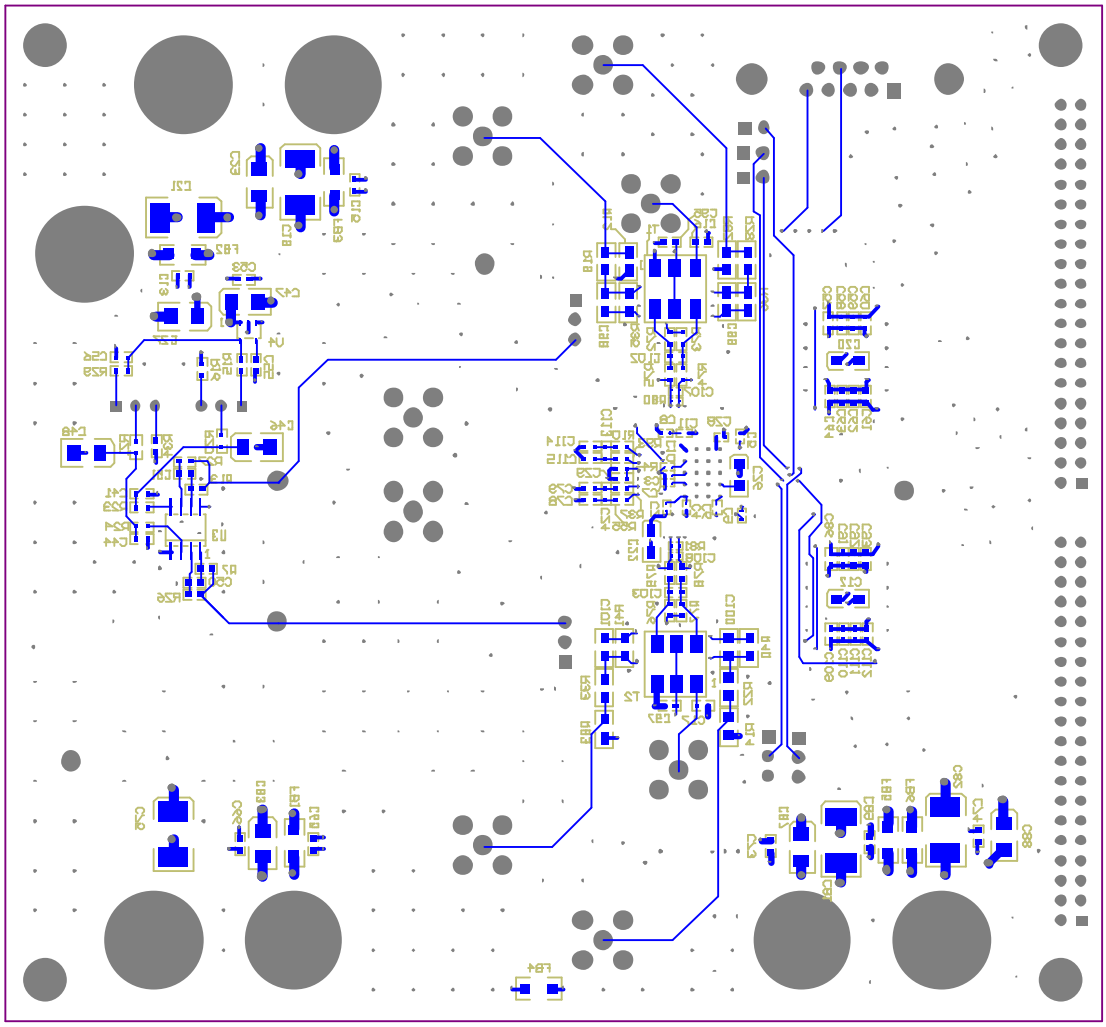
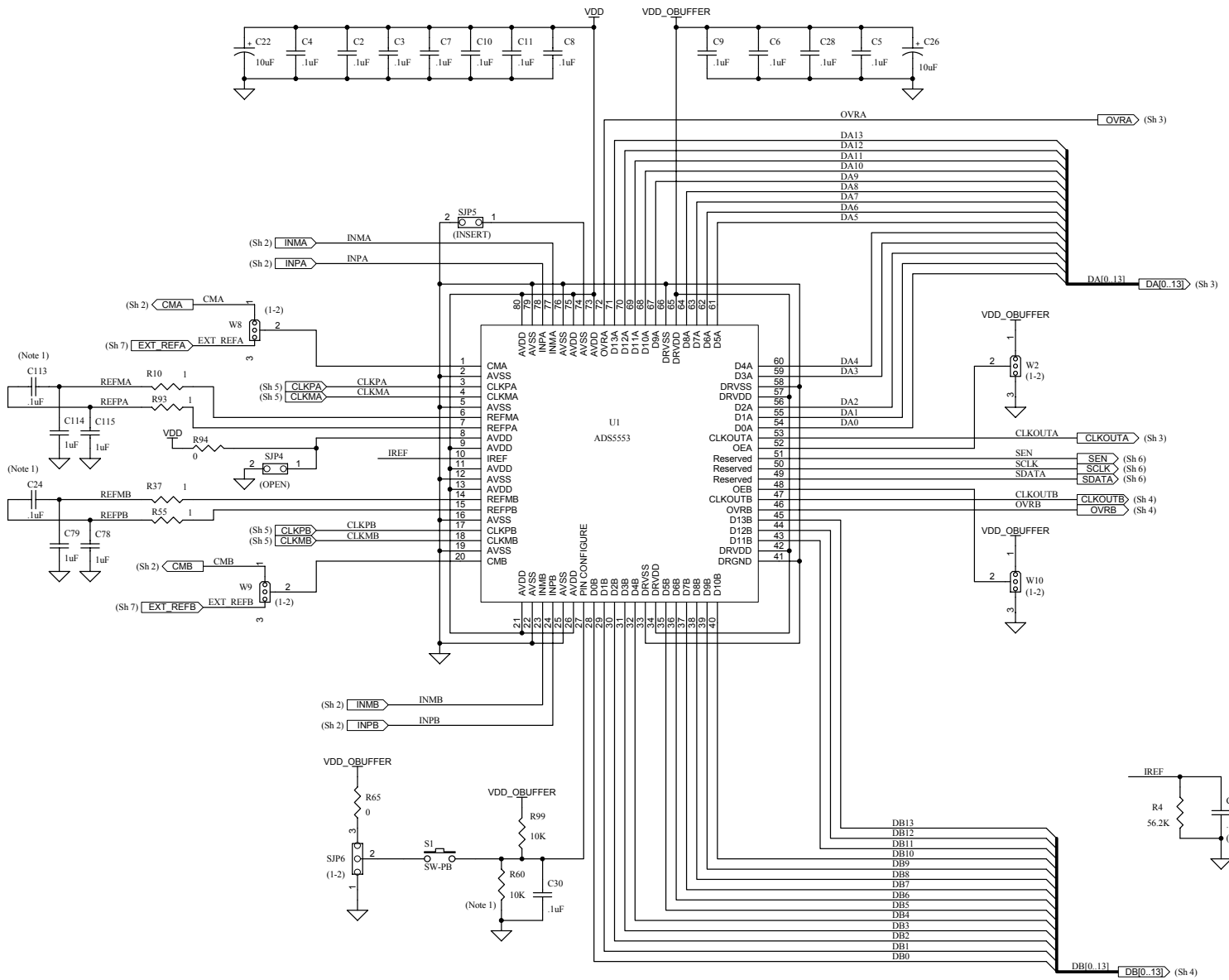


Figure 4-6. Layer 6, Bottom Layer



Note 1. Part not installed

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Engineer: J. SETON			
Drawn By: Y. DEWONCK	SIZE:	DATE: 17-Jan-2005	REV: A
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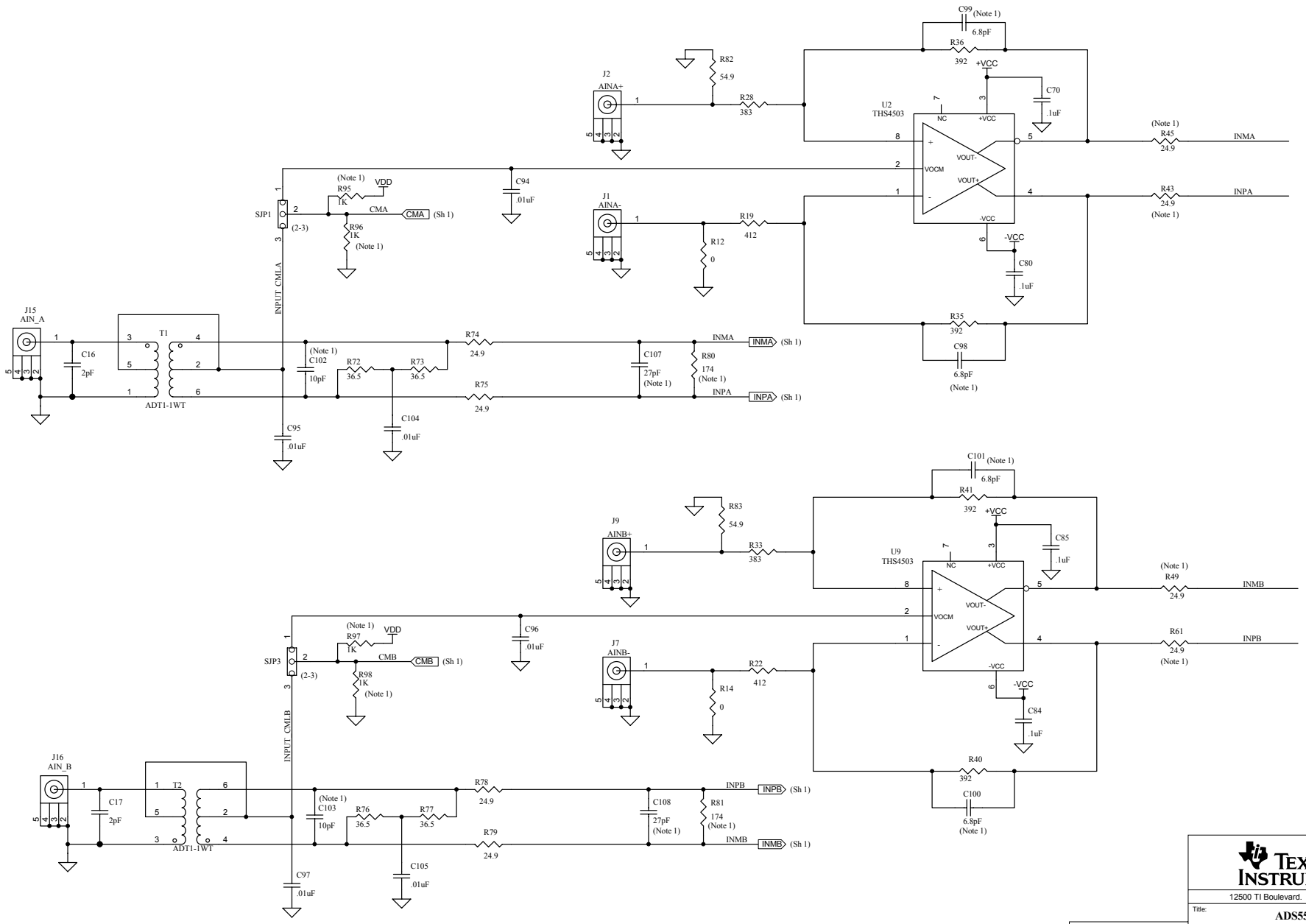

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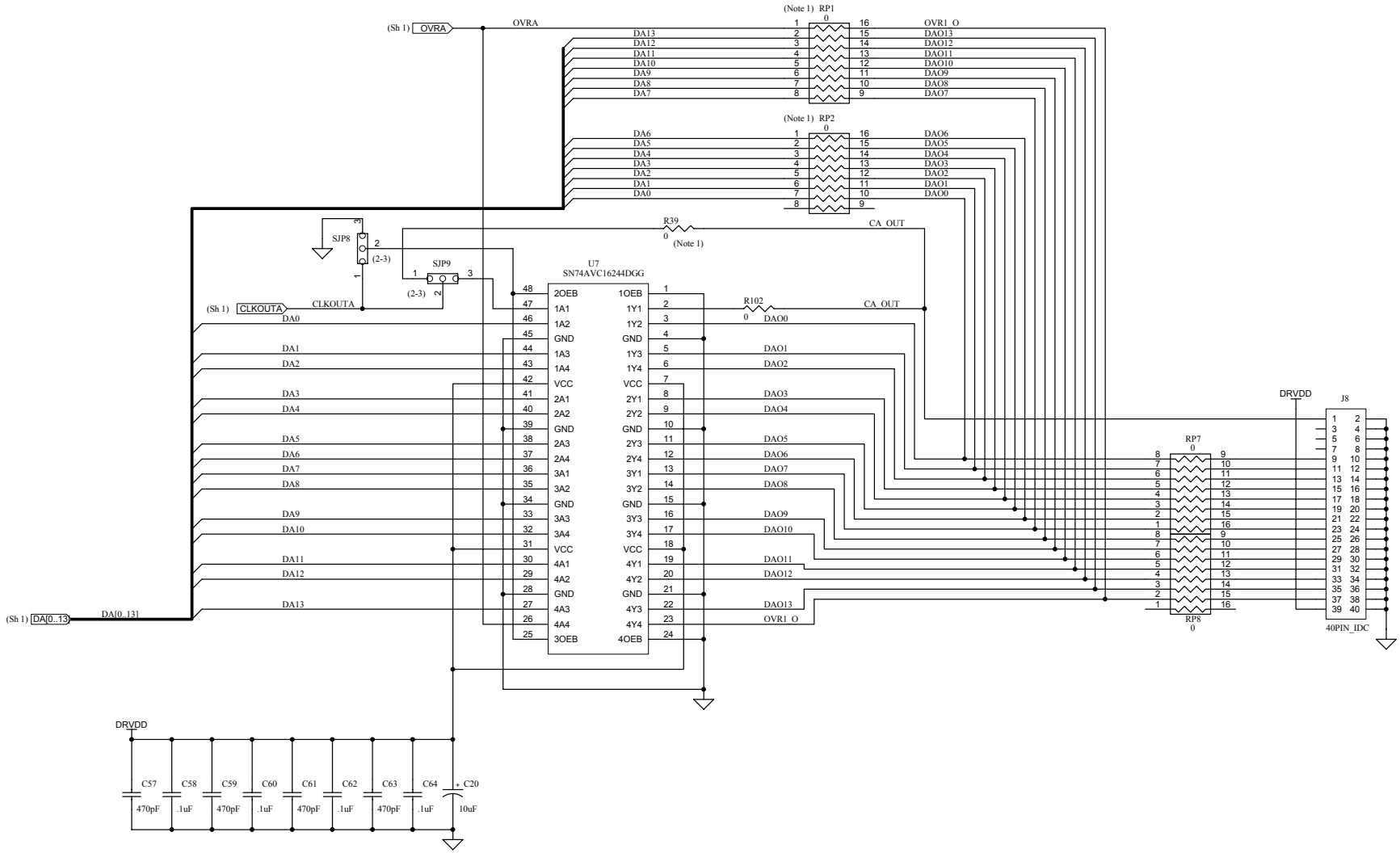

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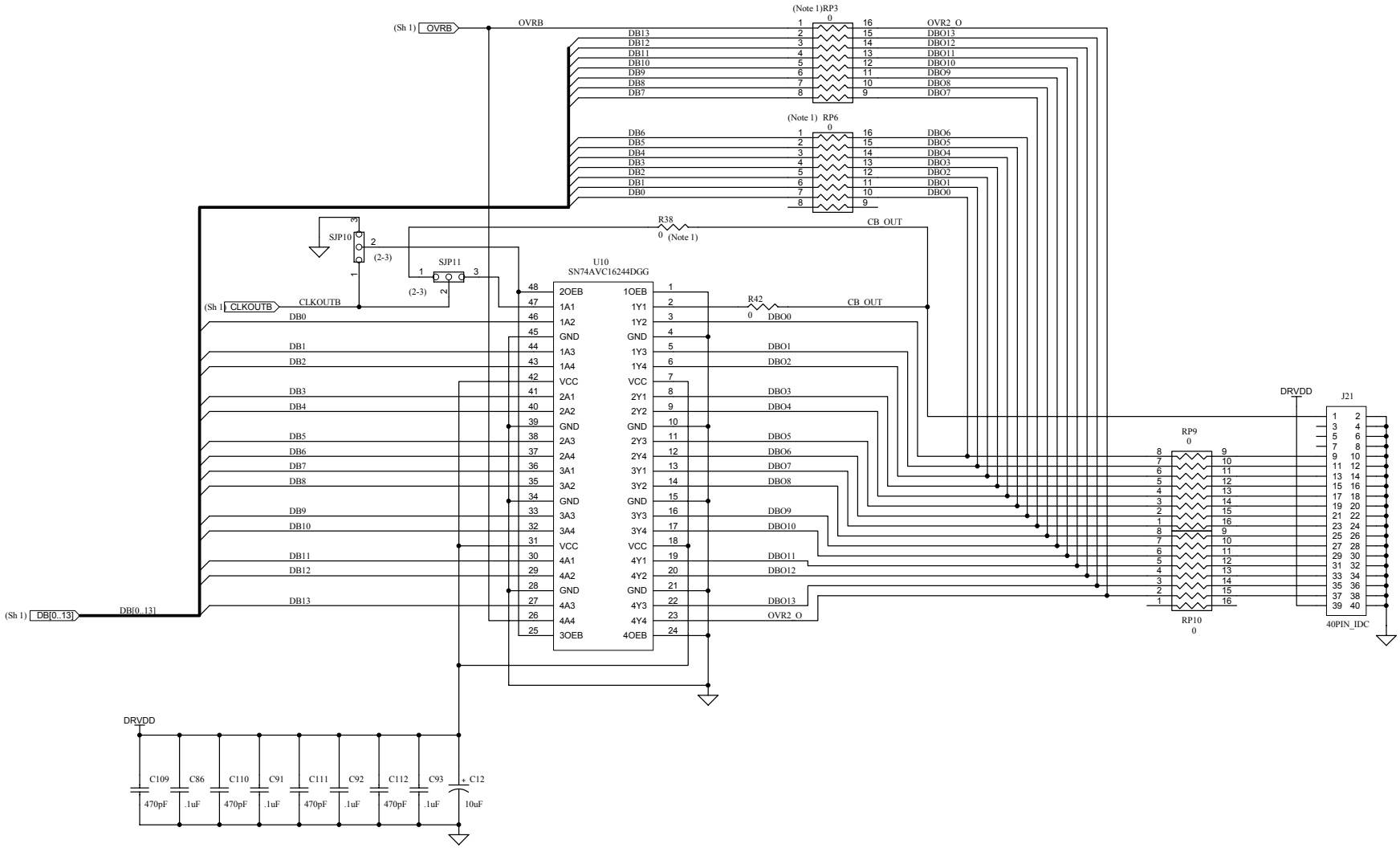

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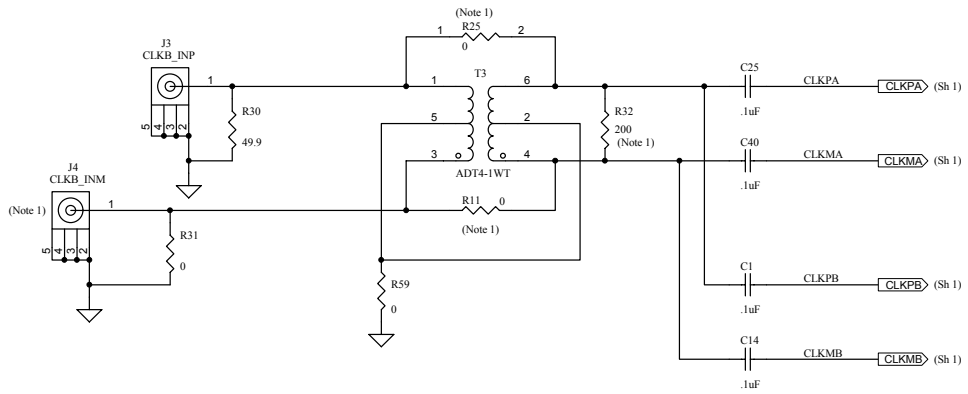

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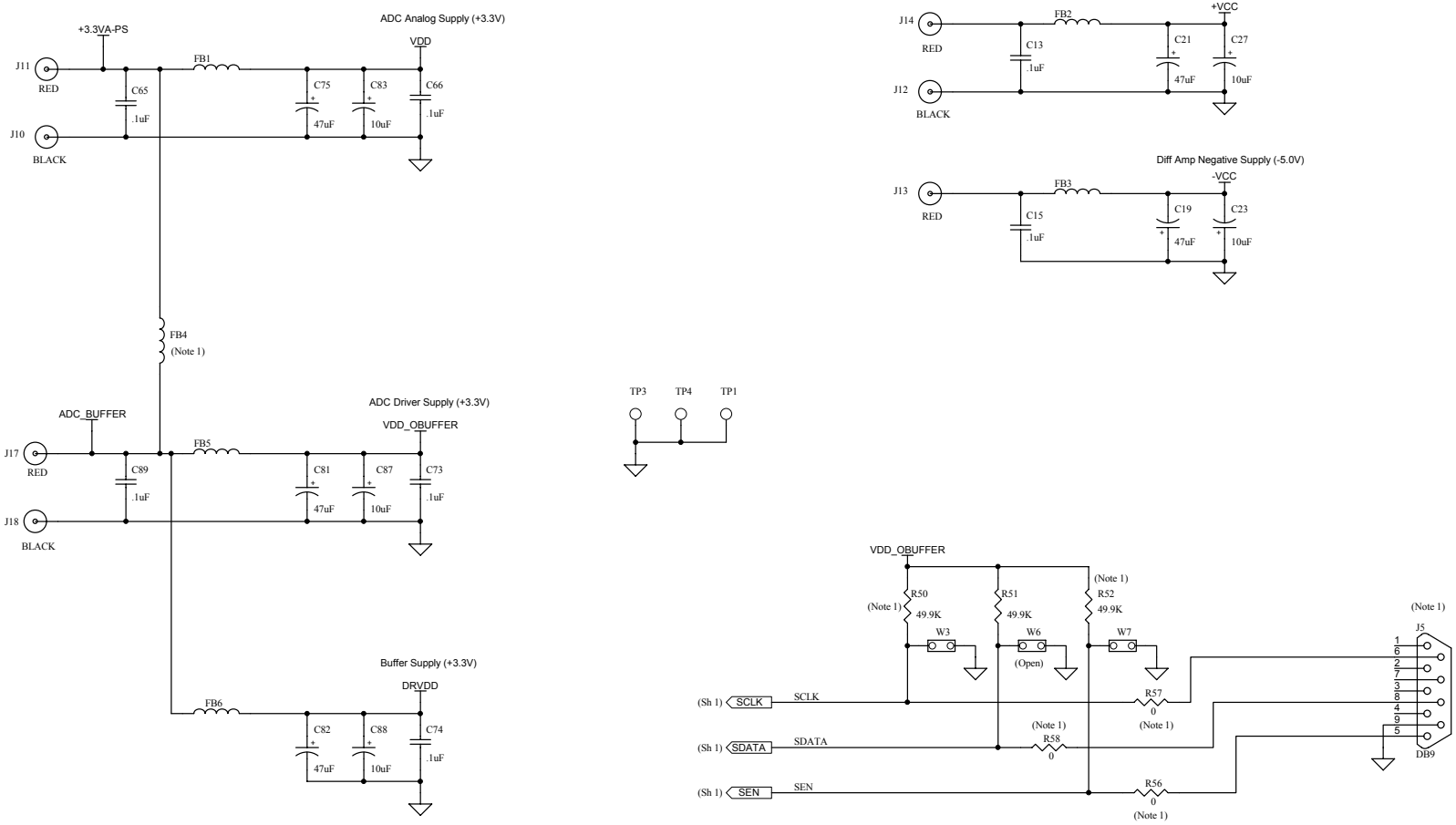

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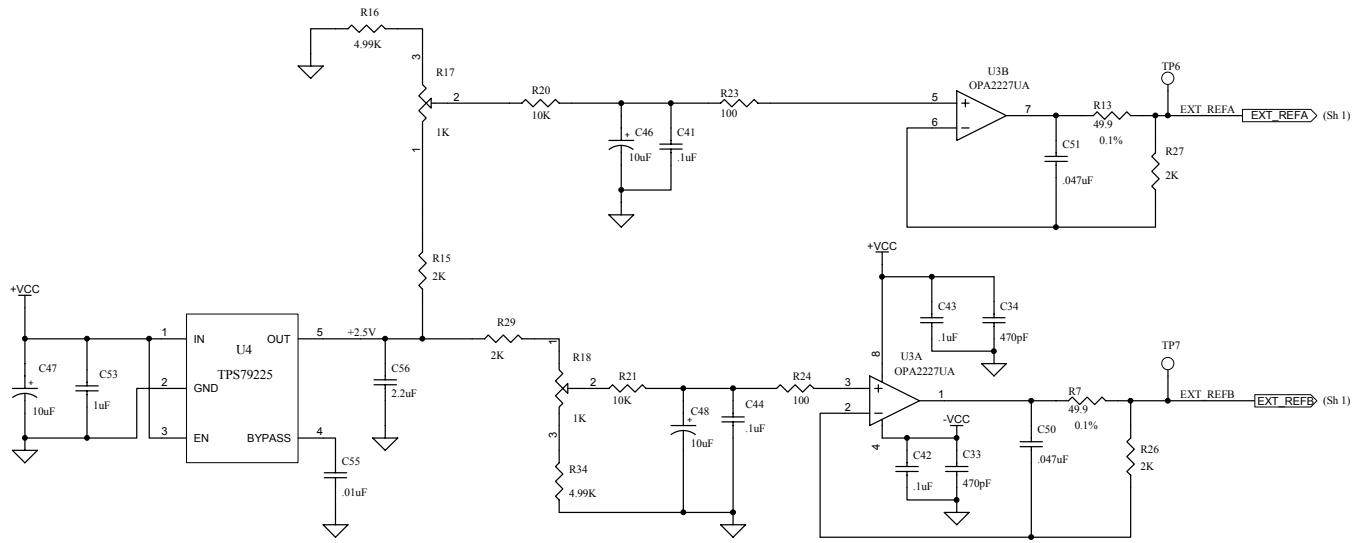

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