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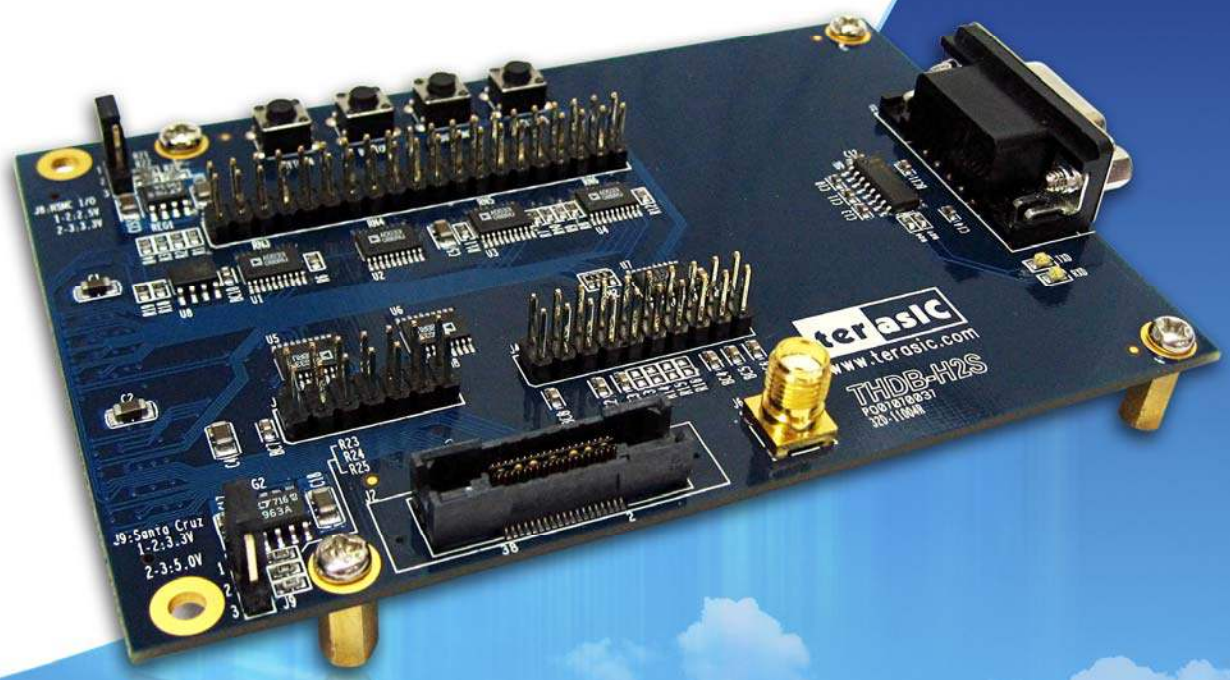
THDB-H2S

Terasic HSMC to Santa Cruz Daughter Board

User Manual



Document Version 0.1 AUG. 15, 2007 by Terasic

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CHAPTER 1 Introduction

THDB-H2S is an adapter board for converting High Speed Mezzanine Card (HSMC) connector to Santa Cruz (SC) interface which allows users to use the SC interface boards on a board with a HSMC connector. Also, the source signals form the HSMC connector to the SC header on the THDB-H2S board pass through level shifters to adjust the logic level difference between the HSMC and SC interface board.

Features

Figure 1.1 shows the photo of the THDB-H2S board. The important features are listed below:

- HSMC and Santa Cruz interface conversion
- Adjustable logic levels between HSMC and SC interface signals
- One Mictor Connector for logic analyzer debug interface
- One SMA Connector for external clock input
- One DB9 Connector for RS232 serial I/O interface
- Four Push buttons for general user-interface

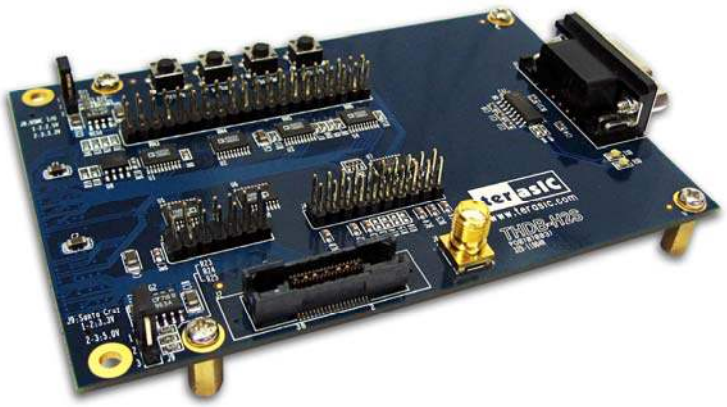

Figure 1.1. The THDB-H2S board

Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000

CHAPTER 2 Architecture

This chapter describes the architecture of the THDB-H2S board including its PCB and block diagram.

Layout and Componets

The picture of the TDRB-H2S board is shown in Figure 2.1 and Figure 2.2. It depicts the layout of the board and indicates the location of the connectors and key components.

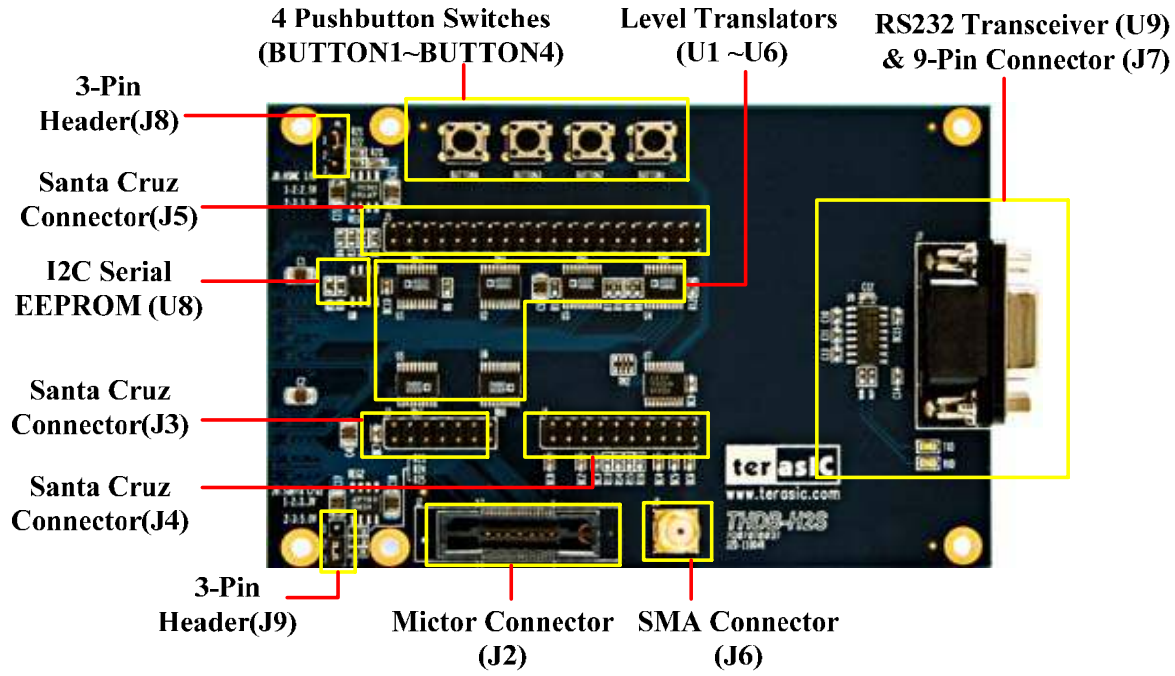

Figure 2.1 The TDRB-H2S PCB and Component diagram

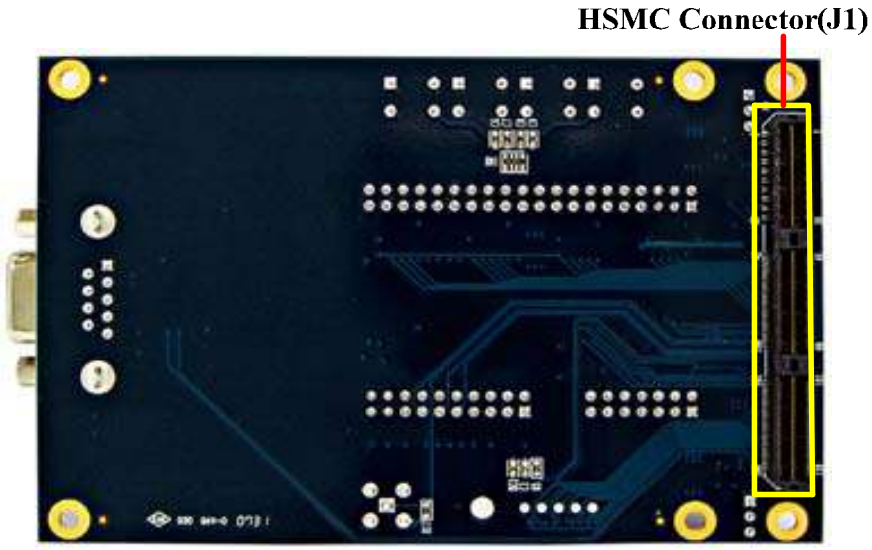

Figure 2.2 The TDRB-H2S Back side – HSMC connector view

The following components are provided on the THDB-H2S board :

- HSMC expansion connector (J1)
- Santa Cruz Headers(J3,J4,J5)
- Mictor connector (J2)
- SMA connector (J6)
- 9-pin connector (J7) and RS232 Transceiver (U9)
- 4 Push buttons (BUTTON1~BUTTON4)
- Logic level configuration headers (J8,J9)
- I2C serial EEPROM (U8)
- Level translator (U1~U6)

Block Diagram

Figure 2.3 shows the block diagram of the THDB-H2S board

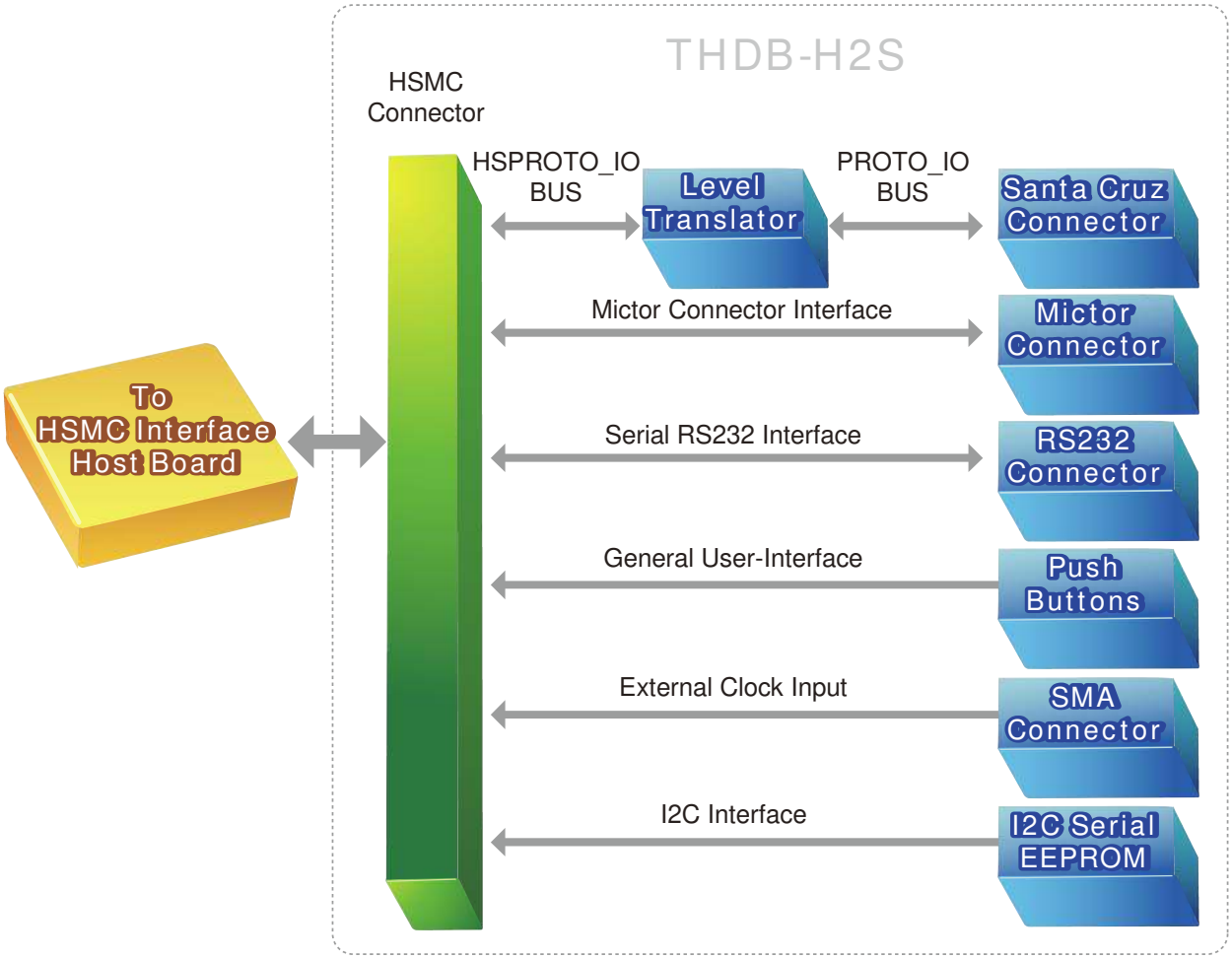

Figure 2.3. The block diagram of the THDB-H2S board

CHAPTER 3 Board Components

This section will describe the detailed information of the components, connector interfaces, and the pin mapping tables of the THDB-H2S board

The HSMC Connector

This section describes the HSMC connector on the THDB-H2S board

THDB-H2S board contains an Altera standard HSMC connector. All the other connector interfaces on the THDB-H2S board are connected to the HSMC connector. Figure 3.1, Figure 3.2, and Figure 3.3 show the pin-outs of the HSMC connector.

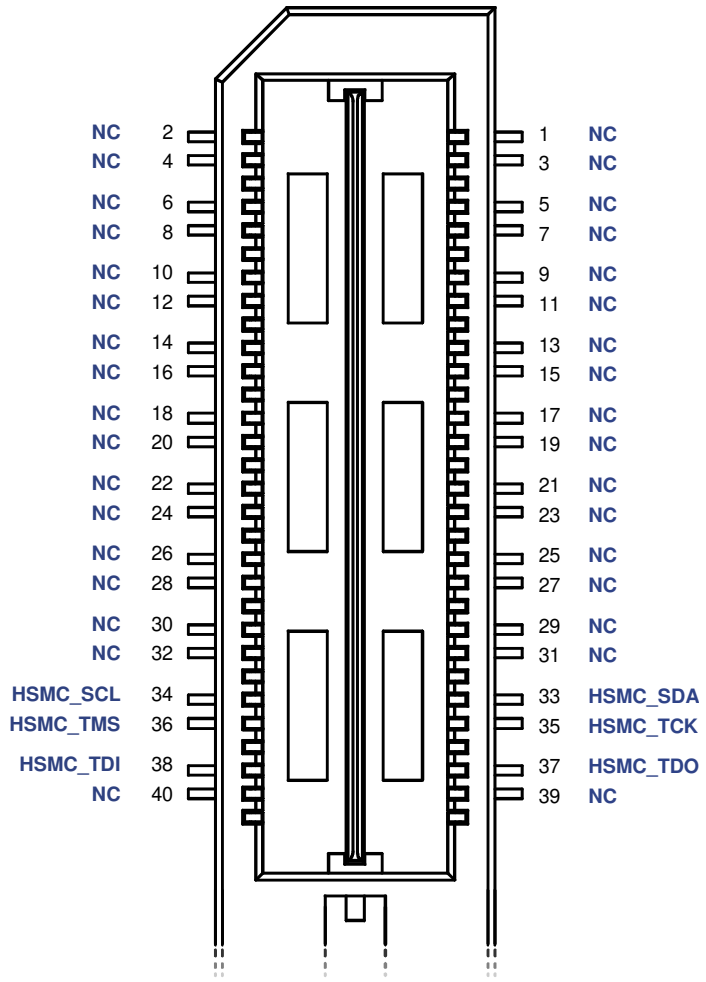

Figure 3.1 The pin-outs of Bank 1 on the HSMC connector

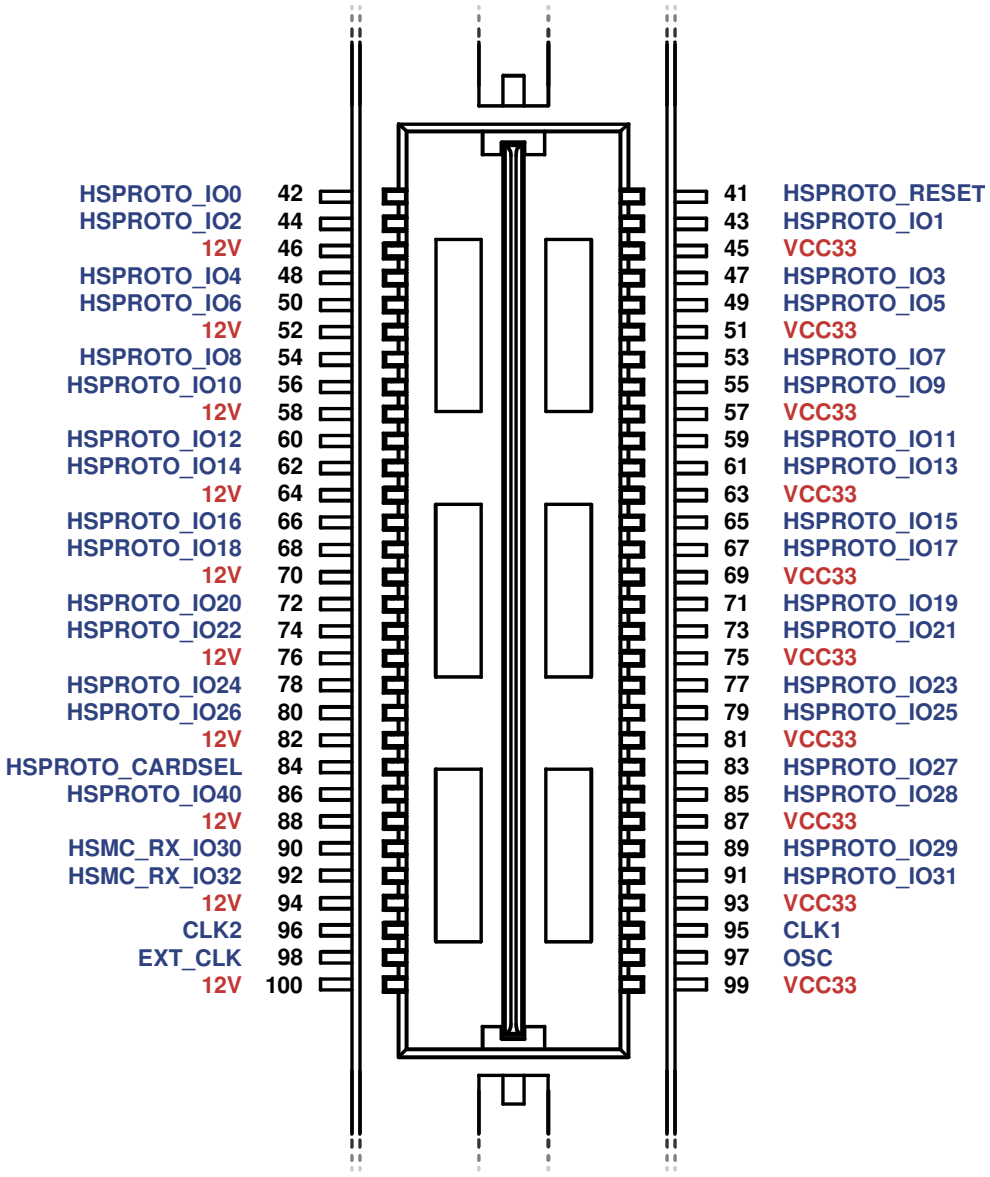

Figure 3.2 The pin-outs of Bank 2 of the HSMC connector.

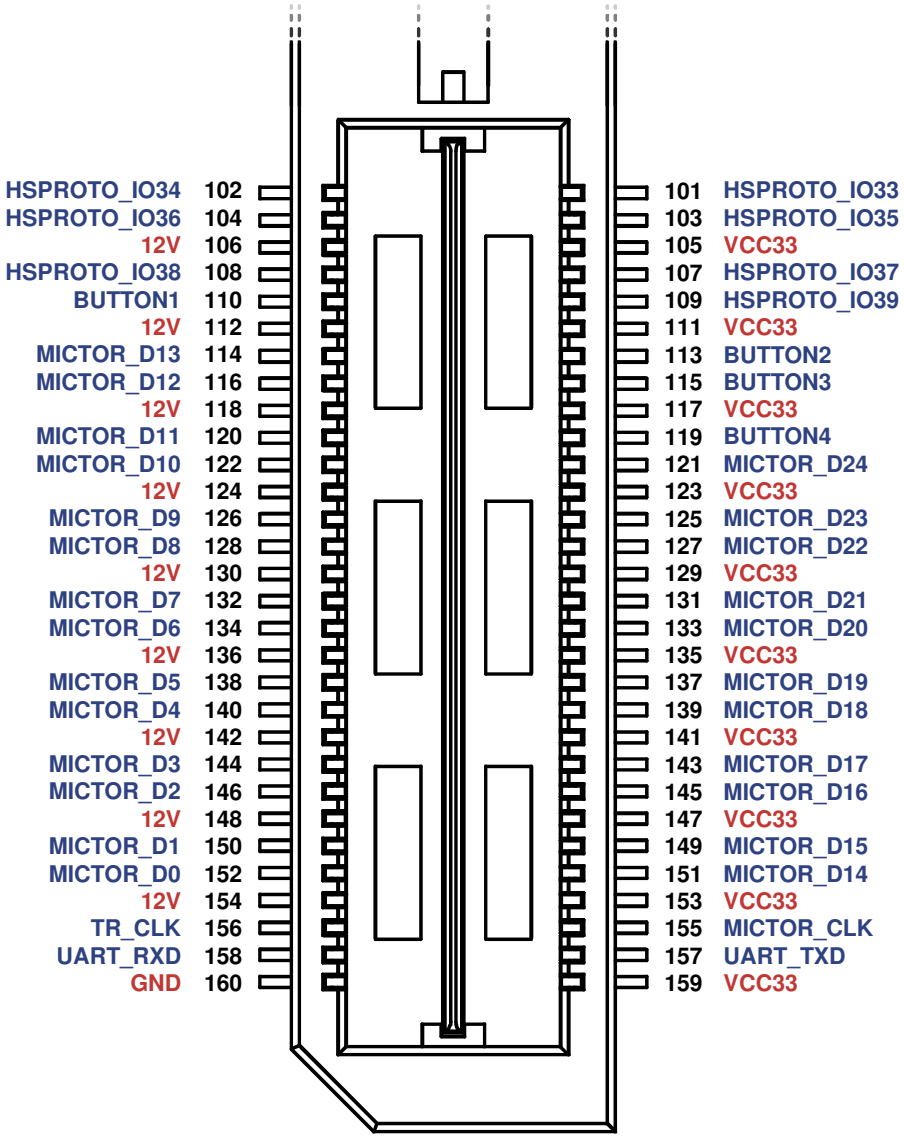

Figure 3.3 The pin-outs of Bank 3 of the HSMC connector

Level Translators and Configuration Headers

This section describes how to use the level translators and configuration headers on the THDB-H2S board

The level translators of the THDB-H2S board convert the signal levels between the HSMC and Santa Cruz connectors according to the configurations of the headers (J8, J9). Figure 3.4 shows the block diagram of such function. Table 3.1 and Table 3.2 list the configurations of the HSPROTO_IO BUS and the PROTO_IO BUS, respectively

The voltage level of the HSPROTO_IO BUS is controlled by VHSMC(VCCA pin); the voltage level of the PROTO_IO_BUS is controlled by VSC(VCCB pin), as shown in Figure 3.4. Therefore, Shorting Pin 1 and Pin 2 of J8 provides 2.5V to HSPROTO_IO BUS. Alternatively, shorting Pin 2 and Pin 3 of the J8 provides 3.3V to the HSPROTO_IO BUS. Similarly shorting Pin 1 and Pin 2 of J9 provides 3.3V to the PROTO_IO BUS. Shorting Pin 2 and Pin 3 provides 5V to the PROTO_IO BUS.

Note:

1. **Headers J8 and J9 must be configured with jumpers. If the pin1, pin2, and pin3 are opened at the same time, the level translator will NOT work.**
2. **Because of the characteristic of the level translators, the data rate of the HSPROTO_IO and PROTO_IO bus should be under 50 Mbps.**

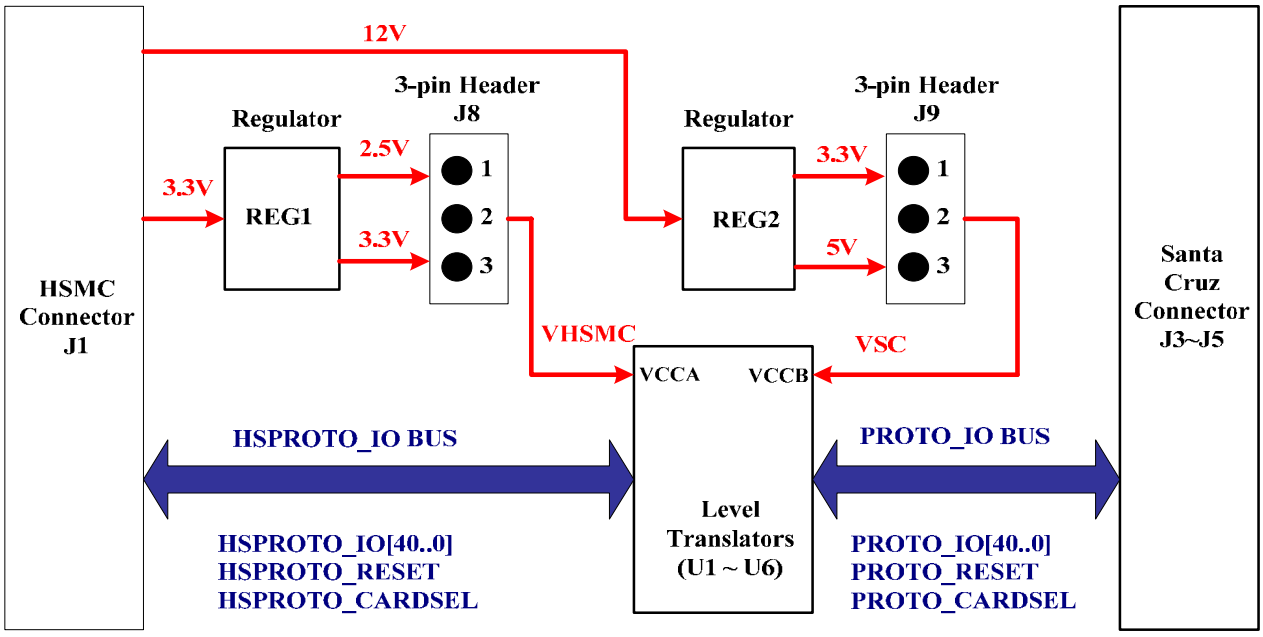

Figure 3.4 The diagram of the voltage-controlling circuit block

Table 3.1 The configuration of the logic level on the HSPROTO_IO BUS

Configuration of J8	Logic level of the HSPROTO_IO BUS
Short pins 1 and 2	2.5 volts
Short pins 2 and 3	3.3 volts

Table 3.2 The configuration of the logic level on the PROTO_IO BUS

Configuration of J9	Logic level of the PROTO_IO BUS
Short pins 1 and 2	3.3 volts
Short pins 2 and 3	5 volts

Santa Cruz Connector

This section describes the Santa Cruz connector on the THDB-H2S board

The THDB-H2S board comes with Santa Cruz connectors (J3, J4 and J5) to connect to a daughter board with Santa Cruz interface. Figure 3.5 shows the pin-outs of the Santa Cruz connector. Detailed pin mappings between J3, J4, and J5 to the HSMC connector is listed in Table 3.3, Table 3.4, and Table 3.5, respectively.

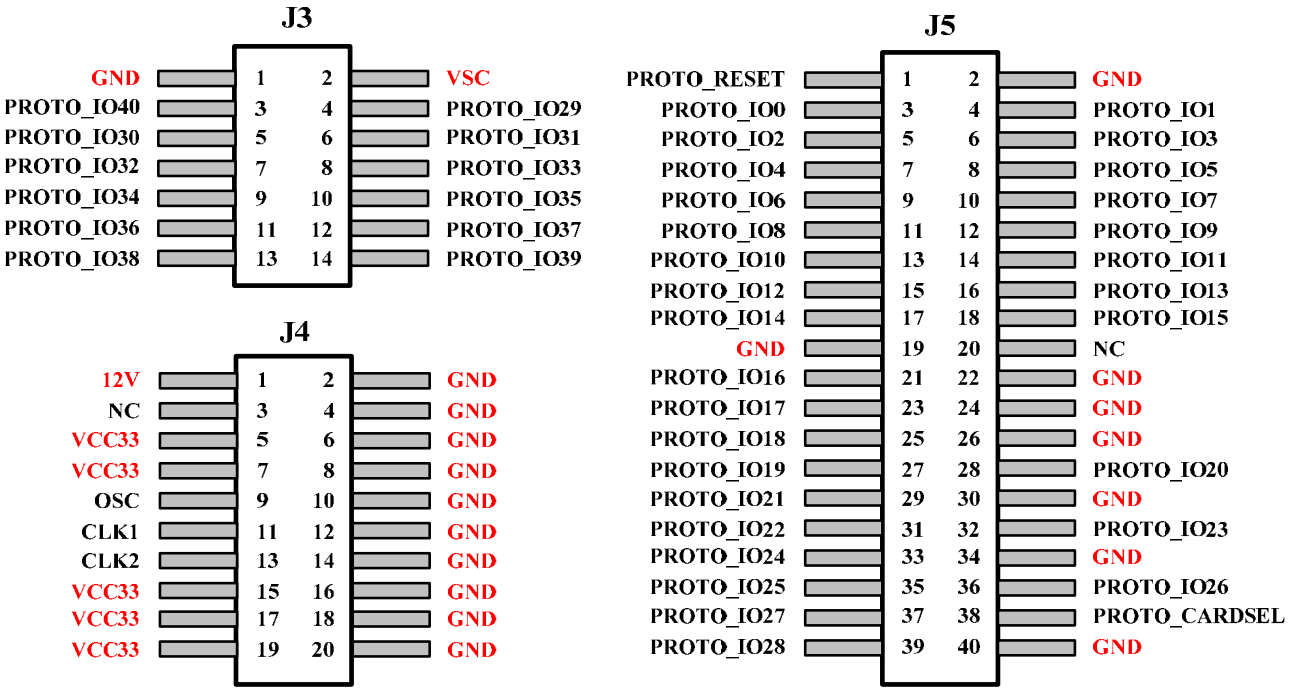

Figure 3.5 Santa Cruz connector pin-outs

Table 3.3 The pin assignments of the Santa Cruz connector J3

Santa Cruz connector J3			
SC Pin Number	**SC Signal Name**	**HSMC Pin Number**	**HSMC Pin Signal Name**
3	**PROTO_IO40**	**86**	**HSPROTO_IO40**
4	**PROTO_IO29**	**89**	**HSPROTO_IO29**
5	**PROTO_IO30**	**90**	**HSPROTO_IO30**
6	**PROTO_IO31**	**91**	**HSPROTO_IO31**
7	**PROTO_IO32**	**92**	**HSPROTO_IO32**
8	**PROTO_IO33**	**101**	**HSPROTO_IO33**
9	**PROTO_IO34**	**102**	**HSPROTO_IO34**
10	**PROTO_IO35**	**103**	**HSPROTO_IO35**
11	**PROTO_IO36**	**104**	**HSPROTO_IO36**
12	**PROTO_IO37**	**107**	**HSPROTO_IO37**
13	**PROTO_IO38**	**108**	**HSPROTO_IO38**
14	**PROTO_IO39**	**109**	**HSPROTO_IO39**

Table 3.4 The pin assignments of the Santa Cruz connector J4

Santa Cruz connector J4			
SC Pin Number	**SC Signal Name**	**HSMC Pin Number**	**HSMC Pin Signal Name**
9	**OSC**	**97**	**OSC**
11	**CLK1**	**95**	**CLK1**
13	**CLK2**	**96**	**CLK2**

Table 3.5 The pin assignments of the Santa Cruz connector J5

Santa Cruz connector J5			
SC Pin Number	**SC Signal Name**	**HSMC Pin Number**	**HSMC Pin Signal Name**
1	**PROTO_RESET**	**41**	**HSPROTO_RESET**
3	**PROTO_IO0**	**42**	**HSPROTO_IO0**
4	**PROTO_IO1**	**43**	**HSPROTO_IO1**
5	**PROTO_IO2**	**44**	**HSPROTO_IO2**
6	**PROTO_IO3**	**47**	**HSPROTO_IO3**
7	**PROTO_IO4**	**48**	**HSPROTO_IO4**
8	**PROTO_IO5**	**49**	**HSPROTO_IO5**
9	**PROTO_IO6**	**50**	**HSPROTO_IO6**

10	PROTO_IO7	53	HSPROTO_IO7
11	PROTO_IO8	54	HSPROTO_IO8
12	PROTO_IO9	55	HSPROTO_IO9
13	PROTO_IO10	56	HSPROTO_IO10
14	PROTO_IO11	59	HSPROTO_IO11
15	PROTO_IO12	60	HSPROTO_IO12
16	PROTO_IO13	61	HSPROTO_IO13
17	PROTO_IO14	62	HSPROTO_IO14
18	PROTO_IO15	65	HSPROTO_IO15
21	PROTO_IO16	66	HSPROTO_IO16
23	PROTO_IO17	67	HSPROTO_IO17
25	PROTO_IO18	68	HSPROTO_IO18
27	PROTO_IO19	71	HSPROTO_IO19
28	PROTO_IO20	72	HSPROTO_IO20
29	PROTO_IO21	73	HSPROTO_IO21
31	PROTO_IO22	74	HSPROTO_IO22
32	PROTO_IO23	77	HSPROTO_IO23
33	PROTO_IO24	78	HSPROTO_IO24
35	PROTO_IO25	79	HSPROTO_IO25
36	PROTO_IO26	80	HSPROTO_IO26
37	PROTO_IO27	83	HSPROTO_IO27
38	PROTO_CARDSEL	84	HSPROTO_CARDSEL
39	PROTO_IO28	85	HSPROTO_IO28

Mictor Connector

This section describes how to use the Mictor connector on the THDB-H2S board

The Mictor connector (J2) can be used for logic analysis on the HSMC-interfaced host board by connecting an external scope or a logic analyzer to it. Figure 3.6 shows the pin-outs of the Mictor connector. Table 3.6 shows the detailed pin mappings between the Mictor connector and the HSMC connector.

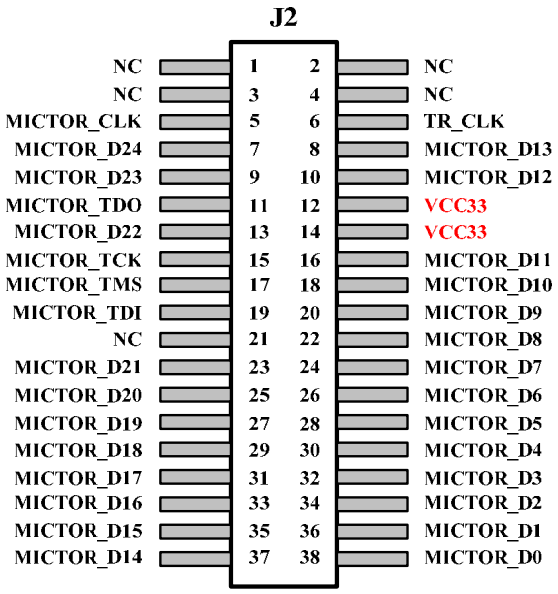

Figure 3.6 Mictor connector pin-outs

Table 3.6 The pin assignments of the Mictor connector (J2)

Mictor Connector Pin Number	Mictor Connector Signal Name	HSMC Pin Number
5	MICTOR_CLK	155
6	TR_CLK	156
7	MICTOR_D24	121
8	MICTOR_ D13	114
9	MICTOR_ D23	125
10	MICTOR_ D12	116
11	MICTOR_TDO	37
13	MICTOR_D22	127
15	MICTOR_TCK	35
16	MICTOR_D11	120
17	MICTOR_TMS	36
18	MICTOR_D10	122
19	MICTOR _TDI	38
20	MICTOR _D9	126
22	MICTOR _D8	128
23	MICTOR _D21	131
24	MICTOR _D7	132
25	MICTOR _D20	133
26	MICTOR _D6	134
27	MICTOR _D19	137
28	MICTOR _D5	138

29	MICTOR _D18	139
30	MICTOR _D4	140
31	MICTOR _D17	143
32	MICTOR _D3	144
33	MICTOR _D16	145
34	MICTOR _D2	146
35	MICTOR _D15	149
36	MICTOR _D1	150
37	MICTOR _D14	151
38	MICTOR _D0	152

To use this interface, user needs to configure the JTAG interface on the HSMC interface host board. For example, the steps of controlling the Cyclone III start board using Mictor interface is shown below:

1. Connecting the THDB-H2S board to the Cyclone III Start Board.
2. Removing the jumpers of JP1 and JP2 of the Cyclone III Start Board to connect the JTAG interface between Cyclone III FPGA and the THDB-H2S board.
3. Short the TDI and TDO pins of the JTAG connector(J4), as shown in Figure 3.7
4. Disable the built-in USB blaster by shorting JP8 on the Cyclone III Starter Board

The above FOUR steps will make a closed JTAG chain as shown in Figure 3.8

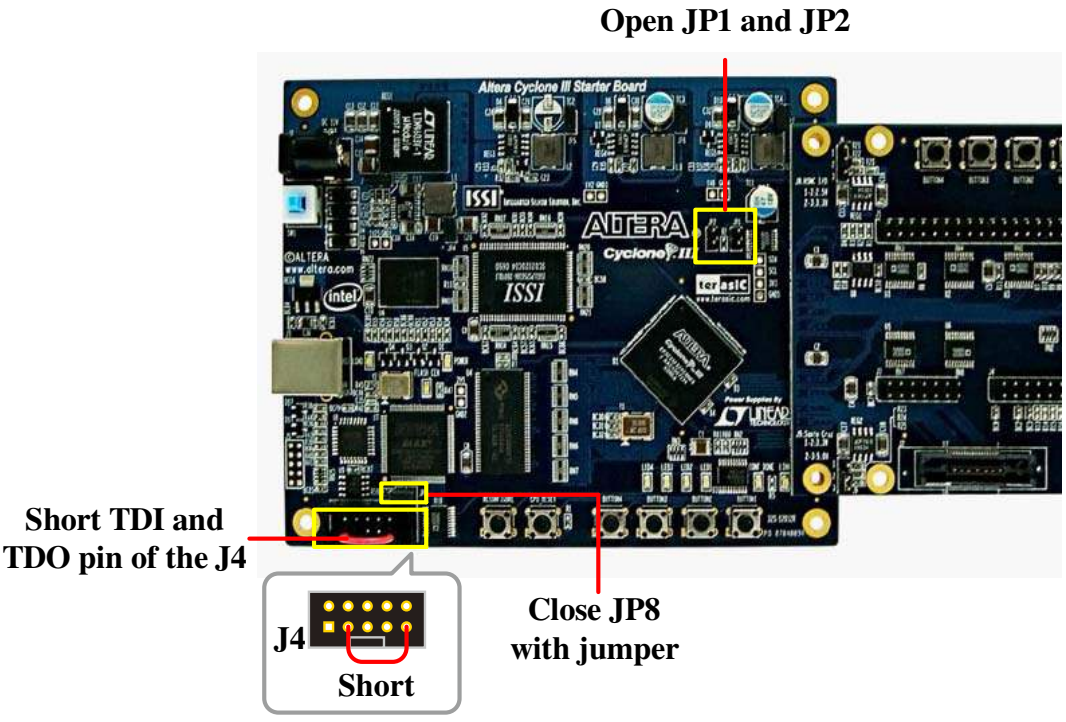

Figure 3.7 The configuration of the Cyclone III start board for controlling the JTAG chain using the Mictor connector

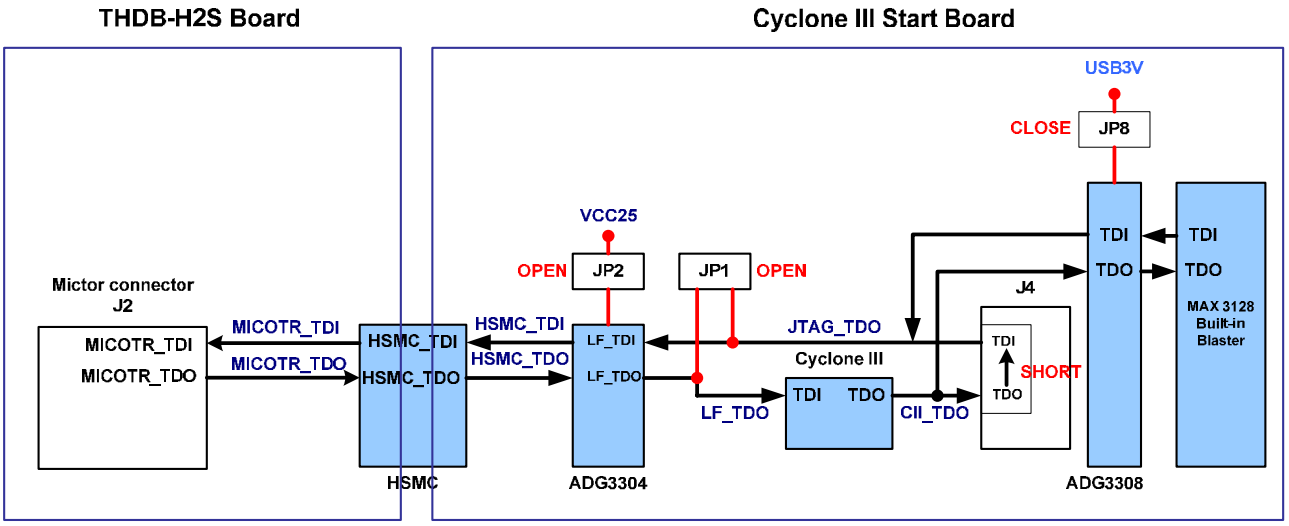

Figure 3.8 The JTAG chain between the THDB-H2S board and Cyclone III Start Board

RS232 Transceiver and the 9-Pin Connector

This section describes the RS232 Transceiver and 9-Pin Connector on the THDB-H2S board

The THDB-H2S is equipped with a RS232 transceiver (U9) and a 9-pin connector (J7) to provide RS232 serial I/O interface to the HSMC interface host board. The pin assignments of the RS232 interface are shown in Table3.7.

Table 3.7 The pin assignments of the RS232 interface

RS232 Transceiver Pin Number	RS232 Transceiver Signal Name	HSMC Pin Number
U9-11	UART_TXD	157
U9-12	UART_RXD	158

SMA Connector

This section describes the SMA connector on the THDB-H2S board

The THDB-H2S board provides a SMA connector (J6) for external clock input. The pin assignments of the SMA connector are shown in table 3.8.

Table 3.8 The pin assignments of the SMA connector

SMA	SMA	HSMC Pin

Connector Pin Number	Connector Signal Name	Number
J6-1	EXT_CLK	98

I2C Serial EEPROM

This section describes the I2C Serial EEPROM on the THDB-H2S board

The THDB-H2S board provides an EEPROM (U8) which can be configured by the I2C interface. The size of the EEPROM is 128 bit that can store the board information or user's data. The detailed pin description between EEPROM and HSMC connector is listed in the Table 3.9.

Table 3.9 The pin assignments of the I2C serial EEPROM

EEPROM Pin Number	EPPROM Signal Name	HSMC Pin Number
U8-5	HSMC_SDA	33
U8-6	HSMC_SCL	34

Power Supply

This section describes the power supply on the THDB-H2S board

The power distribution on the THDB-H2S board is shown in Figure 3.9.

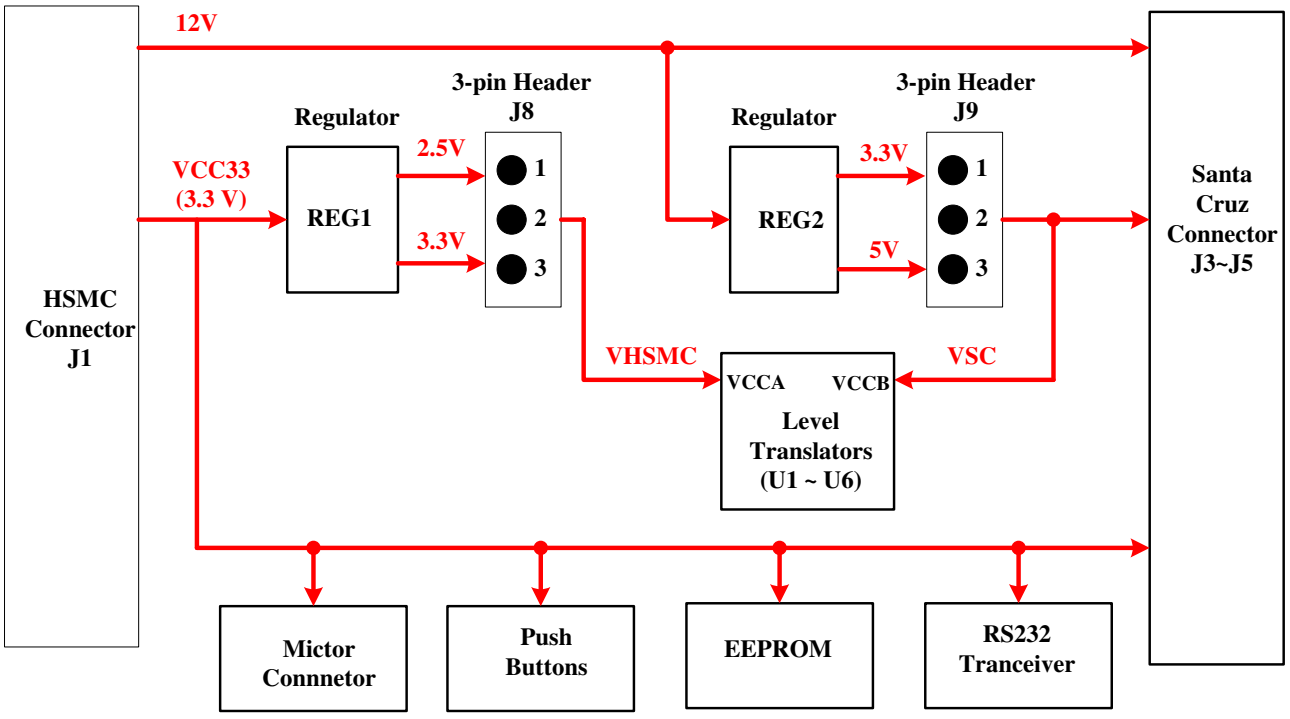

Figure 3.9 THDB-H2S board power distribution diagram.

CHAPTER 4 Demonstration

This chapter illustrates how to connect the THDB-H2S board to a HSMC interface host board using a Cyclone III Starter Board as an example

Connecting THDB-H2S Board to Cyclone III Start Board

This section describes how to use THD-H2S board the Cyclone III start board and what users need to know during the operation

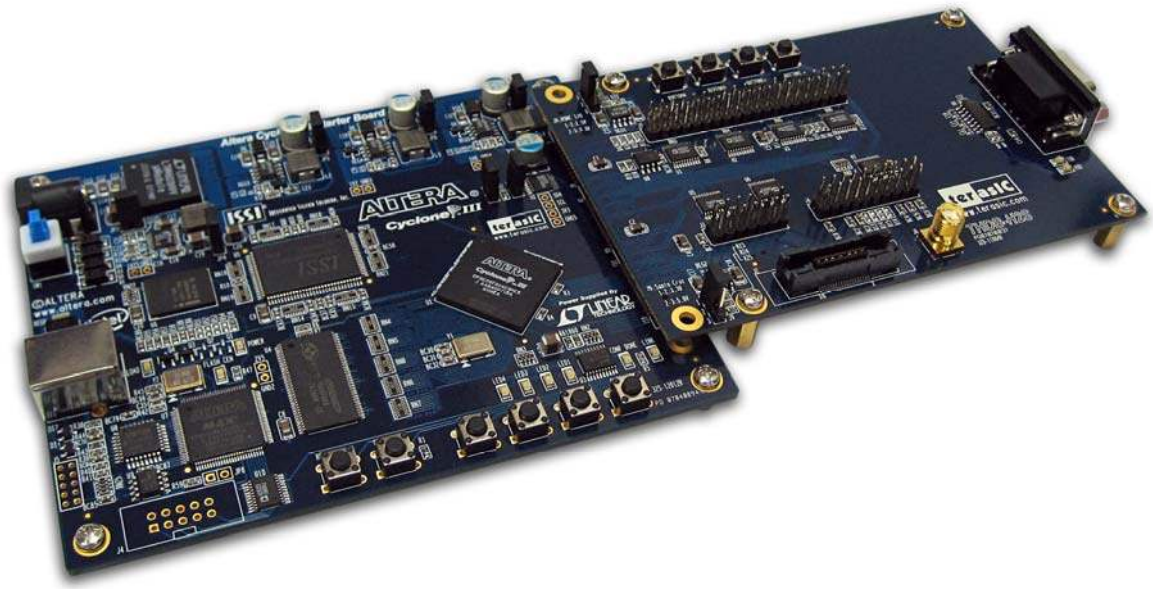

Figure 4.1 Connecting the THDB-H2S board to the Cyclone III start board

To correctly operate the THDB-H2G board with the Cyclone III start board, users need to pay attention to the following notes:

1. Observe the orientation of the HSMC connector when connecting the THDB-H2S to the Cyclone III Starter Board.
2. Users **MUST** short Pin 1 and Pin 2 of the J8 on the THDB-H2S to force the voltage level to 2.5V to match the 2.5V IO pins of the Cyclone III board.
3. Configure J9 of the THDB-H2S according to the logic level of the Santa Cruz daughter board (refer to Table 3.2)
4. Please note that there are two LVDS pairs on the HSMC connector: the HSMC_CLK_p1/n1 (form a close loop via R3) and HSMC_CLKIN_p2/n2 (form a close loop via R4). Therefore, using any one of the signal in a LVDS pair under single-ended mode will prevent users from using the other signal in the same pair.

CHAPTER 5 Appendix

Revision History

Date	Change Log
AUG 15, 2007	Initial Version

Always Visit THDB-H2S Webpage for New Main board

We will be continuing providing interesting examples and labs on our THDB-H2S webpage. Please visit www.altera.com or h2s.terasic.com for more information.