



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ. @ V_{GS} = -4.5V, T_A = +25°C)

BV _{DSS}	R _{DS(ON)}	Qg	Q_{gd}	I _D
-8V	8.2mΩ	8.1nC	1.8nC	-10A

Description

This 3rd generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high-efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R_{DS(ON)} per footprint area.

Applications

- **DC-DC Converters**
- **Battery Management**
- Load Switch

Features

- LD-MOS Technology with the Lowest Figure of Merit: $-R_{DS(ON)} = 8.2m\Omega$ to Minimize On-State Losses
 - -Q_q = 8.1nC for Ultra-Fast Switching
- V_{GS(th)} = -0.8V Typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm x 1.5mm
- Height = 0.60mm for Low Profile
- ESD = 6kV HBM Protection of Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

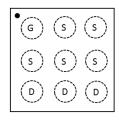
Mechanical Data

Case: U-WLB1515-9

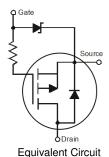
Terminal Connections: See Diagram Below

U-WLB1515-9 (Type B)





Top View Pin Configuration



Ordering Information (Note 4)

	Part Number	Case	Packaging			
	DMP1011UCB9-7	U-WLB1515-9 (Type B)	3,000/Tape & Reel			
Notes:	1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.					

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- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-WLB1515-9 (Type B)



NX = Product Type Marking Code YM = Date Code Marking Y or \overline{Y} = Year (ex: G = 2019) M or \overline{M} = Month (ex: 9 = September)

Date Code Key

Year	2012		2013	2014		2015	2016		2017	2018		2019
Code	Z		Α	В		С	D		Е	F		G
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Au	g Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Drain-Source Voltage		V_{DSS}	-8	V	
Gate-Source Voltage		V _{GSS}	-6	V	
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I _D	-10 -8	А
Continuous Drain Current (Note 6) V _{GS} = -4.5V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I _D	-7.4 -6.0	Α
Pulsed Drain Current (Pulse Duration 10µs, Duty C	ycle ≤1%)	I _{DM}	-50	Α	
Continuous Source Pin Current (Note 6)		Is	-2	Α	
Pulsed Source Pin Current (Pulse Duration 10µs, D	outy Cycle:	Ism	-15	Α	
Continuous Gate Current			I _G	-0.5	Α

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P _D	0.89	W
Total Power Dissipation (Note 6)	P _D	1.57	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{0JA}	142.1	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R _{0JA}	80.5	°C/W
Operating and Storage Temperature Range	$T_{J_i} T_{STG}$	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

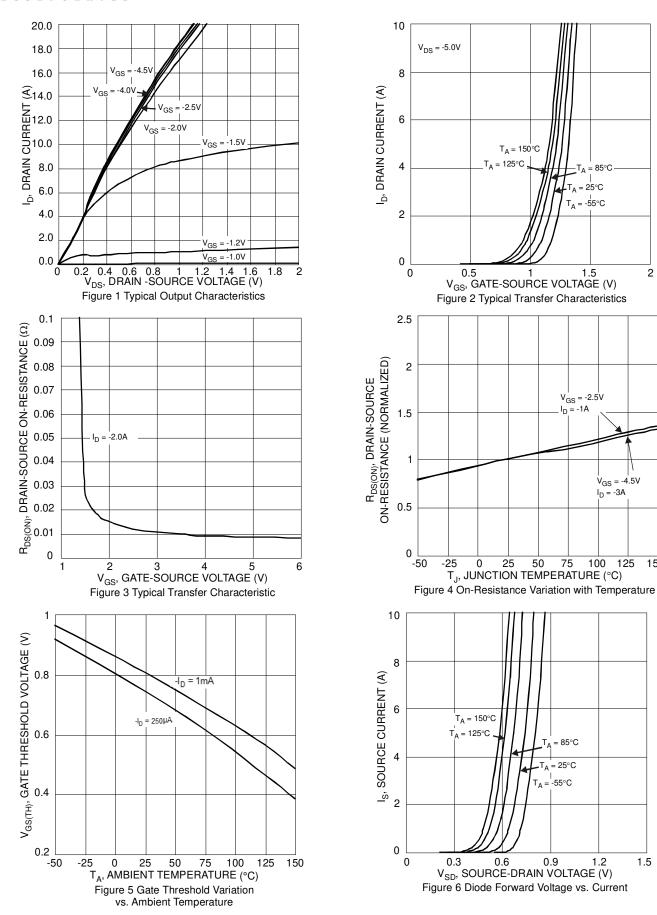
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)		·	-			
Drain-Source Breakdown Voltage	BV _{DSS}	-8	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$
Gate to Source Voltage	BV _{SGS}	6	_		V	$V_{DS} = 0V, I_S = 250\mu A$
Zero Gate Voltage Drain Current $@T_C = +25^{\circ}C$	I _{DSS}	_		-1	μA	$V_{DS} = -4.0V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	_	-100	nA	$V_{GS} = -4.0V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)	•				•	•
Gate Threshold Voltage	V _{GS(TH)}	-0.4	-0.8	-1.1	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
			8.2	10		$V_{GS} = -4.5V, I_D = -2A$
Static Drain-Source On-Resistance	R _{DS(ON)}	_	10	13	mΩ	$V_{GS} = -3.0V, I_D = -2A$
			11	14		$V_{GS} = -2.5V, I_D = -2A$
Forward Transfer Admittance	Y _{fs}	_	16.8	_	S	$V_{DS} = -4V, I_{D} = -2A$
Diode Forward Voltage (Note 6)	V_{SD}	_	-0.7	-1	V	$V_{GS} = 0V, I_{S} = -2A$
Reverse Recovery Charge	Q _{RR}	_	6.3	_	nC	$V_{DD} = -5V, I_F = -2A,$
Reverse Recovery Time	t _{RR}	_	18.5	_	ns	di/dt = 200A/µs
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	_	817	1,060	pF	\\ \ \ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\
Output Capacitance	Coss	_	595	770	pF	$V_{DS} = -4V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	269	350	pF	1 = 1.0IVII IZ
Series Gate Resistance	R_{G}	_	1.9	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge	Qg	_	8.1	10.5	nC	
Gate-Source Charge	Q _{gs}	_	0.9	_	nC	$V_{GS} = -4.5V, V_{DS} = -4V,$
Gate-Drain Charge	Q _{gd}	_	1.8	_	nC	$I_D = -2A$
Turn-On Delay Time	t _{D(ON)}	_	6.2	10	ns	
Turn-On Rise Time	t _R	_	22.6	_	ns	$V_{DD} = -4V$, $V_{GS} = -4.5V$,
Turn-Off Delay Time	t _{D(OFF)}	_	30.1	48	ns	$I_{DS} = -2A$, $R_G = 10\Omega$
Turn-Off Fall Time	t _F	_	22.7	_	ns	

Notes:

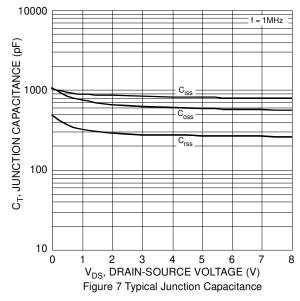
- 5. Device mounted on FR-4 PCB with minimum recommended pad layout. 6. Device mounted on FR-4 material with 1-inch² (6.45cm²), 2oz (0.071mm thick) Cu.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to production testing.

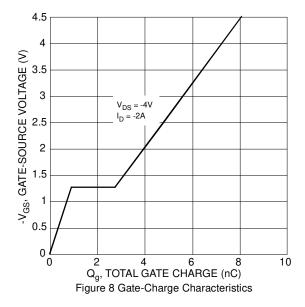
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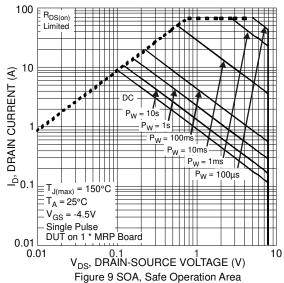


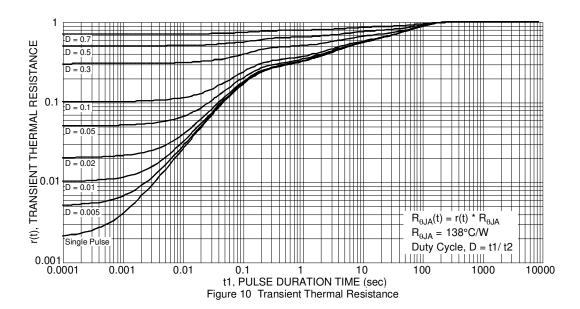










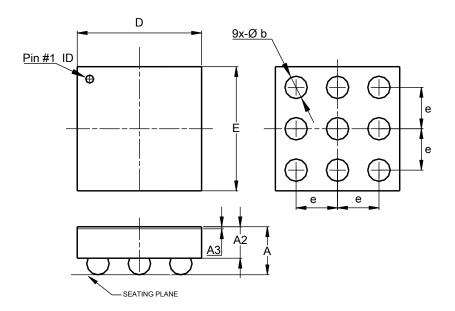




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1515-9 (Type B)

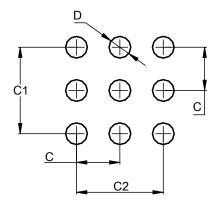


U-WLB1515-9 (Type B)							
Dim	Min	Max	Тур				
Α		0.60					
A2		0.36	0.36				
А3	0.020	0.030	0.025				
b	0.22	0.32	0.27				
D	1.47	1.50	1.49				
Е	1.47	1.50	1.49				
е			0.50				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1515-9 (Type B)



Dimensions	Value (in mm)
С	0.50
C1	1.00
C2	1.00
D	0.25



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