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FQT4N20L N-Channel QFET® MOSFET

200 V, 0.85 A, 1.40 Ω

Description

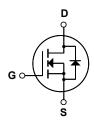
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



Features

- 0.85 A, 200 V, $R_{DS(on)}$ =1.35 $\Omega(Typ.)$ @ V_{GS} =10 V, I_{D} =0.425 A
- Low Gate Charge (Typ. 4 nC)
- Low C_{rss} (Typ. 6 pF)
- · 100% Avalanche Tested
- Low Level Gate Drive Requirments Allowing Direct Operation From Logic Drives





Absolute Maximum Ratings T_C = 25°C unless otherwise noted

G				
Symbol	Parameter		FQT4N20L	Unit
V_{DSS}	Drain-Source Voltage		200	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 70°C)		0.85	Α
			0.68	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	3.4	Α
V _{GSS}	Gate-Source Voltage		± 20	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	52	mJ
I _{AR}	Avalanche Current	(Note 1)	0.85	А
E _{AR}	Repetitive Avalanche Energy	(Note 1)	0.22	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns
P_D	Power Dissipation (T _C = 25°C)		2.2	W
	- Derate above 25°C		0.018	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C
'L			300	

Thermal Characteristics

Symbol	Parameter	Тур	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *		57	°C/W

^{*} When mounted on the minimum pad size recommended (PCB Mount)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	200			V
$\Delta B_{VDSS}/$ ΔT_{J}	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.16		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 200 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 160 V, T _C = 125°C	-		10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	-	-	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	-	-	-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.0	V
R _{DS(on)}	Static Drain-Source	V _{GS} = 10 V, I _D = 0.425 A		1.10	1.35	
DO(OII)	On-Resistance	V _{GS} = 5 V, I _D = 0.425 A		1.13	1.40	Ω
g _{FS}	Forward Transconductance	V _{DS} = 30 V, I _D = 0.425 A (Note 4)		1.42		S
C _{iss}	Input Capacitance Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		240 36	310 45	pF pF
C _{rss}	Reverse Transfer Capacitance	1 - 1.0 WINZ	-	6	8	pF
	ing Characteristics	T				
t _{d(on)}	Turn-On Delay Time	V _{DD} = 100 V, I _D = 3.8 A,	-	7	25	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		70	150	ns
	Turn-Off Delay Time			15	40	ns
	,	(Note 4. E)		40		
t _f	Turn-Off Fall Time	(Note 4, 5)			90	ns
t _f Q _g	Turn-Off Fall Time Total Gate Charge	V _{DS} = 160 V, I _D = 3.8 A,		4.0	5.2	nC
t _f Q _g Q _{gs}	Turn-Off Fall Time Total Gate Charge Gate-Source Charge	V _{DS} = 160 V, I _D = 3.8 A, V _{GS} = 5 V		1.0	5.2	nC nC
$t_{d(off)}$ t_{f} Q_{g} Q_{gs} Q_{gd}	Turn-Off Fall Time Total Gate Charge	V _{DS} = 160 V, I _D = 3.8 A,			5.2	nC
t _f Q _g Q _{gs} Q _{gd}	Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DS} = 160 \text{ V}, I_{D} = 3.8 \text{ A},$ $V_{GS} = 5 \text{ V}$ (Note 4, 5)		1.0	5.2	nC nC
t _f Q _g Q _{gs} Q _{gd} Drain-S	Turn-Off Fall Time Total Gate Charge Gate-Source Charge	V_{DS} = 160 V, I_{D} = 3.8 A, V_{GS} = 5 V (Note 4, 5)		1.0	5.2	nC nC
t _f Q _g Q _{gs} Q _{gd} Drain-S	Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge cource Diode Characteristics and	V _{DS} = 160 V, I _D = 3.8 A, V _{GS} = 5 V (Note 4, 5) and Maximum Ratings ode Forward Current	 	1.0	5.2	nC nC
$egin{array}{l} t_{f} & & & \\ Q_{g} & & & \\ Q_{gs} & & & \\ Q_{gd} & & & \\ \hline egin{array}{c} \textbf{Drain-S} & & \\ I_{SM} & & & \\ \hline \end{array}$	Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics at Maximum Continuous Drain-Source Dio	V _{DS} = 160 V, I _D = 3.8 A, V _{GS} = 5 V (Note 4, 5) and Maximum Ratings ode Forward Current		1.0	5.2 	nC nC nC
t _f Q _g Q _{gs} Q _{gd}	Turn-Off Fall Time Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics and Maximum Continuous Drain-Source Diode Faxing Maximum Pulsed Drain-Source Diode Faxing Times Total Times Time	V _{DS} = 160 V, I _D = 3.8 A, V _{GS} = 5 V (Note 4, 5) and Maximum Ratings de Forward Current Forward Current	 	1.0	5.2 0.85 3.4	nC nC nC

- $\label{eq:Notes:1} \begin{array}{ll} \textbf{Notes:} \\ \textbf{1.} \ \ \text{Repetitive Rating: Pulse width limited by maximum junction temperature} \\ \textbf{2.} \ \ \text{L} = \ \textbf{108mH, } \ \ \textbf{I}_{AS} = \textbf{0.85A}, \ \textbf{V}_{DD} = 50\text{V, } \ \textbf{R}_{G} = 25 \ \Omega, \ \textbf{Starting } \ \ \textbf{T}_{J} = 25^{\circ}\text{C} \\ \textbf{3.} \ \ \textbf{I}_{SD} \leq \textbf{3.8A}, \ \ \text{di/dt} \leq 300\text{A/µs, } \ \ \textbf{V}_{DD} \leq \text{BV}_{DSS, } \ \text{Starting } \ \ \textbf{T}_{J} = 25^{\circ}\text{C} \\ \textbf{4.} \ \ \text{Pulse Test: Pulse width} \leq 300\text{µs, } \ \text{Duty cycle} \leq 2\% \\ \textbf{5.} \ \ \ \text{Essentially independent of operating temperature} \end{array}$

Typical Characteristics

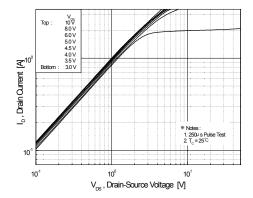


Figure 1. On-Region Characteristics

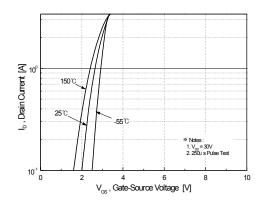


Figure 2. Transfer Characteristics

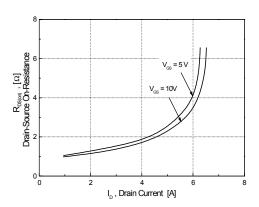


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

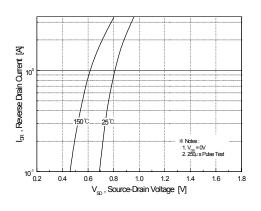


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

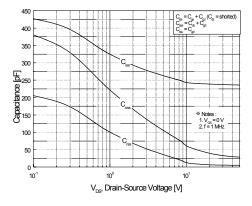


Figure 5. Capacitance Characteristics

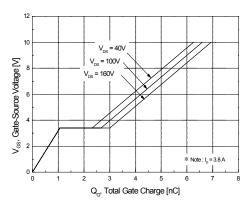


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

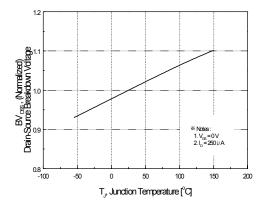
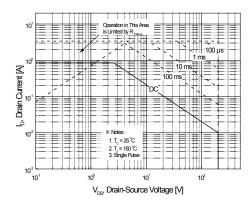


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



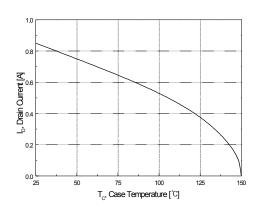


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

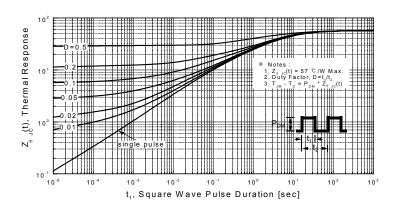
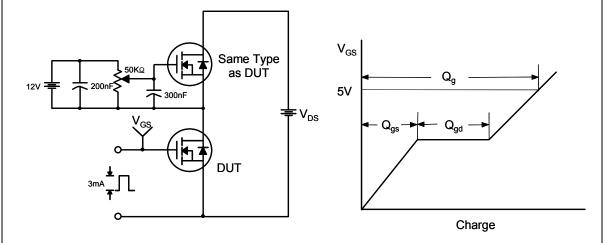
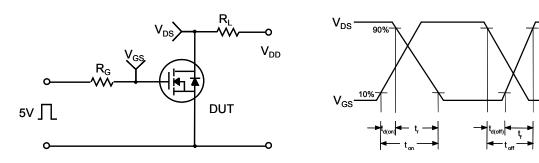


Figure 11. Transient Thermal Response Curve

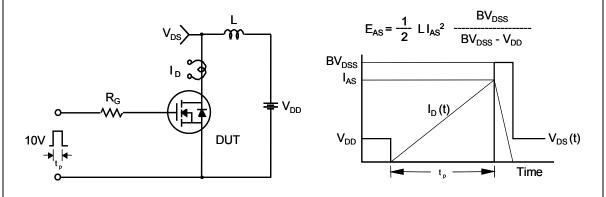
Gate Charge Test Circuit & Waveform

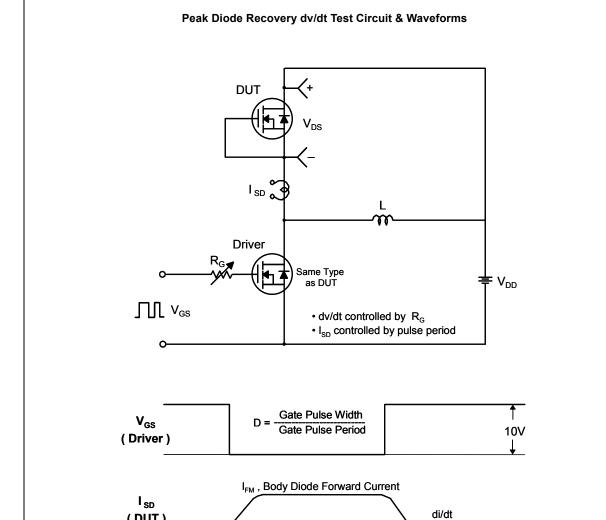


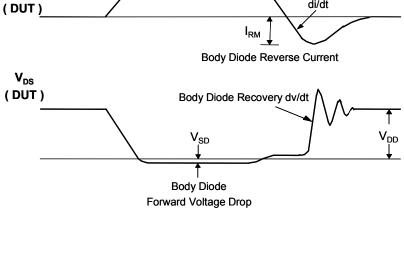
Resistive Switching Test Circuit & Waveforms

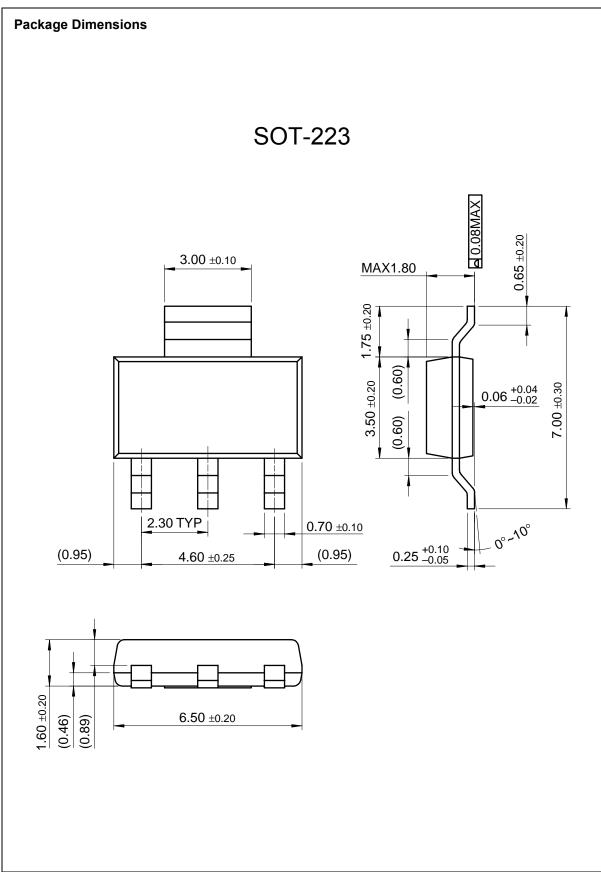


Unclamped Inductive Switching Test Circuit & Waveforms













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