32-Channel High Voltage Amplifier Array

Features

- 32 independent high voltage amplifiers
- Up to 250V output voltage
- 3.0V/µs typical output slew rate
- Very low operating current (typically 45µA per channel)
- High value internal feedback resistors
- Fixed gain of 50V/V
- Integrated silicon diode for temperature sensing

Applications

- MEMS (microelectromechanical systems) driver
- Piezoelectric transducer driver
- Optical crosspoint switches (using MEMS technology)

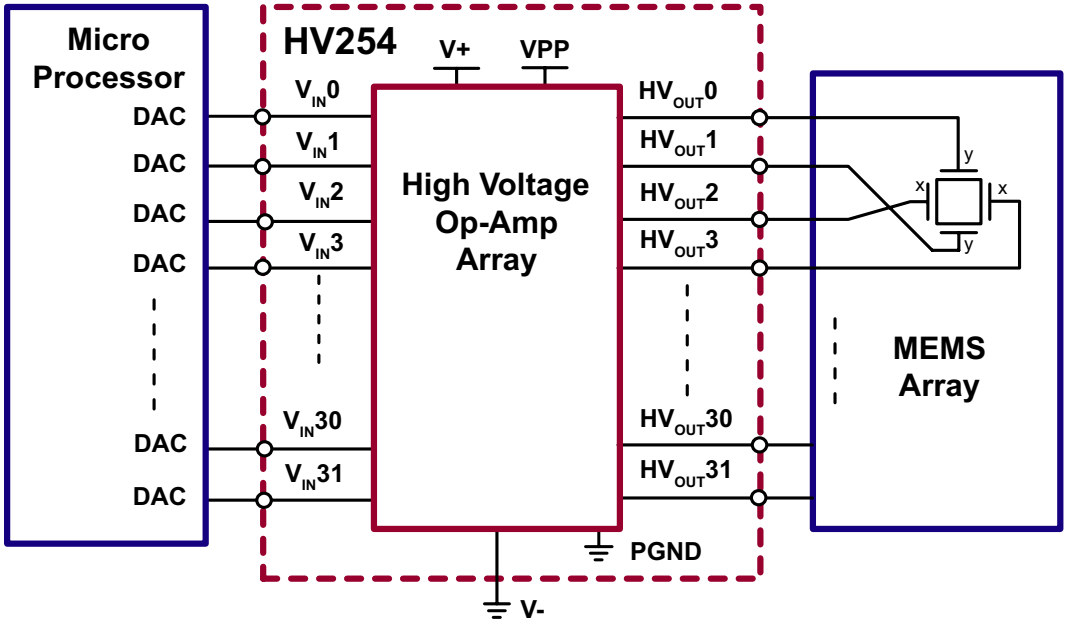
General Description

The Supertex HV254 is a 32-channel, high voltage, amplifier array integrated circuit. It operates on a 275V high voltage supply and two low voltage supplies: +5.0V and -5.0V. Each channel has its own input and output. An integrated diode is included to help monitor die temperature.

The input voltage can be from a DAC (Digital to Analog Converter) with a voltage range of 0V to the low voltage supply, V+. The output of the HV254 will swing from 7.0 to 250V. It cannot swing to ground. With the internal gain set at 50V/V, a minimum input signal of 140mV will still maintain linearity. Input voltages below 140mV can be applied without damage to the device. However, the amplifier will be saturated. Typical output load is equivalent to a 125MΩ resistor in parallel with a 100pF capacitor. The outputs have a guaranteed slew rate of at least 3.0V/µs. The internal closed loop gain is set at a nominal value of 34.0dB (50V/V).

The HV254 is designed to operate with minimal power consumption while maintaining a guaranteed slew rate of 3.0V/µs. High value resistors are used for the gain setting to minimize current on the feedback path.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV254FG-G	100-Lead MQFP	66/Tray

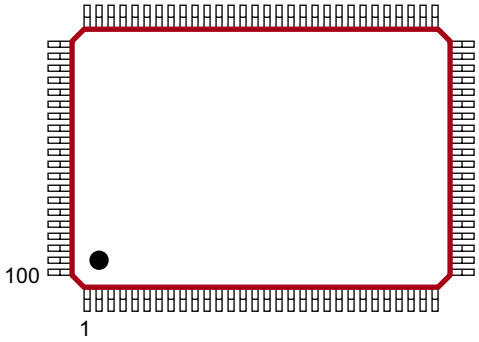
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{PP}, High voltage supply	275V
V+, Low voltage positive supply	7.0V
V-, Low voltage negative supply	-7.0V
HV_{OUT}, Output voltage	0V to 275V
V_{IN}, Analog input signal	0V to 5.0V
Storage temperature range	-65°C to 150°C
Maximum junction temperature	150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



100-Lead MQFP
(top view)

Product Marking

Top Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID
____ = "Green" Packaging

Package may or may not include the following marks: Si or

100-Lead MQFP

Typical Thermal Resistance

Package	θ_{ja}
100-Lead MQFP	39°C/W

Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High voltage positive supply	50	-	275	V	---
V+	Low voltage positive supply	4.75	5.00	5.25	V	---
V-	Low voltage negative supply	-4.75	-5.00	-5.25	V	---
I_{PP}	V_{PP} supply current	1.0	-	2.5	mA	V_{PP} = 275V. All inputs set at 140mV. Typically 45µA per channel.
I+	V+ supply current	-	-	1.0	mA	V+ = 5.25V
I-	V- supply current	-	-	-3.0	mA	V- = -5.25V
T_A	Ambient temperature range	-10	-	70	°C	---
T_J	Operating temperature range	-10	-	125	°C	---

Electrical Characteristics *(over operating conditions, unless otherwise specified)*

High Voltage Amplifier Output

Sym	Parameter	Min	Typ	Max	Units	Conditions
HV_{OUT}	HV_{OUT} voltage swing	7.0	-	250	V	V_{PP} = 275V, Load = 125MΩ//100pF
V_{IN}	Input voltage range	0.14	-	V+	V	---
HV_{OS}	HV_{OUT} DC offset	-	±1.50	±1.52	V	V_{PP} = 275V, 30mV input offset
SR	HV_{OUT} slew rate	3.0	-	-	V/µs	V_{PP} = 275V, load = 125MΩ//100pF
R_{FB}	Feedback impedence	8.0	12	-	MΩ	---
A_V	Closed loop gain	47.5	50.0	52.5	V/V	---
BW	HV_{OUT} -3dB channel bandwidth	5.0	-	-	KHz	V_{PP} = 275V
C_{LOAD}	HV_{OUT} capacitive load	0	-	100	pF	---
	Stability (max drift)	-	-	500	mV	Measured at HV_{OUT}

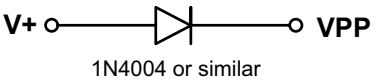
Temperature Diode

Sym	Parameter	Min	Typ	Max	Units	Conditions
PIV	Peak inverse voltage	-	-	5.0	V	cathode to anode
V_F	Forward diode drop	-	-	0.8	V	I_F = 100µA, anode to cathode
I_F	Forward diode current	-	-	100	µA	anode to cathode
T_C	V_F temperature coefficient	-	-2.2	-	mV/°C	anode to cathode

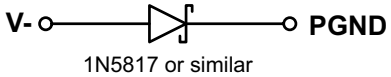
Power Up/Down Sequence

External Diode Protection

The device can be damaged due to improper power up/down sequence. To prevent damage, please follow the acceptable power up/down sequences and add two external diodes as shown in the diagram below. The first diode is a high voltage diode across VPP and V+ where the anode of the diode is connected to V+ and the cathode of the diode is connected to VPP. Any low current high voltage diode such as a 1N4004 will be adequate. The second diode is a schottky diode across V- and DGND where the anode of the schottky diode is connected to V- and the cathode is connected to DGND. Any low current schottky diode such as a 1N5817 will be adequate.



1N4004 or similar



1N5817 or similar

Acceptable Power Up Sequences

The HV254 can be powered up with any of the following sequences listed below.

1) VPP 2) V- 3) V+ 4) Inputs and Anode

or

1) V- 2) V+ 3) VPP 4) Inputs and Anode

Acceptable Power Down Sequences

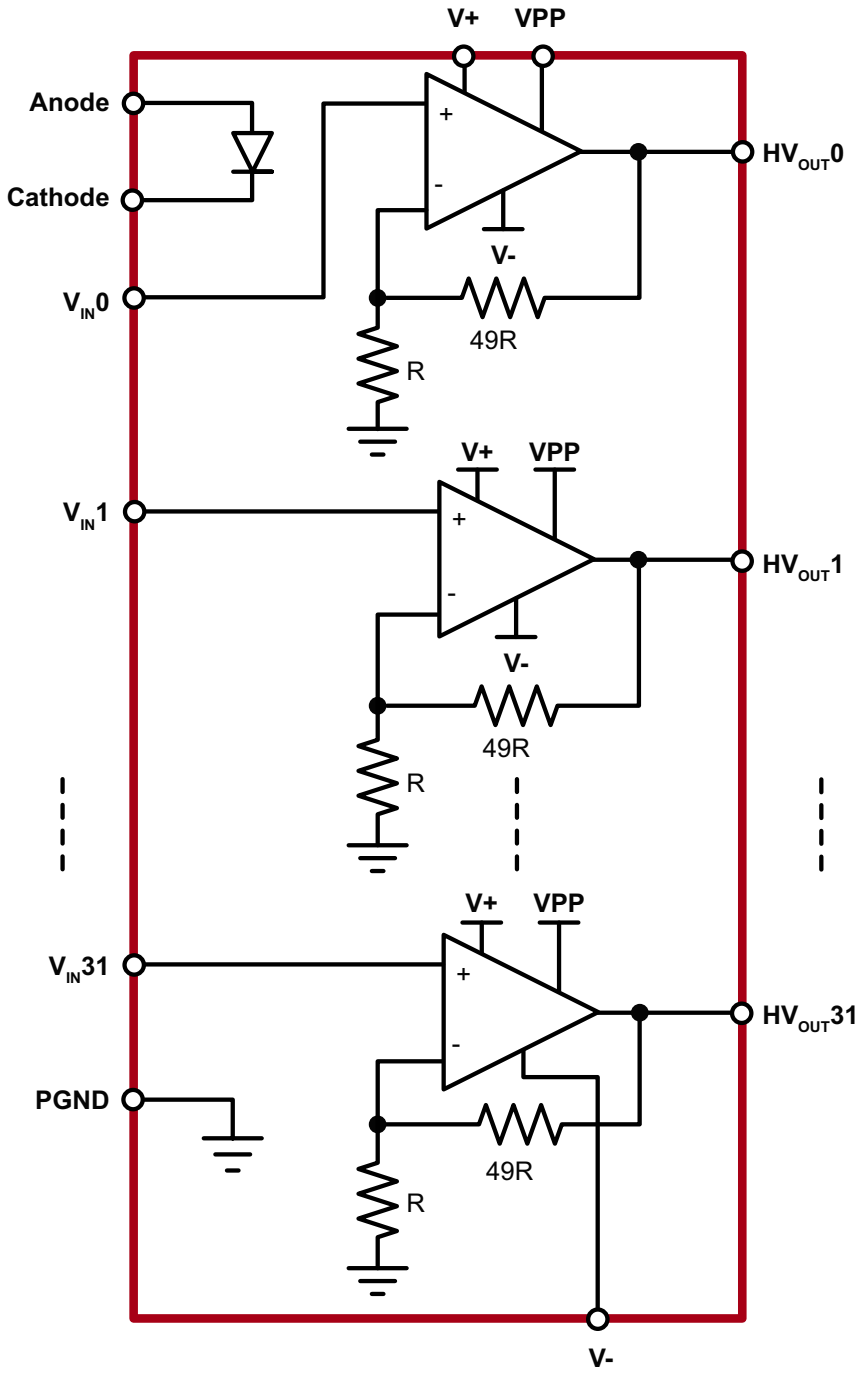
The HV254 can be powered down with any of the following sequences listed below.

1) Inputs and Anode 2) V+ 3) V- 4) VPP

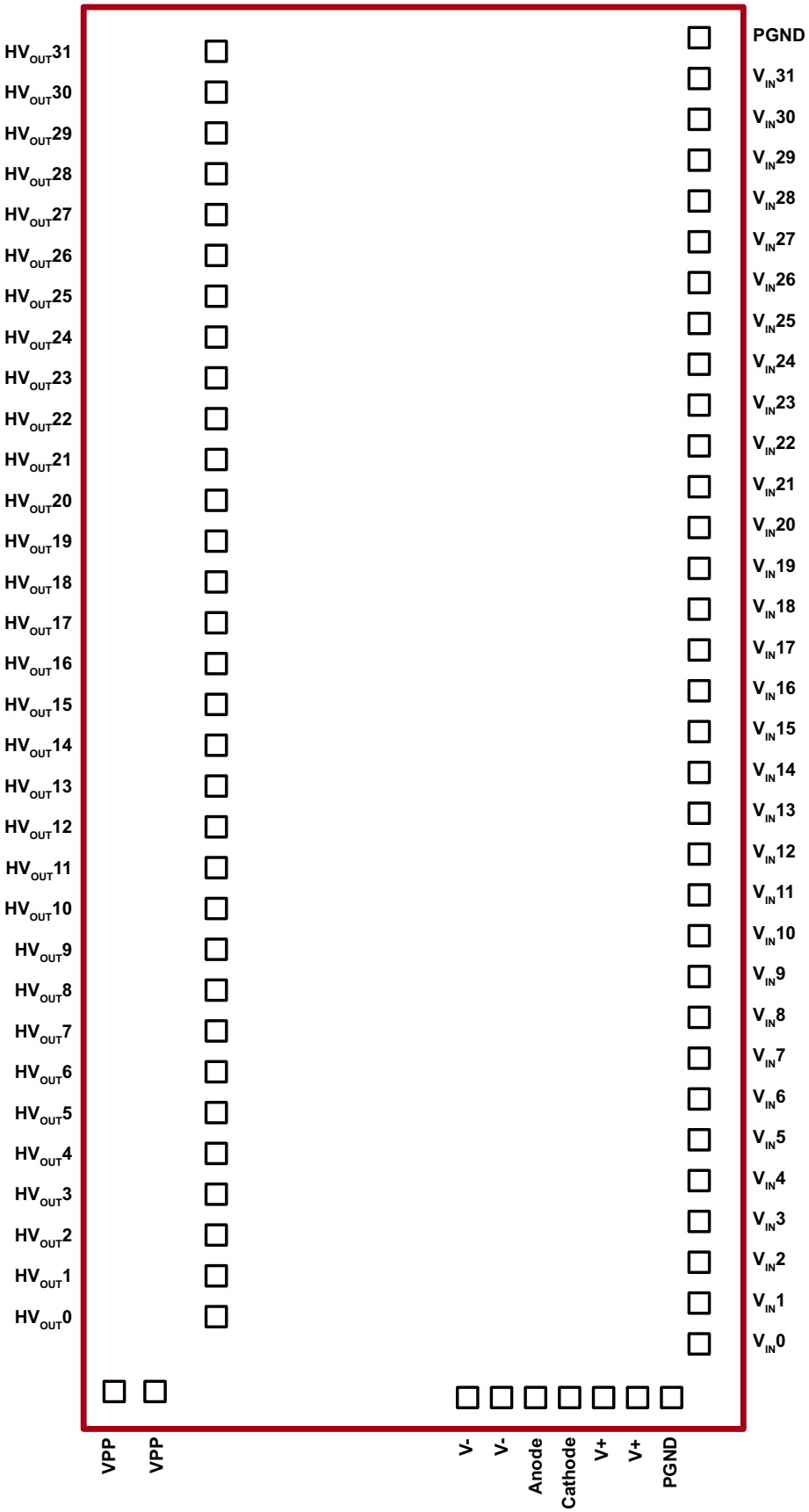
or

1) Inputs and Anode 2) VPP 3) V+ 4) V-

HV254 Block Diagram



Pad Configuration *(not drawn to scale)*



Pad Coordinates

Chip size: 4800µm x 11180µm
Center of die is (0,0)

Pad Name	X (µm)	Y (µm)
$HV_{OUT}31$	-1447.5	5244.0
$HV_{OUT}30$	-1447.5	4926.5
$HV_{OUT}29$	-1447.5	4609.0
$HV_{OUT}28$	-1447.5	4291.5
$HV_{OUT}27$	-1447.5	3974.0
$HV_{OUT}26$	-1447.5	3656.5
$HV_{OUT}25$	-1447.5	3339.0
$HV_{OUT}24$	-1447.5	3021.5
$HV_{OUT}23$	-1447.5	2704.0
$HV_{OUT}22$	-1447.5	2386.5
$HV_{OUT}21$	-1447.5	2069.0
$HV_{OUT}20$	-1447.5	1751.5
$HV_{OUT}19$	-1447.5	1434.0
$HV_{OUT}18$	-1447.5	1116.5
$HV_{OUT}17$	-1447.5	799.0
$HV_{OUT}16$	-1447.5	481.5
$HV_{OUT}15$	-1447.5	164.0
$HV_{OUT}14$	-1447.5	-153.5
$HV_{OUT}13$	-1447.5	-471.0
$HV_{OUT}12$	-1447.5	-788.5
$HV_{OUT}11$	-1447.5	-1106.0
$HV_{OUT}10$	-1447.5	-1423.5
$HV_{OUT}9$	-1447.5	-1741.0
$HV_{OUT}8$	-1447.5	-2058.5
$HV_{OUT}7$	-1447.5	-2376.0
$HV_{OUT}6$	-1447.5	-2693.5
$HV_{OUT}5$	-1447.5	-3011.0
$HV_{OUT}4$	-1447.5	-3328.5
$HV_{OUT}3$	-1447.5	-3646.0
$HV_{OUT}2$	-1447.5	-3963.5
$HV_{OUT}1$	-1447.5	-4281.0
$HV_{OUT}0$	-1447.5	-4598.5
VPP	-2057.0	-4985.0
VPP	-1897.0	-4985.0
V-	1030.5	-5018.0
V-	1190.5	-5018.0
ANODE	1350.5	-5018.0
CATHODE	1550.5	-5018.0
V+	1710.5	-5018.0
V+	1870.5	-5018.0
PGND	2034.5	-5018.0
$V_{IN}0$	2156.5	-4725.0
$V_{IN}1$	2156.5	-4411.0
$V_{IN}2$	2156.5	-4097.0
$V_{IN}3$	2156.5	-3783.0
$V_{IN}4$	2156.5	-3469.0
$V_{IN}5$	2156.5	-3155.0
$V_{IN}6$	2156.5	-2841.0
$V_{IN}7$	2156.5	-2527.0
$V_{IN}8$	2156.5	-2213.0
$V_{IN}9$	2156.5	-1899.0
$V_{IN}10$	2156.5	-1585.0
$V_{IN}11$	2156.5	-1271.0
$V_{IN}12$	2156.5	-957.0
$V_{IN}13$	2156.5	-643.0
$V_{IN}14$	2156.5	-329.0
$V_{IN}15$	2156.5	-15.0
$V_{IN}16$	2156.5	299.0
$V_{IN}17$	2156.5	613.0
$V_{IN}18$	2156.5	927.0
$V_{IN}19$	2156.5	1241.0
$V_{IN}20$	2156.5	1555.0
$V_{IN}21$	2156.5	1869.0
$V_{IN}22$	2156.5	2183.0
$V_{IN}23$	2156.5	2497.0
$V_{IN}24$	2156.5	2811.0
$V_{IN}25$	2156.5	3125.0
$V_{IN}26$	2156.5	3439.0
$V_{IN}27$	2156.5	3753.0
$V_{IN}28$	2156.5	4067.0
$V_{IN}29$	2156.5	4381.0
$V_{IN}30$	2156.5	4695.0
$V_{IN}31$	2156.5	5009.0
PGND	2156.5	5315.5

Notes:

1. *The two PGND pads are not electrically connected.*
2. *The two VPP pads, V+ pads, and V- pads are electrically connected.*
3. *Backside potential is VPP. Leave floating or connect to VPP.*
4. *Anode and Cathode are connected to the P and N terminals (respectively) of a silicon diode which can be used to measure temperature.*

Pin Description

Pin #	Function	Description
1	$HV_{OUT}29$	Amplifier outputs.
2	$HV_{OUT}28$	
3	$HV_{OUT}27$	
4	$HV_{OUT}26$	
5	$HV_{OUT}25$	
6	$HV_{OUT}24$	
7	$HV_{OUT}23$	
8	$HV_{OUT}22$	
9	$HV_{OUT}21$	
10	$HV_{OUT}20$	
11	$HV_{OUT}19$	
12	$HV_{OUT}18$	
13	$HV_{OUT}17$	
14	$HV_{OUT}16$	
15	$HV_{OUT}15$	
16	$HV_{OUT}14$	
17	$HV_{OUT}13$	
18	$HV_{OUT}12$	
19	$HV_{OUT}11$	
20	$HV_{OUT}10$	
21	$HV_{OUT}09$	
22	$HV_{OUT}08$	
23	$HV_{OUT}07$	
24	$HV_{OUT}06$	
25	$HV_{OUT}05$	
26	$HV_{OUT}04$	
27	$HV_{OUT}03$	
28	$HV_{OUT}02$	
29	$HV_{OUT}01$	
30	$HV_{OUT}0$	
31	NC	No connect.
32		
33		
34		
35		

Pin Description *(cont.)*

Pin #	Function	Description
36	VPP	High voltage positive supply.
37		
38	NC	No connect.
39	IBIAS	For internal testing only. Leave floating.
40	NC	No connect.
41	V-	Low voltage negative supply.
42		
43	ANODE	Anode side of of a low voltage silicon diode that can be used to monitor die temperature.
44	CATHODE	Cathode side of of a low voltage silicon diode that can be used to monitor die temperature.
45	V+	Low voltage positive supply.
46		
47	NC	No connect.
48	PGND	Power ground. Two PGND pads. Need to be externally connected.
49	$V_{IN}0$	Amplifier inputs.
50	$V_{IN}1$	
51	$V_{IN}2$	
52	$V_{IN}3$	
53	$V_{IN}4$	
54	$V_{IN}5$	
55	$V_{IN}6$	
56	$V_{IN}7$	
57	$V_{IN}8$	
58	$V_{IN}9$	
59	$V_{IN}10$	
60	$V_{IN}11$	
61	$V_{IN}12$	
62	$V_{IN}13$	
63	$V_{IN}14$	
64	$V_{IN}15$	
65	$V_{IN}16$	
66	$V_{IN}17$	
67	$V_{IN}18$	

Pin Description *(cont.)*

Pin #	Function	Description
68	$V_{IN}19$	Amplifier inputs.
69	$V_{IN}20$	
70	$V_{IN}21$	
71	$V_{IN}22$	
72	$V_{IN}23$	
73	$V_{IN}24$	
74	$V_{IN}25$	
75	$V_{IN}26$	
76	$V_{IN}27$	
77	$V_{IN}28$	
78	$V_{IN}29$	
79	$V_{IN}30$	
80	$V_{IN}31$	
81	PGND	Power ground. Two PGND pads. Need to be externally connected.
82	NC	No connect.
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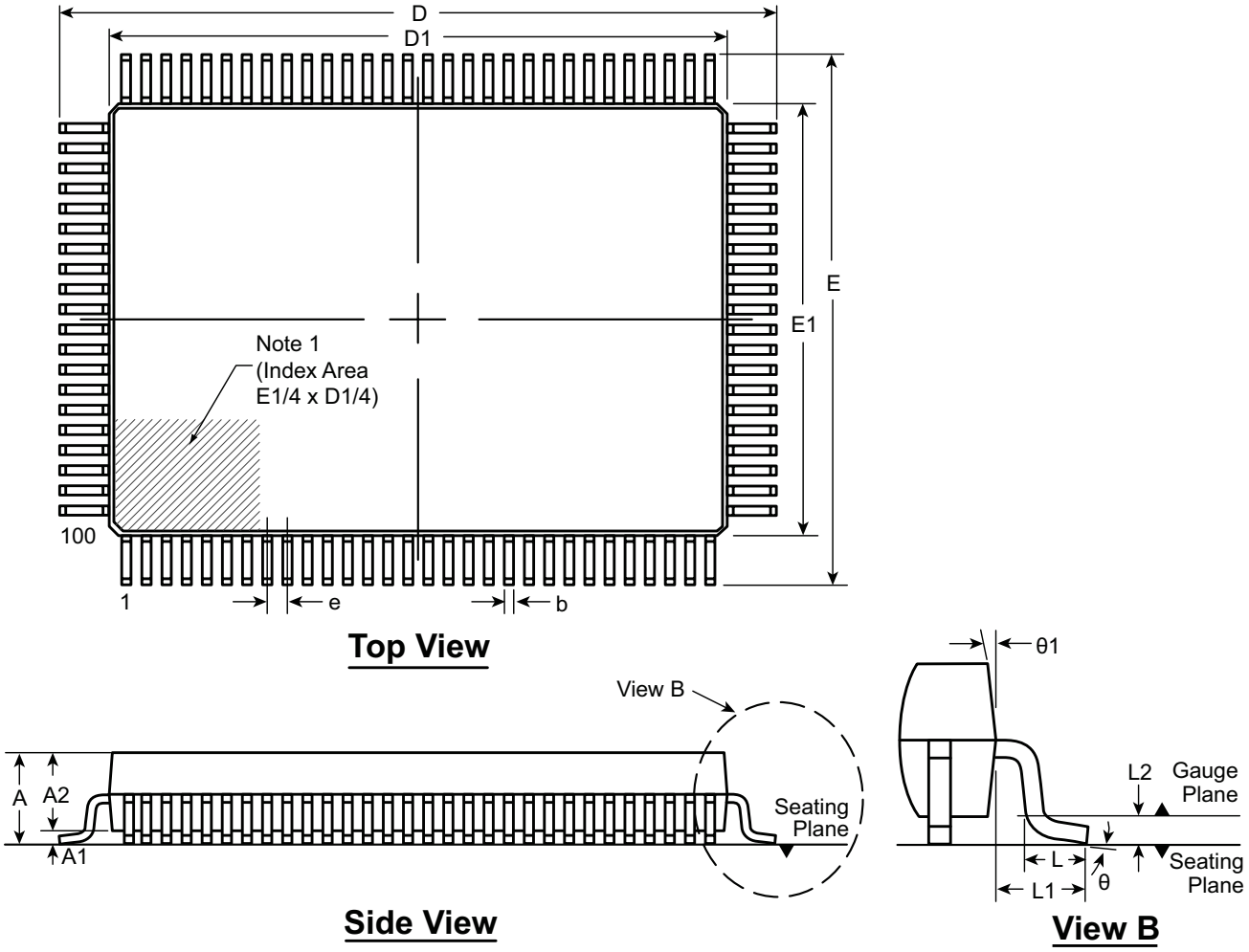
99	$HV_{OUT}31$	Amplifier outputs.
100	$HV_{OUT}30$	

100-Lead MQFP Package Outline (FG)

20.00x14.00mm body, 3.15mm height (max), 0.65mm pitch, 3.20mm footprint



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.50*	0.00	2.50	0.22	22.95*	19.80*	16.95*	13.80*	0.65 BSC	0.73	1.60 REF	0.25 BSC	0°	5°
	NOM	-	-	2.70	-	23.20	20.00	17.20	14.00		0.88			-	-
	MAX	3.15	0.25	2.90	0.40	23.45*	20.20*	17.45*	14.20*		1.03			7°	16°

JEDEC Registration MS-022, Variation GC-2, Issue B, Dec. 1996.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-100MQFPFG, Version F041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com