



BU808DFI

HIGH VOLTAGE FAST-SWITCHING NPN POWER DARLINGTON TRANSISTOR

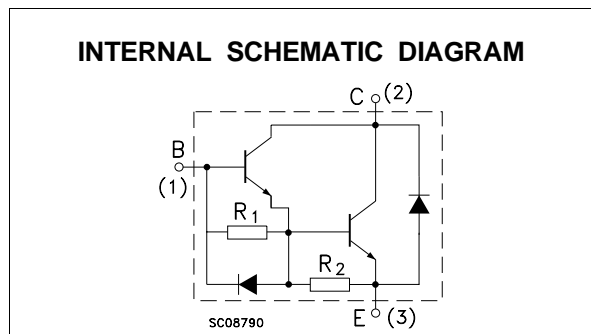
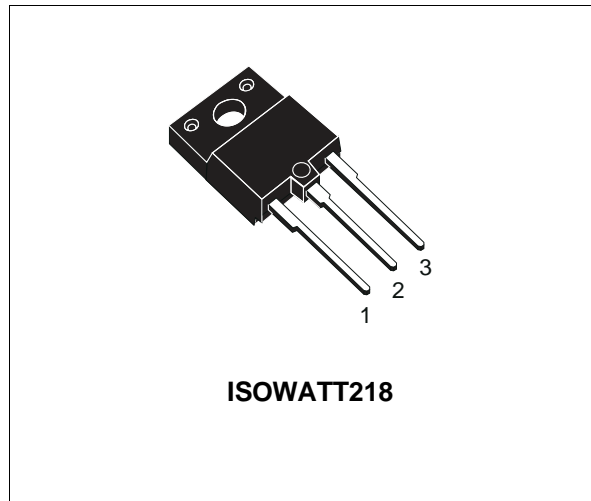
- STMicroelectronics PREFERRED SALESTYPE
- NPN MONOLITHIC DARLINGTON WITH INTEGRATED FREE-WHEELING DIODE
- HIGH VOLTAGE CAPABILITY ($> 1400\text{ V}$)
- HIGH DC CURRENT GAIN (TYP. 150)
- FULLY INSULATED PACKAGE (U.L. COMPLIANT) FOR EASY MOUNTING
- LOW BASE-DRIVE REQUIREMENTS
- DEDICATED APPLICATION NOTE AN1184

APPLICATIONS

- COST EFFECTIVE SOLUTION FOR HORIZONTAL DEFLECTION IN LOW END TV UP TO 21 INCHES.

DESCRIPTION

The BU808DFI is a NPN transistor in monolithic Darlington configuration. It is manufactured using Multi-epitaxial Mesa technology for cost-effective high performance.



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------|------------------------------------------------------------------------------|------------|------|
| V_{CBO} | Collector-Base Voltage ($I_E = 0$) | 1400 | V |
| V_{CEO} | Collector-Emitter Voltage ($I_B = 0$) | 700 | V |
| V_{EBO} | Emitter-Base Voltage ($I_C = 0$) | 5 | V |
| I_C | Collector Current | 8 | A |
| I_{CM} | Collector Peak Current ($t_p < 5\text{ ms}$) | 10 | A |
| I_B | Base Current | 3 | A |
| I_{BM} | Base Peak Current ($t_p < 5\text{ ms}$) | 6 | A |
| P_{tot} | Total Dissipation at $T_c = 25\text{ °C}$ | 52 | W |
| V_{isol} | Insulation Withstand Voltage (RMS) from All Three Leads to External Heatsink | 2500 | V |
| T_{stg} | Storage Temperature | -65 to 150 | °C |
| T_j | Max. Operating Junction Temperature | 150 | °C |

BU808DFI

THERMAL DATA

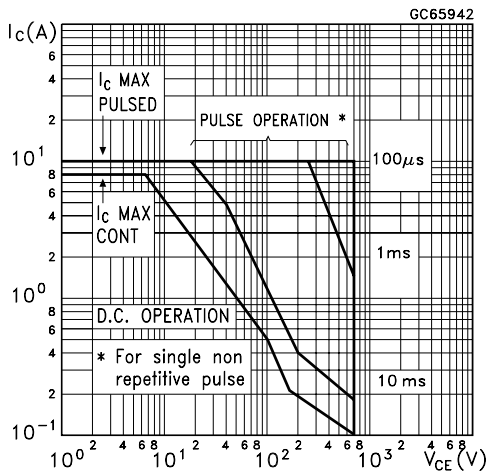
| | | | | |
|----------------|----------------------------------|-----|-----|---------------|
| $R_{thj-case}$ | Thermal Resistance Junction-case | Max | 2.4 | $^{\circ}C/W$ |
|----------------|----------------------------------|-----|-----|---------------|

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

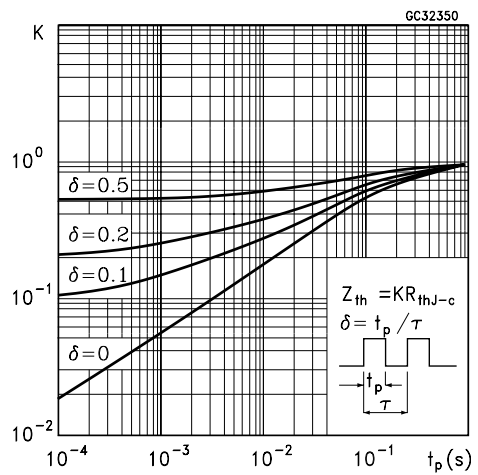
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------------------|-----------------------------------------------------------------------------------------------|----------|----------|----------|--------------------|
| I_{CES} | Collector Cut-off Current ($V_{BE} = 0$) | $V_{CE} = 1400 V$ | | | 400 | μA |
| I_{EBO} | Emitter Cut-off Current ($I_C = 0$) | $V_{EB} = 5 V$ | | | 100 | mA |
| $V_{CE(sat)*}$ | Collector-Emitter Saturation Voltage | $I_C = 5 A$ $I_B = 0.5 A$ | | | 1.6 | V |
| $V_{BE(sat)*}$ | Base-Emitter Saturation Voltage | $I_C = 5 A$ $I_B = 0.5 A$ | | | 2.1 | V |
| h_{FE*} | DC Current Gain | $I_C = 5 A$ $V_{CE} = 5 V$ $I_C = 5 A$ $V_{CE} = 5 V$ $T_j = 100^{\circ}C$ | 60 20 | | 230 | |
| t_s t_f | INDUCTIVE LOAD Storage Time Fall Time | $V_{CC} = 150 V$ $I_C = 5 A$ $I_{B1} = 0.5 A$ $V_{BE(off)} = -5 V$ | | | 3 0.8 | μs μs |
| t_s t_f | INDUCTIVE LOAD Storage Time Fall Time | $V_{CC} = 150 V$ $I_C = 5 A$ $I_{B1} = 0.5 A$ $V_{BE(off)} = -5 V$ $T_j = 100^{\circ}C$ | | 2 0.8 | | μs μs |
| V_F | Diode Forward Voltage | $I_F = 5 A$ | | | 3 | V |

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

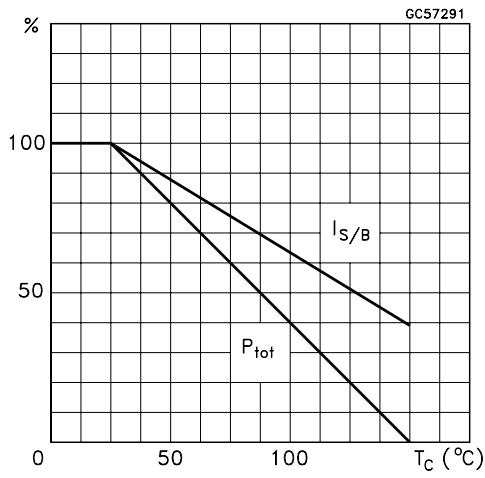
Safe Operating Area



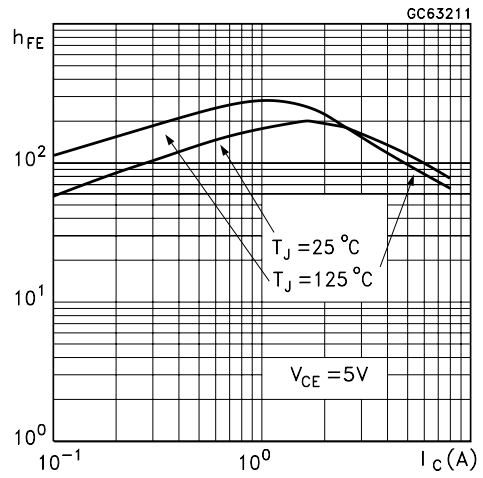
Thermal Impedance



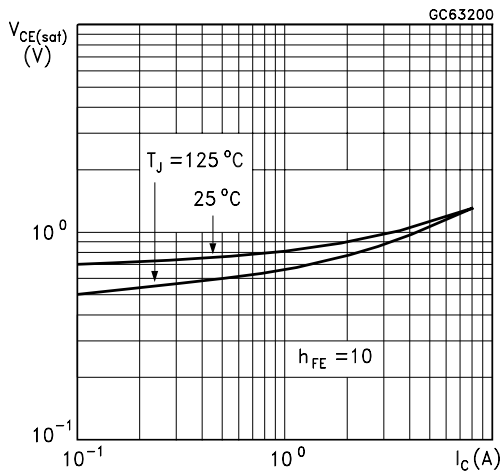
Derating Curve



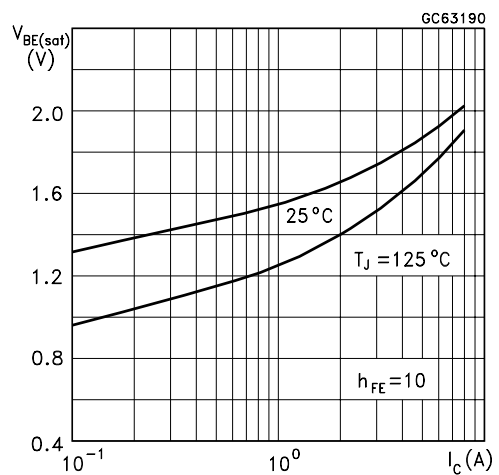
DC Current Gain



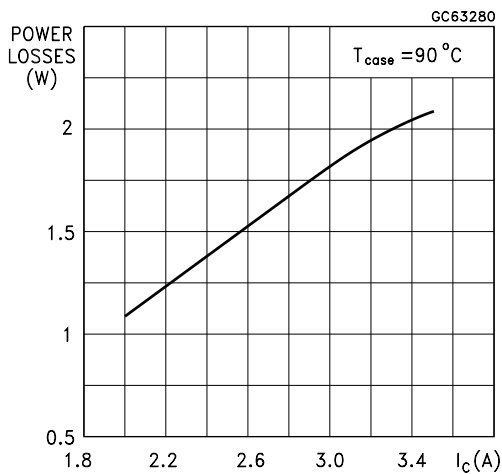
Collector Emitter Saturation Voltage



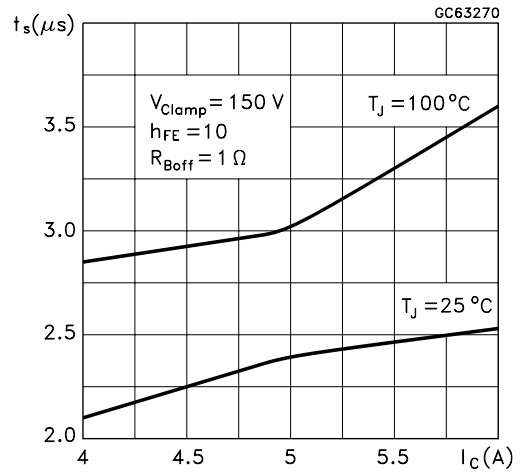
Base Emitter Saturation Voltage



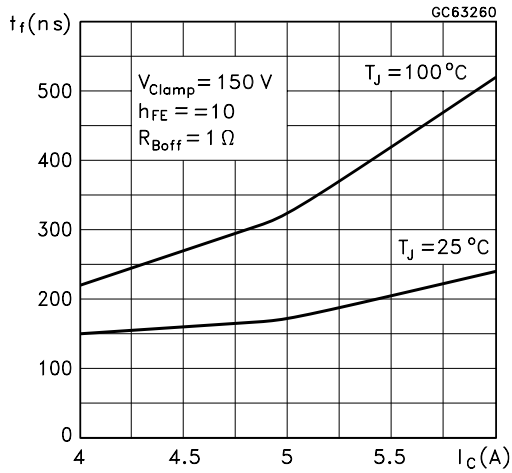
Power Losses at 16 KHz



Switching Time Inductive Load at 16KHz



Switching Time Inductive Load at 16KHZ

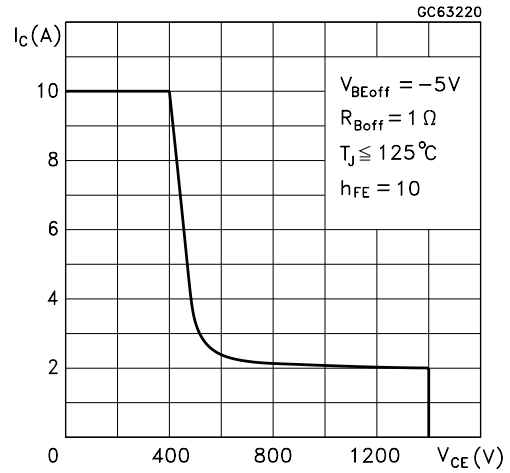


BASE DRIVE INFORMATION

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at $100\ ^\circ\text{C}$ (line scan phase). On the other hand, negative base current I_{B2} must be provided to turn off the power transistor (retrace phase).

Most of the dissipation, in the deflection application, occurs at switch-off. Therefore it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j . A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz scanning frequencies for choosing the optimum negative

Reverse Biased SOA



drive. The test circuit is illustrated in figure 1.

Inductance L_1 serves to control the slope of the negative base current I_{B2} to recombine the excess carrier in the collector when base current is still present, this would avoid any tailing phenomenon in the collector current.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2 \quad \omega = 2\pi f = \frac{1}{\sqrt{LC}}$$

Where I_C = operating collector current, V_{CEfly} = flyback voltage, f = frequency of oscillation during retrace.

Figure 1: Inductive Load Switching Test Circuits.

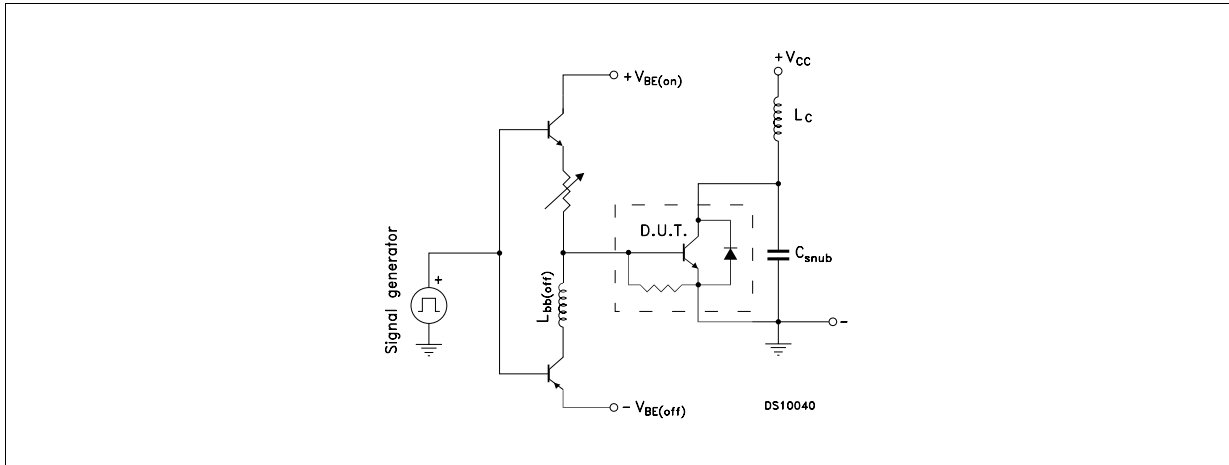
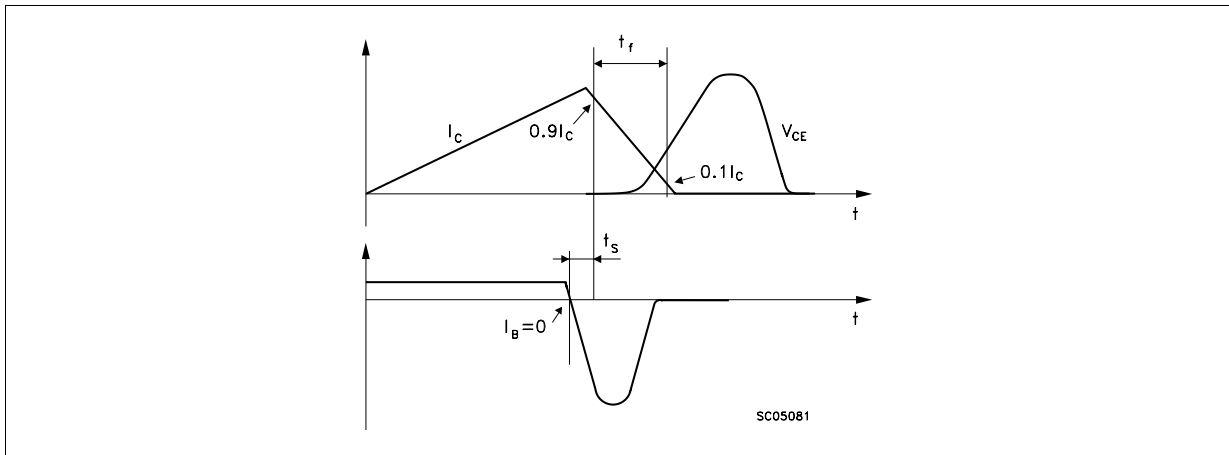
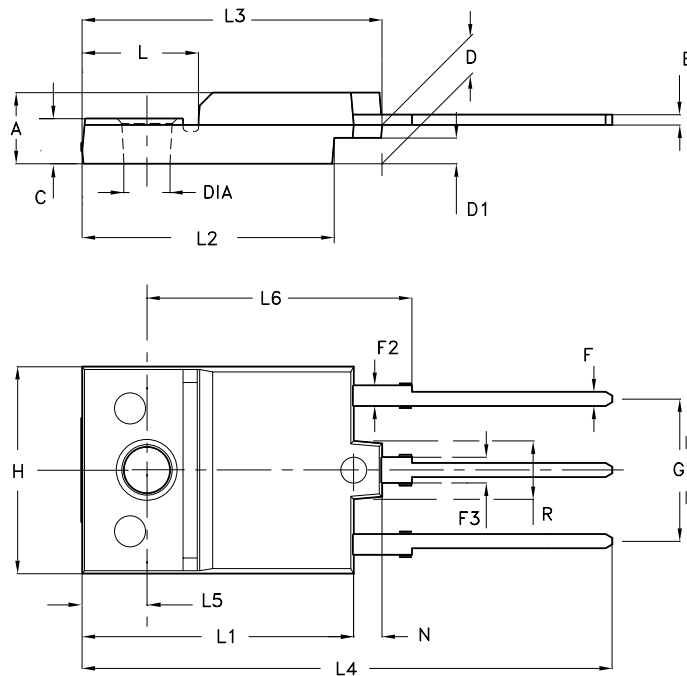


Figure 2: Switching Waveforms in a Deflection Circuit



ISOWATT218 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-------|------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 5.35 | | 5.65 | 0.211 | | 0.222 |
| C | 3.30 | | 3.80 | 0.130 | | 0.150 |
| D | 2.90 | | 3.10 | 0.114 | | 0.122 |
| D1 | 1.88 | | 2.08 | 0.074 | | 0.082 |
| E | 0.75 | | 0.95 | 0.030 | | 0.037 |
| F | 1.05 | | 1.25 | 0.041 | | 0.049 |
| F2 | 1.50 | | 1.70 | 0.059 | | 0.067 |
| F3 | 1.90 | | 2.10 | 0.075 | | 0.083 |
| G | 10.80 | | 11.20 | 0.425 | | 0.441 |
| H | 15.80 | | 16.20 | 0.622 | | 0.638 |
| L | | 9 | | | 0.354 | |
| L1 | 20.80 | | 21.20 | 0.819 | | 0.835 |
| L2 | 19.10 | | 19.90 | 0.752 | | 0.783 |
| L3 | 22.80 | | 23.60 | 0.898 | | 0.929 |
| L4 | 40.50 | | 42.50 | 1.594 | | 1.673 |
| L5 | 4.85 | | 5.25 | 0.191 | | 0.207 |
| L6 | 20.25 | | 20.75 | 0.797 | | 0.817 |
| N | 2.1 | | 2.3 | 0.083 | | 0.091 |
| R | | 4.6 | | | 0.181 | |
| DIA | 3.5 | | 3.7 | 0.138 | | 0.146 |



- Weight : 4.9 g (typ.)
- Maximum Torque (applied to mounting flange) Recommended: 0.8 Nm; Maximum: 1 Nm
- The side of the dissipator must be flat within 80 μm

P025C/A

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2002 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>