National Semiconductor

LM3001 Primary-Side PWM Driver

General Description

The LM3001 is a primary-side PWM driver that provides all the system start-up, switch control, and protection functions needed on the primary side of an isolated offline converter. It is primarily designed for pulse communication between the primary and secondary controllers.

The LM3001 combined with the LM3101 secondary-side controller forms an offline converter chip set which allows electrical isolation between the high-power primary-side switch and the precision secondary-side control. Secondary-to-primary communication is achieved using pulse communication, via a small pulse transformer.

The primary-side driver includes a 2.5A totem-pole output switch with rise and fall times of less than 20 ns. This allows the LM3001 to operate at frequencies from below 50 kHz to beyond 1 MHz. The maximum duty cycle is programmable for each application. There are two levels of current limit within the LM3001, both of which are ground-referenced. One is a cycle-by-cycle current limit which activates at 0.38V. The other is a secondary current limit that activates at 0.6V. This current limit shuts down the LM3001 for a programmable deadtime, which is set with an external capacitor. Although the LM3001 is optimized for pulse feedback communication, it can also operate with conventional opto-coupler feedback.

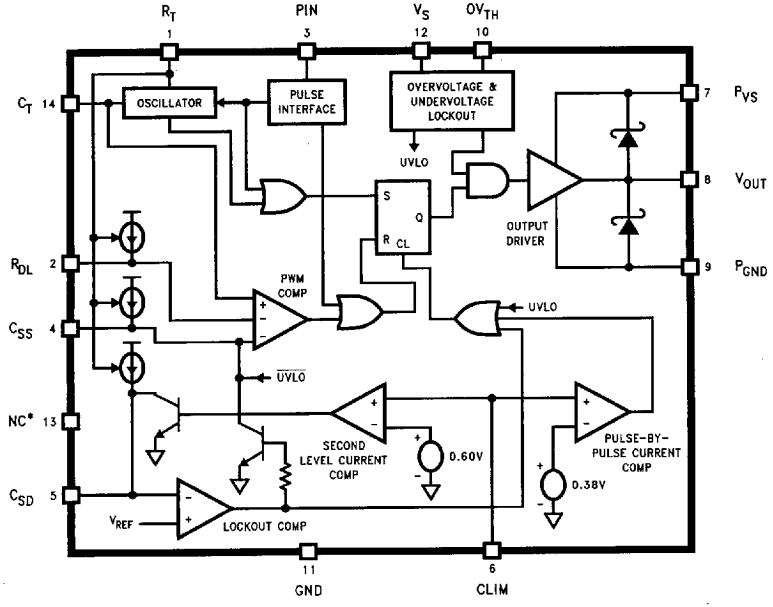
Features

- 2.5A peak high speed output driver
- Low start-up current (typ. 190 μA)
- Dual-level current limit with programmable lockout time
- Duty cycle clamp
- Operation beyond 1 MHz
- Soft-Start, undervoltage and overvoltage lockout with hysteresis
- Low output saturation voltage: Maximum of 1.5V at 400 mA sink current
- Active low output when in Undervoltage Lockout

Typical Applications

- Isolated offline switching power supplies
- Isolated Power DC/DC converters
- Flyback converter
- Forward converter

Block Diagram



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*Internal Test Point. Leave Open.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_S, P_{VS})	20V
$V_S - P_{VS}$	±0.3V
Pulse Interface Input Current (I_{PIN})	±4 mA
ESD (Note 2)	2 kV

Operating Ratings

Supply Voltages	$8.5V \le V_S \le 20V$
	$8.5V \le P_{VS} \le 20V$
Junction Temperature Range	$-40°C \le T_J \le +125°C$

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_S = P_{VS} = 15V, C_L = 1 nF, R_L = 10 kΩ, R_T = 5.76 kΩ, C_T = 200 pF (F_O = 500 kHz).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OSCILLATOR SECTION						
F_O	Oscillator Frequency (Note 3)	R_T = 5.76 kΩ, C_T = 200 pF	425 **400**	500	575 **600**	kHz
		R_T = 5.29 kΩ, C_T = 100 pF	0.85 **0.80**	1.0	1.15 **1.20**	MHz
V_{PP}	Peak-to-Peak Voltage (Pin 14)			1.0		V
$I_{CT(SINK)}$	Timing Capacitor Sink Current	V_{CT} = 3.5V		3.0		mA
$\Delta F_O/\Delta V_S$	Line Regulation	$9.8V \le V_S \le 20V$		0.02	0.1	%/V
PULSE INTERFACE SECTION (Note 4)						
$I_{PIN(SINK)}$	Minimum Pulse Input Sink Current Threshold			0.16	0.25 **0.35**	mA
$I_{PIN(SOURCE)}$	Minimum Pulse Input Source Current Threshold			0.25	0.40 **0.50**	mA
t_{PW}	Minimum Pulse Width			15	30	ns
t_{dON}	Pulse Rise Delay-to-Output Time			28	42 **49**	ns
t_{dOFF}	Pulse Fall Delay-to-Output Time			26	42 **47**	ns
PULSE-WIDTH MODULATOR SECTION						
D_{MIN}	Minimum Duty Cycle			3	4.75 **5**	%
D_{MAX}	Maximum Duty Cycle	R_{DL} = 26.1 kΩ	78	85	91 **97**	%
		R_{DL} = 22.6 kΩ	42	50	58 **60**	%
CURRENT LIMIT SECTION						
V_{CL1}	Pulse-by-Pulse Current Limit Threshold Voltage		0.32 **0.28**	0.38	0.44 **0.46**	V
V_{CL2}	Secondary Current Limit Threshold Voltage		0.55 **0.50**	0.60	0.67 **0.70**	V
Δt_{dCL}	Pulse-by-Pulse Current Limit Delay Time	200 mV overdrive		50	70 **85**	ns

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those in **bold type face** apply over full **Operating Temperature Range**. Unless otherwise specified, V_S = P_{VS} = 15V, C_L = 1 nF, R_L = 10 kΩ, R_T = 5.76 kΩ, C_T = 200 pF (F_O = 500 kHz). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CURRENT LIMIT SECTION (Continued)						
I_B	Current Limit Sense Input Bias Current			−0.35		µA
I_{CSD}	Secondary Current Limit Restart Capacitor Charge Current (Pin 5)	(Note 5)	58 **42**	65	70 **84**	µA
ΔV_{SD}	Secondary Current Limit Restart Hysteresis		1.30 **1.20**	1.40	1.55 **1.65**	V
OUTPUT SECTION						
V_{OL}	Output Low Saturation Voltage	I_{SINK} = 400 mA		1.3	1.5 **1.8**	V
		I_{SINK} = 20 mA		1.0	1.2	V
V_{OH}	Output High Saturation Voltage	I_{SOURCE} = 400 mA		2.0	2.4	V
		I_{SOURCE} = 20 mA		1.6	1.9	V
t_R	Rise Time	C_L = 1000 pF		11	22 **25**	ns
t_F	Fall Time	C_L = 1000 pF		8	18 **20**	ns
OVERVOLTAGE SHUTDOWN SECTION						
V_{OVTH}	Overvoltage Shutdown Comparator Threshold Voltage		3.05 **2.80**	3.30	3.55 **3.80**	V
V_{OVH}	Overvoltage Shutdown Comparator Hysteresis		0.10 **0.06**	0.19	0.25 **0.31**	V
UNDERVOLTAGE LOCKOUT SECTION						
V_{ULTH}	Turn-On Threshold Voltage		11.0 **10.0**	11.8	12.6 **13.6**	V
V_{ULH}	Undervoltage Lockout Hysteresis		2.80 **2.40**	3.20	3.60 **3.80**	V
SOFT-START/DELAY SECTION						
I_{SS}	Soft-Start Current	(Note 5)	61 **57**	66	71 **75**	µA
V_{SS}	Soft-Start Threshold Voltage		2.10 **1.90**	2.30	2.60 **2.80**	V
V_{SI}	Initial Soft-Start Voltage	(Note 6)		0.7		V
SUPPLY AND START-UP SECTION						
I_S	Supply Current	100% Duty Cycle and No Load (Note 7)		21	28 **32**	mA
I_Q	Quiescent Current	V_S = 9V (Note 7)		190	250 **300**	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Pins 6 and 10, the Current Limit Input and the Overvoltage Threshold pins respectively, have an ESD rating of 1.8 kV.
Note 3: The oscillator frequency is set by R_T and C_T according to the equation:

$$\frac{1}{F_O} = T = C_T \bullet (1.5\,(R_T) + 728\Omega).$$

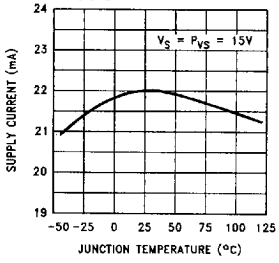
Note 4: The internal oscillator will synchronize to the frequency of the feedback pulse.
Note 5: These currents are set by R_T according to the equation:

$$I = 1.4V/(2 \bullet R_T).$$

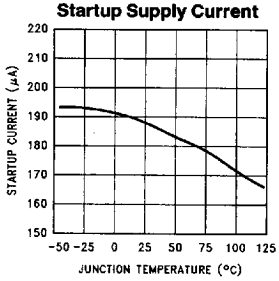
The timing resistor during these tests is set at 10.6 kΩ.
Note 6: The initial Soft-Start voltage is the voltage at the beginning of the start-up or re-start cycle.
Note 7: Total supply current drawn by V_S and P_{VS} supply pins.

Typical Performance Characteristics

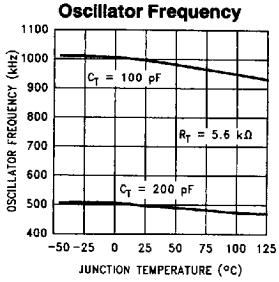
Supply Current



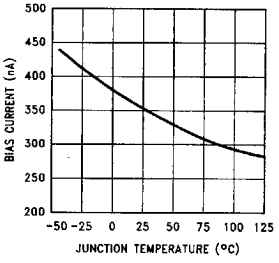
Startup Supply Current



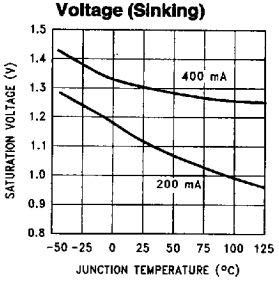
Oscillator Frequency



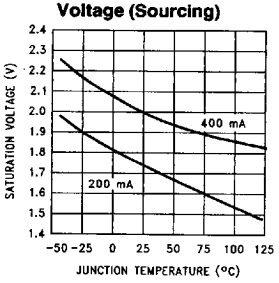
Current Sense Comparator Input Bias Current



Output Low Saturation Voltage (Sinking)



Output High Saturation Voltage (Sourcing)



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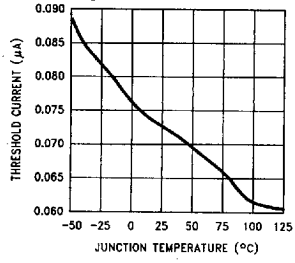
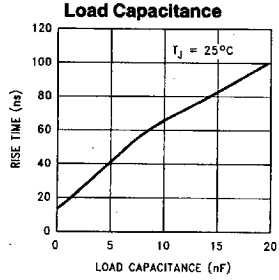
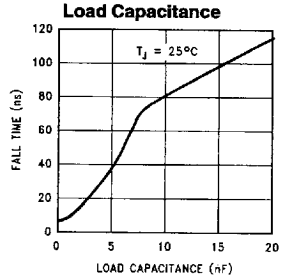
Overvoltage Comparator Input Bias Current



Rise Time vs Load Capacitance



Fall Time vs Load Capacitance



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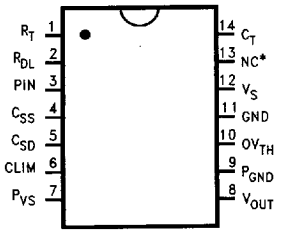
Connection Diagram and Ordering Information

14-Lead Package



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*Do not connect to this pin.

Top View

For DIP Package
Order Number LM3001N
See NS Package Number N14A

For Surface Mount Package
Order Number LM3001M
See NS Package Number M14B

Consult your local National Semiconductor Sales Office for Availability of this Device in the Surface-Mount Package

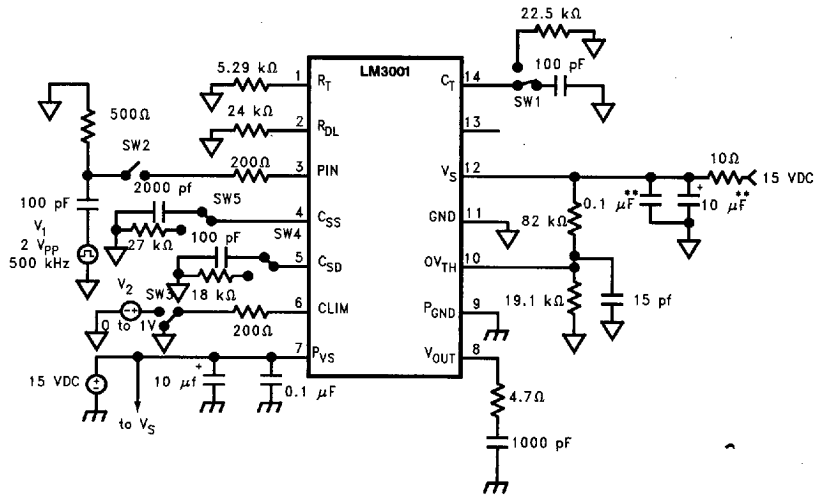
Pin-by-Pin Description

Pin No.	Symbol	Function	Description
Pin 1	R_T	Timing Resistor	A resistor from this pin to ground and a capacitor from pin 14 to ground programs the oscillator frequency by the following formula: $1/F_O = T = C_T \bullet (1.5 \bullet R_T + 728)$ [s, F, Ω]
Pin 2	R_{DL}	Duty Cycle Limit	The duty cycle limit is set by connecting a resistor, from this pin to ground, using the following formula: $R_{DL} = R_T [(D_{MAX} \bullet 1.71V) + 3.11V]$ [Ω, V] for $R_T \geq 5\ k\Omega$ and $3.37V \leq R_{DL}/R_T \leq 4.56$. An internal current source develops a voltage across this resistor which is compared to the oscillator ramp voltage (see the block diagram and the Oscillator section of the Functional Decriptions).
Pin 3	PIN	Pulse Input	Input for feedback pulses in pulse communication operating mode. The peak current of these pulses can range from 0.3 mA to 4 mA.
Pin 4	C_{SS}	Soft-Start Capacitor and Delay	A capacitor, connected from this pin to ground, programs the Soft-Start time delay. The Soft-Start time delay is made up of two parts: a time delay during which the output is turned off (zero duty cycle), and a time period in which the duty cycle goes from zero to its maximum value, set by the Duty Cycle Limit (see pin 2 description). The time delay equation is: $t_{DSS} = 2 \bullet C_{SS} \bullet R_T$ [s, F,Ω] The rate at which the duty cycle ramps up from zero to its maximum limit follows the equation: $D/t = 0.58/(C_{SS} \bullet R_T)$ [s, F,Ω]
Pin 5	C_{SD}	Shutdown Delay Capacitor	A capacitor, connected from this pin to ground. provides a time delay before the device can restart from a second level current limit shutdown (see pin 6 description). This action is governed by the formula: $t_{SD} = 2 \bullet C_{SD} \bullet R_T$ [s, F,Ω]
Pin 6	CLIM	Current Limit Input	This provides a pulse-by-pulse current limit, with a voltage threshold of 0.38V. If that is exceeded, a second level current limit, with a 0.60V threshold voltage shuts down the chip completely for a programmed time period (see pin 5 description).
Pin 7	P_{VS}	Driver Supply Voltage	Supply of the output driver.
Pin 8	V_{OUT}	Driver Output	Driver output. It can drive an external power MOSFET (in 11 ns typically) with peak source or sink currents of up to 2.5A.
Pin 9	P_{GND}	Power Ground	Power ground.

Pin-by-Pin Description (Continued)

Pin No.	Symbol	Function	Description
Pin 10	OV_{TH}	Overvoltage Threshold	This monitors the supply voltage through an external resistor divider. It shuts down the output driver if the threshold voltage is exceeded. The threshold voltage is 3.3V typical.
Pin 11	GND	Ground	Signal ground.
Pin 12	V_S	Supply Voltage	Supply voltage of the control circuit.
Pin 13	NC	No Connect	Internal Test Point. Leave Open.
Pin 14	C_T	Timing Capacitor	Inserting a capacitor from this pin to ground and a resistor from pin 1 to ground programs the oscillator frequency by the following formula: $1/F_O = T = C_T \bullet (1.5 \bullet R_T + 728)$ [s, F,Ω]

LM3001 Test Circuit



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Initial Conditions:
SW1—Connects pin 14 to 100 pF capacitor.
SW2—Open.
SW3—Connects 200Ω to ground.
SW4—Connects pin 5 to 100 pF capacitor.
SW5—Connects pin 4 to 2000 pF capacitor.

Bench Test Procedure*

*The LM3001 specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.

Required Equipment: Voltmeter, Storage Oscilloscope, Function Generator, Power Supply. Apply 15V between P_{VS} and P_{GND}. Then proceed with the following steps.

OSCILLATOR SECTION

Step 1: Measure the voltage at pin 1, across the 5.29 kΩ timing resistor R_T. It should range between 1.35 VDC and 1.55 VDC. Switch pin 14 from the 100 pF timing capacitor, C_T, to the 22.5 kΩ resistor. Measure the voltage across the resistor. It should be about 2.5V. Switch pin 14 back to the 100 pF capacitor.

Step 2: Measure the peak-to-peak voltage at pin 14 (across the timing capacitor C_T). It should be approximately 1.0V. Observe the waveform across the capacitor. The waveform frequency should measure approximately 1 MHz, and the shape of the waveform should be sawtooth.

Step 3: Measure the voltage at pin 2 (across the 24k resistor R_{DL}). It should be approximately 2.65V.

Bench Test Procedure* (Continued)

SWITCHING OUTPUT SECTION

Step 4: Observe the waveform at pin 8 (V_{OUT}). It should be a pulse-width modulated waveform with a frequency of about 1 MHz, the same frequency as the waveform of C_T (Step 2). Measure the duty cycle of the V_{OUT} waveform. It should be approximately 35%.

Step 5: Measure the rise and fall times of the V_{OUT} signal at pin 8. They each should be typically 12 ns. Measure the saturation voltage levels. The low saturation voltage level should measure about 1.5V, and the high saturation voltage level should be about 13.5V (15V−1.5V).

Step 6: Close SW2 to apply V_1, a 500 kHz $2V_{PK\text{-}to\text{-}PK}$ square wave, to pin 3 (the PIN input) through the 500Ω, 100 pF RC filter. The waveform at the V_{OUT} output should be a 500 kHz square wave. Measure the delay time from the rising edge of the input signal to the rising edge of the output waveform. The delay time should measure about 20 ns. The delay time between the falling edges of each signal should be the same.

Step 7: Open SW2 to disconnect the pulse waveform from pin 3. Observe the V_{OUT} waveform. It should also be off. Turn off the supply voltage.

INTERNAL SUPPLY OPERATIONS

Step 8: Slowly turn on the supply voltage back up toward 15V, while observing the V_{OUT} pin. Note the supply voltage when the V_{OUT} PWM waveform starts up—i.e., when the device turns on. The supply voltage should be about 11.8V. Measure the current into the supply pins P_{VS} and V_S (pins 7 and 12 respectively). The P_{VS} supply current should range from 13 mA to 23 mA, while the V_S supply current is about 12 mA. Decrease the supply voltage until the output shuts down. The supply voltage should read approximately 8.6V. Reset the supply voltage to 15V so that the device is back on.

Step 9: Increase the supply voltage until the V_{OUT} signal turns off. The voltage at the Overvoltage Threshold pin (pin 10) should be between 3.0V and 3.6V. The supply voltage should be approximately 20V. Return the supply voltage to 15V.

CURRENT LIMIT SECTION

Step 10: Connect V_2 (an adjustable voltage source set to 0V) through SW3 to the 200Ω resistor connected to pin 6, the Current Limit Input. Raise the voltage from 0V to 0.45V into the 200Ω resistor while monitoring the V_{OUT} signal. Output driver V_{OUT} should show a PWM waveform with a minimum duty cycle of approximately 3%. The minimum duty cycle waveform should start when the voltage source reaches approximately 0.38V.

Step 11: Increase the voltage at the source until the output turns off completely. The voltage should measure approximately 0.6V. The output should remain completely off until the shutdown time delay has expired and the voltage is removed.

SHUTDOWN DELAY/SOFT-START CONTROL SECTION

Step 12: Measure the shutdown time delay between when the V_2 voltage source is removed from the 200Ω resistor and when the output starts up again. It should equal the product of the following equation:

$$T_{SD} = 2 \bullet C_{SD} \bullet R_T.$$

With a 100 pF shutdown delay capacitor (C_{SD}) at pin 5 and a 5.29 kΩ timing resistor (R_T) at pin 1, the shutdown time delay should be approximately 1.3 μs.

Step 13: Switch SW4 from the shutdown delay capacitor to the 18 kΩ resistor at pin 5. Measure the voltage across the 18 kΩ. It should measure about 2.0V. Return the switch to the 100 pF capacitor.

Step 14: Switch SW5 from the 2000 pF Soft-Start delay capacitor to the 27 kΩ resistor at pin 4. Measure the voltage across the 27 kΩ resistor. It should measure about 3.0V. Return the switch to the 2000 pF capacitor. Turn off the supply voltage. End of test.

For further information on the IC operation, see the Functional Section Descriptions in the Application Section.

Functional Description

OSCILLATOR SECTION

The LM3001 oscillator can set the operating frequency from 50 kHz to over 1 MHz. The oscillator requires an external resistor and capacitor to determine the operating frequency—the equation is:

$$1/F_O = T = C_T \bullet (1.5 \bullet R_T + 728).$$

With a 6 kΩ timing resistor and a 200 pF timing capacitor, the formula calculates the operating frequency at 514 kHz. At higher operating frequencies, the oscillator frequency deviates from this equation due to switching delays. *Figure 1* shows the oscillator frequency for different combinations of timing capacitors and resistors.

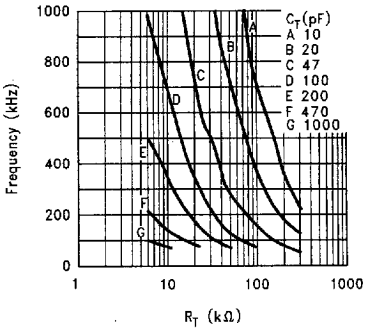

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FIGURE 1. Frequency vs R_T and C_T Graph

Functional Description (Continued)

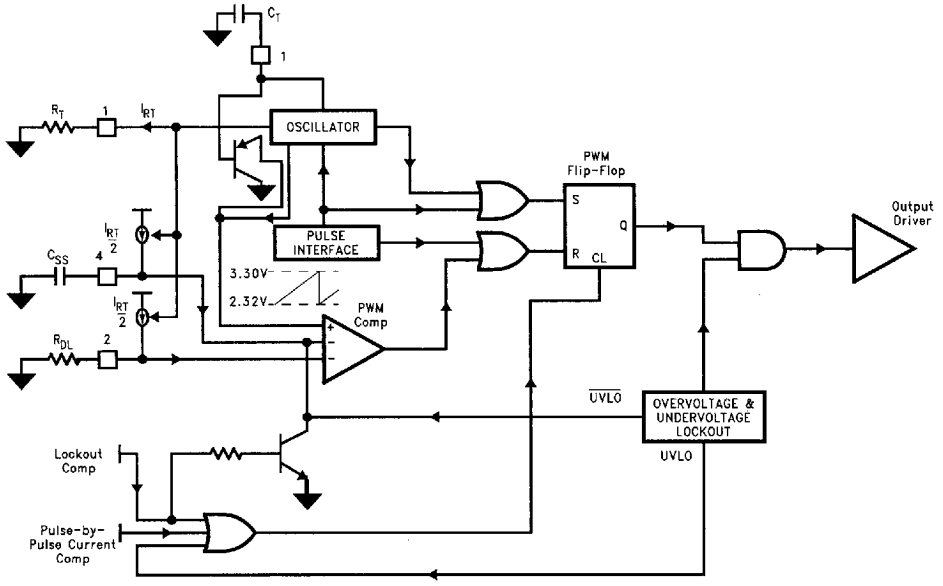

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FIGURE 2. PWM Block Diagram

PULSE-WIDTH MODULATOR SECTION

The pulse-width modulator (PWM) section consists of the PWM comparator and the PWM flip-flop (see *Figure 2*). During normal pulse feedback operation, the pulse interface circuit will set or reset the PWM flip-flop, which in turn, will latch on or off the output driver (see the timing diagrams in the pulse interface section of the Application Hints section). During start-up, or opto-coupler feedback operation, the oscillator will set the PWM latch, and the PWM comparator will reset the latch.

PWM COMPARATOR CIRCUIT

The PWM Comparator is fed by several different inputs. The inverting inputs are the duty cycle limit input (R_{DL}), and the Soft-Start (C_{SS}). The non-inverting input comes from the external timing capacitor, C_T. The sawtooth waveform at C_T is adjusted up one base-emitter junction voltage, and applied to the non-inverting input. Hence, this input is a sawtooth waveform oscillating between 2.32V to 3.3V. The level-shifted oscillator ramp voltage is compared to the two inverting inputs. The lowest input determines the PWM comparator output and thus the state of PWM flip-flop. The PWM flip-flop controls the output driver, driving it on or off.

DUTY CYCLE LIMIT

Duty cycle limit can be used for either pulse or opto-coupler feedback systems. A current mirror delivers one-half of the timing resistor current to the R_{DL} input. Inserting a resistor from this pin to ground will produce a voltage, that is compared to the oscillator ramp voltage. The result limits the duty cycle of the regulator circuit. The maximum duty cycle can be calculated using the following equation:

$$D_{MAX} = [R_{DL}/(1.71 \bullet R_T)] - 1.82$$

For instance, if the R_{DL} input had a 23.3 kΩ resistor connected to it, and the timing resistor was 6 kΩ, the maximum duty cycle would be approximately 45%.

Conversely, if a known maximum duty cycle was desired, the calculation for R_{DL} would be:

$$R_{DL} = R_T [(1.71 \bullet D_{MAX}) + 3.11]$$

For example, a 30% duty cycle (and a 6 kΩ timing resistor) would result in a R_{DL} of 21.7 kΩ.

To disable the duty cycle limit, the voltage at the R_{DL} pin must be greater than 3.3V. The graph in *Figure 3* shows the maximum duty cycle for a range of R_{DL} resistor values.

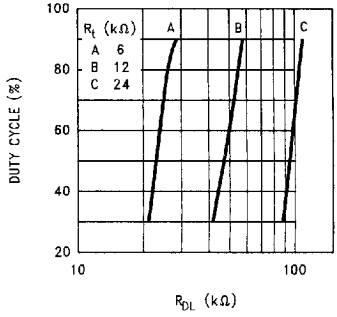

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FIGURE 3. Maximum Duty Cycle vs R_{DL}

Functional Description (Continued)

SOFT-START

The Soft-Start function limits the duty cycle at start-up. At start-up, a current source charges the Soft-Start capacitor with a current that is half the current that flows through the timing resistor (see the PWM block diagram). Before the Soft-Start voltage reaches 2.32V, the low voltage level of the timing capacitor peak-to-peak voltage, the PWM comparator delivers a high signal to the reset input of the PWM flip-flop (see the timing diagram in *Figure 4*). This forces it and the output driver off. At the point where the Soft-Start voltage reaches 2.32V, the PWM comparator changes its output state, turning on the PWM flip-flop and the output driver. However, the Soft-Start circuit still limits the duty cycle. The duty cycle will progressively get longer with each cycle, until either the duty cycle limit is reached or the feedback signal takes control of the PWM circuit.

The formula for the Soft-Start time delay (the time the voltage at the Soft-Start pin reaches the 2.32V level) is:

$$t_D = 2 \bullet C_{SS} \bullet R_T.$$

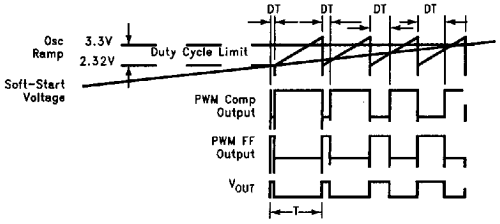
After this time delay, the Soft-Start circuit limits the rise of the duty cycle. The amount the duty cycle rises to, and the time spent getting there, both depend on whether the duty cycle limit voltage level (V_{RDL}) or the current limit voltage level (V_{CLIM}) assumes control of the duty cycle first during start-up. Assuming the duty cycle limit voltage level is the Soft-Start voltage threshold during start-up, then the speed at which the duty cycle achieves its maximum level is:

$$D_{MAX}/t_{SS} = 0.71/(C_{SS} \bullet R_T).$$

And if the rise time is known, then the Soft-Start capacitor can be calculated as:

$$C_{SS} = (0.71 \bullet t_{SS})/(D_{MAX} \bullet R_T).$$

The Soft-Start circuit has a clamp voltage of 4.2V. Leaving the pin open will disable the Soft-Start function.



TL/H/11435–9

FIGURE 4. Soft-Start Timing Diagram

PULSE INTERFACE SECTION

Figure 5 shows the block diagram of the pulse interface section. The pulse interface circuit will take AC coupled feedback pulse signals and set or reset the PWM flip-flop, depending upon whether the pulse signal is positive or negative—a positive pulse will set the flip-flop, a negative one will reset it. In turn, the flip-flop will turn on or off the output driver. Hence, the feedback signal through the pulse interface circuit will control the LM3001 operating frequency and duty cycle (in steady-state operation).

The AC-coupled current pulses can be as low as 0.3 mA (guaranteed), and as narrow as 15 ns (typical). The minimum time between pulses is approximately 10 ns. The maximum current pulse that the feedback pin can handle is 4 mA. Feedback signals beyond 4 mA can either cause improper operation or catastrophic failure of the LM3001. The time delay between when the feedback pulse signal is received and when the output gate drive signal changes state is 28 ns typically.

During start-up of an isolated offline converter, once a positive AC-coupled feedback signal is applied to the pulse interface circuit, the circuit will synchronize the internal oscillator to the feedback signal frequency. The same signal will also turn on the output driver. If, after the pulse feedback was established and for any reason it was terminated, the output would deliver the signal that was set by the last pulse sent by the feedback circuit. For example, if the output driver was set high, and the LM3001 did not receive any further feedback pulses, then the output driver would stay turned on. Either the current limit circuit or the duty cycle limit circuit would shut down the output under these circumstances.

OUTPUT DRIVER SECTION

The Output Driver is a totem pole output stage that can supply or sink 2.5A peak currents at speeds less than 20 ns. That is enough current to charge or discharge thousands of picofarads of load capacitance, which is present when driving Power MOSFETs. The saturation voltages of the internal power transistors are typically 1.5V from the rails when sourcing or sinking 400 mA.

A demonstration of the drive capability of this output stage is shown in *Figure 6*. The drawings show the output stage driving different values of load capacitance during pulse feedback operation. As shown, with a load capacitor value of 1,000 pF, the rise time is typically 11 ns, and the fall time is typically 8 ns. The supply voltage in all cases was 15V.

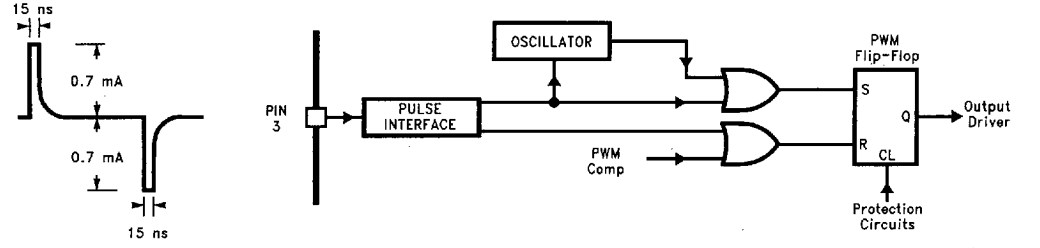


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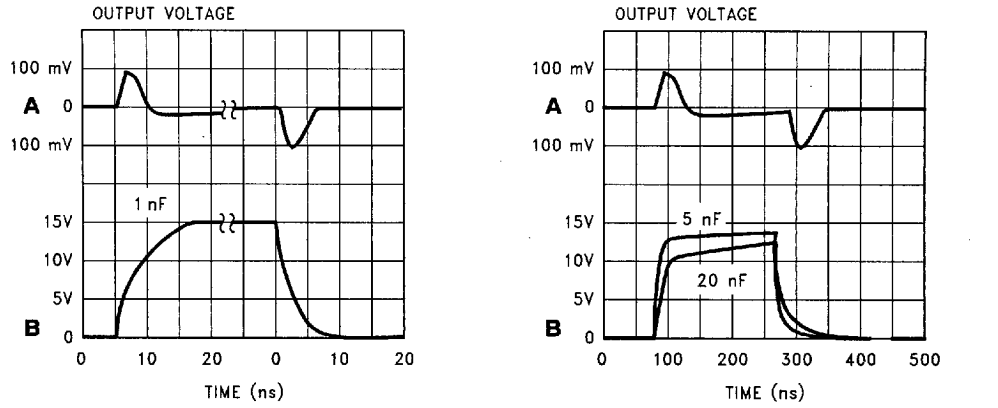
FIGURE 5. Pulse Interface Block Diagram

Functional Description (Continued)



TL/H/11435–11

A: Pulse Feedback Voltage, 100 mV/div. (AC Coupled)
B: Output Voltage, 5V/div.

FIGURE 6. Output Voltage Rise and Fall Times

CURRENT LIMIT SECTION

There are two circuits in the LM3001 that limit the peak primary current. One executes pulse-by-pulse current limiting, and the other is a total shutdown current limit, which shuts down the output driver (and thus, the Power MOSFET) for a programmable amount of time. Both current limit circuits monitor the peak primary current by comparing the voltage on the CLIM input (pin 6) against two different voltage thresholds.

The voltage threshold for the pulse-by-pulse current limit is 0.38V (typical). When that threshold voltage is reached, the pulse-by-pulse current comparator turns off the present Power MOSFET gate drive by sending a high signal to the clear input of the PWM flip-flop. The current limit circuit will activate again during the next cycle, if the 0.38V threshold is exceeded again.

The voltage threshold for the total shutdown current limit is 0.6V. When that current limit comparator is activated, it forces the inverting input of the lockout comparator low (to about 0.7V) by driving a Darlington transistor into saturation. With the other input connected to a 2.1V reference voltage, the lockout comparator outputs a high signal to the PWM flip-flop clear input (via the OR gate). A high signal at its clear pin shuts down the PWM flip-flop and thus, the output driver. The output driver will remain off until the voltage level at the lockout comparator inverting input becomes larger than the voltage at its non-inverting pin (because the shutdown delay has expired and the voltage at the CLIM pin is less than 0.6V).

The shutdown delay is controlled by an external capacitor (on the C_{SD} pin—pin 5) and an internal current source connected to the inverting input of the lockout comparator (the current source delivers approximately half the current through the timing resistor). The current source will charge the capacitor until its voltage is internally clamped at about 3.0V. When the capacitor voltage reaches the reference voltage, the Lockout Comparator will change its output from a high to a low signal. This action will release the PWM flip-flop and the output driver, enabling them to resume normal operation (assuming the problem causing the current limit has been corrected. If not, normal operation will be halted again).

The time the PWM flip-flop and the output driver remain shutdown is programmable, depending on the value of the C_{SD} capacitor. Rearranging the shutdown time delay equation, giving in the pin-by-pin description section, results in a calculation of the capacitor value:

$$C_{SD} = t_{SD}/(2 \bullet R_T).$$

For example, for a desired shutdown delay time of approximately 100 μs and a R_T equal to 6 kΩ gives a C_{SD} of 8200 pF. The shutdown delay circuit is temperature compensated, so the delay time is stable over temperature. Also, after a total shutdown, the IC will repeat the Soft-Start cycle when the shutdown delay time has elapsed.

If the shutdown delay feature is not desired, leaving the pin open will disable the function (the pin voltage is internally clamped to 3V, thereby holding the lockout comparator output low).

Functional Description (Continued)

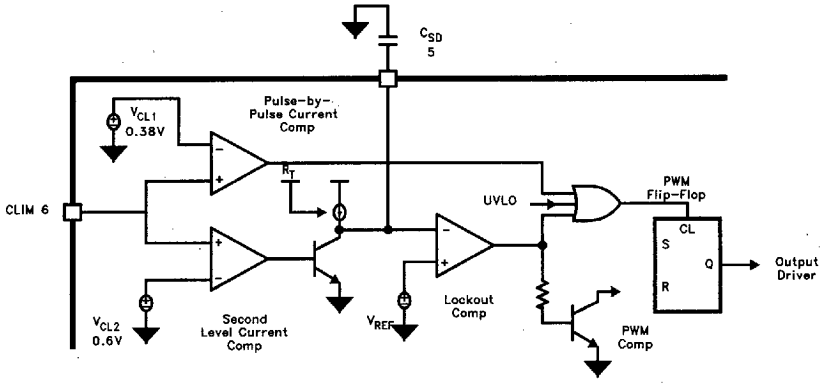


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FIGURE 7. Current Limit Block Diagram

OVERVOLTAGE/UNDERVOLTAGE SHUTDOWN SECTION

The Overvoltage and Undervoltage Lockout circuits protect the LM3001 from deviations of the supply voltage. The Overvoltage Lockout (OVL) circuit monitors the supply voltage via an external resistor divider (for more information, see the OVL section in the Application Hints section). The Overvoltage Lockout Threshold voltage is 3.30V (typically). When an overvoltage condition occurs, the OVL circuit shuts down the Output Driver (the rest of the IC stays on) until the fault causing it disappears. The Thermal Shutdown protection circuit uses the same circuitry to shut down the Output Driver and the entire regulator.

The Undervoltage Lockout (UVL) circuit monitors the supply voltage from within the IC. At start-up, the UVL is turned on when the supply voltage reaches approximately 2.0V. The UVL circuits keeps the rest of the IC off until the supply voltage reaches approximately 11.8V. The start-up supply current during this period is about 190 μA. Hysteresis (about 3.2V) is added to the circuit so that the supply voltage must decrease to 8.6V (typical) before the UVL circuit shuts down the IC. When the UVL circuit is activated, the rest of the IC and the entire regulator are turned off, and the UVL and bandgap reference voltage circuits are the only two internal circuits left on. The UVL circuit will also discharge the Soft-Start capacitor, so Soft-Start will commence at the next start-up.

SIGNAL GROUND AND POWER GROUND

The LM3001 Primary-Side PWM Driver is designed with two separate grounds inside that meet in one location—right at the pins. One ground is for small signals—hence, it is very clean (noise-free). The other ground is the power ground, used by the large signals of the Output Driver. The two grounds are internally connected at the pins; pin 9 is a power ground and pin 11 is a signal ground. The grounds should be isolated from each other on the board (see the PCB Layout section in the Application Hints section).

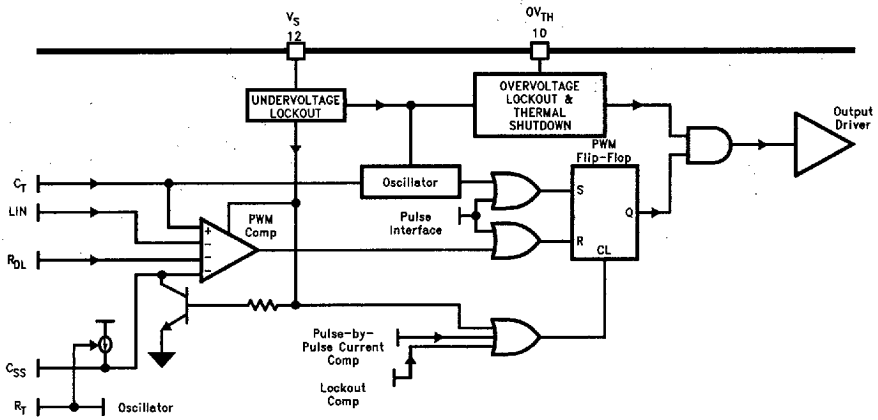

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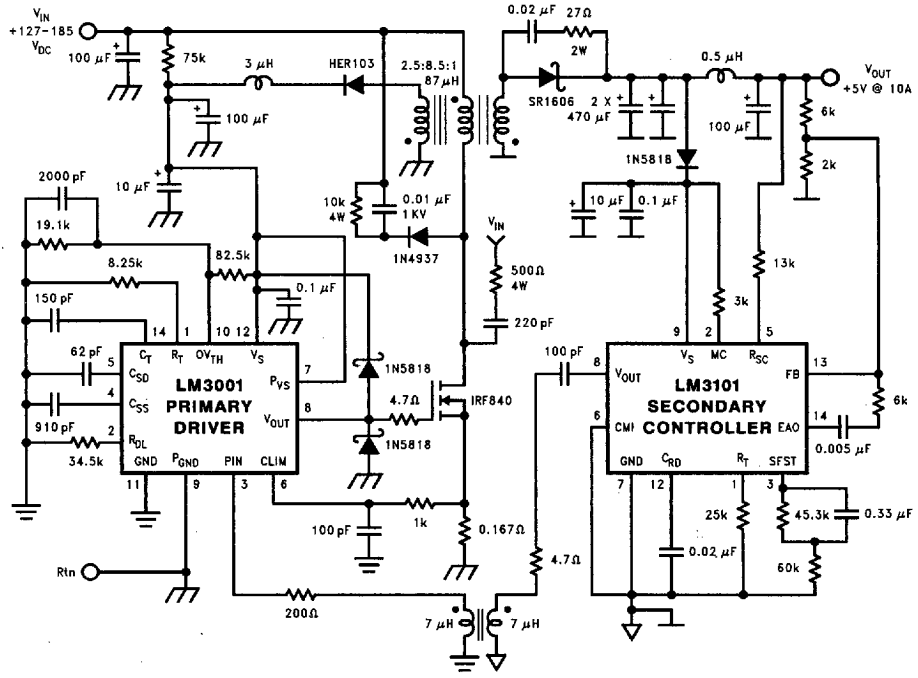
FIGURE 8. Overvoltage/Undervoltage Block Diagram

Typical Application



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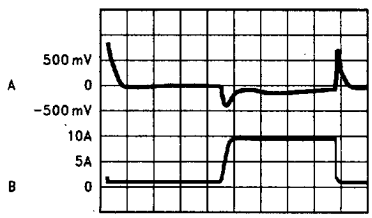
CAUTION: HIGH VOLTAGE
Handle with Extreme Care

FIGURE 9. Offline Voltage Mode Flyback Regulator

This 500 kHz Offline Converter delivers 50W (5V @ 10A) from an input supply ranging from 90 VAC to 130 VAC (130 VDC to 180 VDC). The regulator achieves a line regulation of 0.06% and a load regulation of 0.05%. A 0.5 µH inductor and 100 µF capacitor form an LC filter that reduces the output ripple voltage to 50 mV. As shown in *Figure 10* the regulator can respond to a "step" change in load current from 1A to 10A in about 12 µs. The efficiency of the converter is approximately 80% at full load.



TL/H/11435–15

A: Output Voltage, 500 mV/div., AC Coupled
B: Load Current, 5A/div.
Horizontal Time Base: 20 µs/div.

FIGURE 10. Load Step Response

Typical Application (Continued)

POWER STAGE OPERATION

The LM3001 Primary-Side PWM Driver sends a pulse-width-modulated signal (via pin 8) to a power switch, which in turn, drives a power transformer.

The power switch used in this case is an IRF840 Power MOSFET. It is an N-Channel enhancement mode device that has a drain-to-source voltage (V_{DSS}) rating of 500V and a pulsed drain current (I_{DM}) rating of 32A. Even though the Power MOSFET has a high V_{DSS}, snubber circuits are needed to limit the drain voltage and damp out any ringing that may occur.

The power transformer has a primary inductance of 87 μH. The primary-to-secondary turns ratio is 8.5 to 1 and the secondary-to-tertiary turns ratio is 1 to 2.5. The tertiary winding delivers the LM3001 supply voltage (pins 7 and 12) to the primary-side driver.

There is an internal Overvoltage Threshold circuit (pin 10) monitoring the input voltage via a resistor divider. The overvoltage trip point is 3.3V typically. With the resistor values shown, the maximum supply voltage is approximately 17.5V.

The output rectifier, an SR1606, delivers the secondary current to the output. The SR1606 is specified for 16A forward current, 60V reverse breakdown voltage, and comes in a TO220-AB package. Since the SR1606 dissipates 7W to 8W at full load, it requires a heatsink. An RC snubber is placed in parallel to reduce the ringing voltage caused by the output rectifier turning off during the discontinuous mode of operation.

Two Cornell Dubilier type 226 470 μF, 25V high frequency capacitors, with low ESRs of 0.25Ω, are used as the output capacitors.

OUTPUT VOLTAGE CONTROL

The output voltage is controlled by the LM3101 Secondary-Side PWM Controller. The LM3101 uses its error amplifier to compare the scaled-down output voltage against the internal precision 1.24V reference voltage. The error amplifier provides compensation for the regulator frequency response, by way of an RC feedback network.

The resulting error voltage is converted into a pulse-width-modulated waveform at the system oscillator frequency of approximately 500 kHz. This waveform is then differentiated (using an external high-pass RC filter) into a series of positive and negative pulses representing the desired switch duty cycle.

The pulses are transferred through a pulse transformer to the LM3001 Primary-Side Driver. The driver takes the feedback pulse signal and converts it into a PWM gate drive for the Power MOSFET.

FAULT RECOVERY OPERATION

A 0.15Ω resistor sets the peak primary current limits to 2.28A for the pulse-by-pulse limiting, and to 3.6A for the second-level limit. An RC network filters the current limit voltage to prevent the current limit (pin 6) from being activated by the reverse recovery spike of the output rectifier. When the second level current limit is triggered, the LM3001 shuts down and discharges the capacitor connected to pin 5 (the Shutdown Delay capacitor). After the capacitor is recharged to a voltage of approximately 2.1V, the device will try to restart. If the overcurrent condition persists, the device will shut down again.

The LM3101 provides the fault protection in case of an output short circuit. During normal operation, the operating frequency of this circuit is determined by 25 kΩ resistor connected to pin 1 of the LM3101. However, during a short circuit condition on the output, the frequency of the LM3101 (and the entire circuit operating frequency) drops, yielding a very low duty cycle. This short-circuit frequency is set by the 13 kΩ resistor connected to pin 5.

The LM3101 Mode Control and Current Mode Input pins (pins 2 and 6 respectively) are for current mode control operation. The MCR pin determines which control mode is being used—the resistor tied to the supply voltage means voltage mode control (the resistor tied to ground would indicate current mode control).

START-UP OPERATION

When power is initially applied to the regulator, the LM3001 Primary-Side PWM Driver receives its supply current through a 75 kΩ resistor connected to the input voltage (see *Figure 9*). Once the supply pin voltage reaches the threshold of 11.8V (typical), the LM3001 turns on, sending pulse signals (with an amplitude of approximately 10V) to the gate of the Power MOSFET. Because the output is driving Power MOSFETs, which need gate-to-source voltages greater than 10V for hard turn-on (low $R_{DS\ (ON)}$) the threshold voltage of 11.8V was selected to insure sufficient output voltage.

At the beginning of the start-up process, the secondary side of the regulator is still unbiased—hence the LM3001 does not receive a feedback signal from the secondary side (see the Start-Up Sequence in *Figure 11*). Before the LM3101 Secondary-Side PWM Controller is controlling the circuit, the initial operating frequency of the gate drive is determined by the LM3001 internal oscillator. The oscillator uses an external capacitor and resistor, on pins 14 and 1 respectively. The initial operating frequency in this case is approximately 500 kHz. During this time, the regulator is operating in a "free-running" state.

Also during the beginning, the LM3001 executes Soft-Start by using the Soft-Start capacitor on pin 4. The voltage across this capacitor is compared to the oscillator ramp on pin 14 (see the LM3001 block diagram). In the offline regulator, the Soft-Start time is 15 μs approximately.

During this time, as the Soft-Start capacitor charges up, the duty cycle increases with each progressive cycle, until finally the duty cycle reaches its maximum value set by the Duty Cycle Limit circuit (R_{DL}—pin 2) and the Current Limit circuit (CLIM—pin 6). The Soft-Start phase ends when the duty cycle is limited by the R_{DL} circuit. A resistor at this pin connects to an internal current source which together will generate a voltage that will be compared to the oscillator ramp voltage. This comparison will determine the maximum duty cycle during this phase of the start-up cycle. For the circuit in *Figure 9*, the duty cycle is limited to 63% by the R_{DL} circuit.

The duty cycle will reach the R_{DL} limit for several cycles, letting energy build up in the transformer—see the drain current waveform in *Figure 11*. When the residual energy builds up enough, the duty cycle starts to decrease because it is now determined by the CLIM circuit. A voltage of 0.38V or greater at this pin will toggle a pulse-by-pulse comparator on every cycle (see the LM3001 block diagram). In the ap-

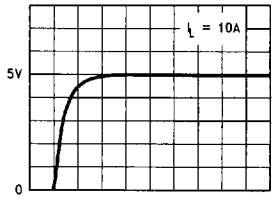
Typical Application (Continued)

plication circuit, a 0.167Ω resistor will generate the current limit threshold voltage when a 2.28A (peak) current flows through it. With the CLIM circuit in control of the duty cycle, the duty cycle will decrease with each sucessive cycle. The duty cycle will continue to shrink until the pulse feedback from the LM3101 takes control.

As the LM3001 switches the Power MOSFET on and off, the Power Transformer starts delivering power to the secondary side of the circuit. This action will cause the supply voltage of the LM3101 and the output voltage to gradually rise. When the supply voltage reaches the Undervoltage Lockout Threshold (of 3.9V), the LM3101 starts supplying a pulse train to the differentiator circuit on pin 8. The resulting PWM signals are fed back to the LM3001 via the pulse transformer. The first pulse signal to the LM3001 will cause it to disconnect its internal oscillator from its PWM and Output Driver circuits and trigger the Output Driver from the pulse feedback signals (of the LM3101). At this point, control of the frequency and the duty cycle changes from the LM3001 to the LM3101.

The LM3101 also exercises Soft-Start capability (pin 3). An RC network connected to this pin allows the LM3101 to gradually increase the duty cycle to its nominal value (in the example, the secondary Soft-Start time delay is 500 μs approximately).

The method of Soft-Start used by the LM3101 ensures that the error amplifier is in its linear region before the output voltage reaches its nominal value, thus yielding a smooth start-up of the output without any overshoot (see *Figure 12*).

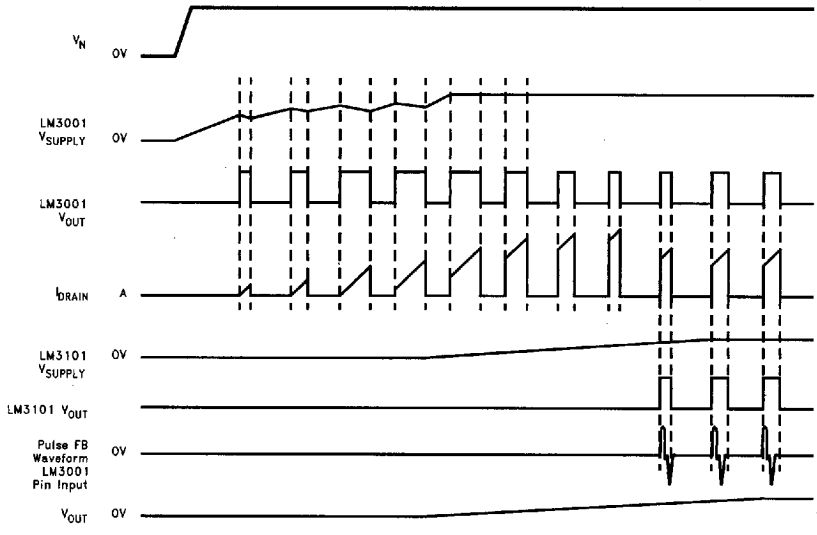


TL/H/11435–17

Output Voltage, 1V/div.
Horizontal Time Base: 500 μs/div.

FIGURE 12. Output Voltage Start-Up

At the end of the start-up sequence. the circuit is in steady-state or normal PWM operation.



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(Representative not to scale)

FIGURE 11. Start-Up Timing Sequence

Typical Applications (Continued)

DESIGN PROCEDURE

For the Offline Voltage Mode Flyback Regulator (*Figure 9*), the specifications for the power transformer, MOSFET switch, the switch snubber, and the output rectifier can be calculated based on the system specifications:

System Specifications:

V_O = 5 VDC

V_I Range = 90 VAC–132 VAC

I_O Range = 0.5A–10A

Efficiency (η) = 80%

F_O = 500 KHz

Transformer Specifications

Manipulating the transfer function of a flyback regulator results in a calculation for the turns ratio of the power transformer, involving the minimum input voltage, the output voltage, and the maximum duty cycle (D):

$$V_O + V_F = (V_{IN(MIN)} - V_{SW(ON)}) \bullet (N_S/N_P) \bullet (D_{(MAX)}/(1 - D_{(MAX)}))$$

$$\downarrow$$

$$N_S/N_P = [(V_O + V_F)/(V_{IN(MIN)} - V_{SW(ON)})] \bullet ((1 - D_{(MAX)})/D_{(MAX)}).$$

Assume that the diode forward voltage (V_F) is about 0.7V and the drain-to-source voltage when the switch is on ($V_{SW(ON)}$) is approximately 0.9V. Selecting a 28% maximum duty cycle results in a turns ratio of:

$$N_S/N_P = (5.7V/126.1V) \bullet (1 - 0.28)/0.28 = 0.12 \quad (N_P/N_S = 8.5/1).$$

Assuming an efficiency (η) of 80%, the average input current (at the maximnum load current andd for the entire period) is:

$$I_{IN} = (V_O)\,(I_O)/(V_{IN(MIN)} \bullet \eta) = (50W)/(127V \bullet 0.80) = 0.49A.$$

The average current when the switch is on is the average current over the entire period divided by the duty cycle:

$$I_{IN(TON)} = I_{IN}/D = (0.49A)/(0.28) = 1.77A.$$

Selecting the primary inductance ripple current (ΔI_P) to be a certain percentage of the $I_{IN(TON)}$, and combining that with the duty cycle, the input voltage, and the operating frequency, gives the primary inductance by the equation:

$$L_P = (V_{IN(MIN)} - V_{SW(ON)}) \bullet D_{(MAX)}/(\Delta I_P \bullet F_O)$$

Assuming the percentage to be 46% in the example, then:

$$L_P = 126.1V \bullet 0.28/(0.81A \bullet 500\ kHz) \cong 87\ \mu H.$$

MOSFET Parameters

The peak current through the primary inductance and the Power MOSFET is the average current when the switch is on plus one-half the primary inductance ripple current:

$$I_{PRI(PK)} = I_{IN(TON)} + (\Delta I_P/2) = 1.77A + (0.81A/2) = 2.18A$$

Assuming ideal conditions, the maximum voltage at the drain of the Power MOSFET when the switch is off is:

$$V_{SW\,(OFF)} = (V_O + V_F)\,(N_P/N_S) + V_{IN(MAX)} = (5.7V)\,(8.5) + 185V = 233V \rightarrow 250V.$$

However, leakage inductance exists in the transformer, causing a voltage spike immediately after the switch turns off. This voltage spike will add to the rest of the drain voltages, making $V_{SW(OFF)}$ even greater. With a leakage inductance that is 2% of the transformer primary inductance and selecting a switch which has a fall time of 2% the total off-time, the added voltage will be:

$$V_{LL} = 2\% \bullet L_P \bullet I_{PRI(PK)} \bullet F_O/[2\% \bullet (1 - D_{(MAX)})].$$

The maximum duty cycle of 28% is used for worst case purposes. Thus, the leakage inductance voltage spike is:

$$V_{LL} = 0.02 \bullet 87\ \mu H \bullet 2.18A \bullet 500\ kHz/[0.02 \bullet (1 - 0.28)] = 130V \rightarrow 150V.$$

This means the actual peak drain voltage is approximately 400V. When choosing the Power MOSFET, add some margin to this number. A 500V MOSFET was used in this application.

Snubber Design

A "snubber" circuit, consisting of a 1N4937 fast recovery diode and a parallel RC network, is inserted around the transformer primary to clamp the voltage spike. This is to the reduce the switch voltage stress when it is off. The "snubber" components are calculated in the following manner:

$$C_{SN} \geq 0.02 \bullet L_P \bullet I_{P(PK)}{}^2/(V_{MAX}{}^2 - V_{SN}{}^2) = 0.02 \bullet 87\ \mu H \bullet (2.18A)^2/[(255V)^2 - (250V^2] \approx 3.3\ nF$$

and

$$R_{SN} \leq [(V_{MAX} + V_{SN} - V_{IN})/2]^2 \bullet [100/F_O \bullet L_P \bullet I_{P(PK)}{}^2)] = [(255V + 250V - 185V)/2]^2 \bullet [100/(500\ kHz \bullet 87\ \mu H \bullet (2.18A)^2)] \approx 12\ k\Omega.$$

In the Offline Flyback Regulator application, a 0.01 μF capacitor and a 10 kΩ resistor are used as the snubber components. V_{MAX} is the selected maximum voltage at the drain of the MOSFET. Usually the RC values are selected so that V_{MAX} is 5V to 10V higher than V_{SN}. The power dissipation of the resistor is:

$$P = [(V_{MAX} + V_{SN} - V_{IN})/2]^2/R = [(255V + 250V - 185V)/2]^2/10\ k\Omega = 2.56W.$$

To add some margin, a 4W resistor is chosen.

The fast recovery diode must have a reverse voltage rating greater than V_{MAX}. The 1N4937 has a 600V rating.

Output Diode Parameters

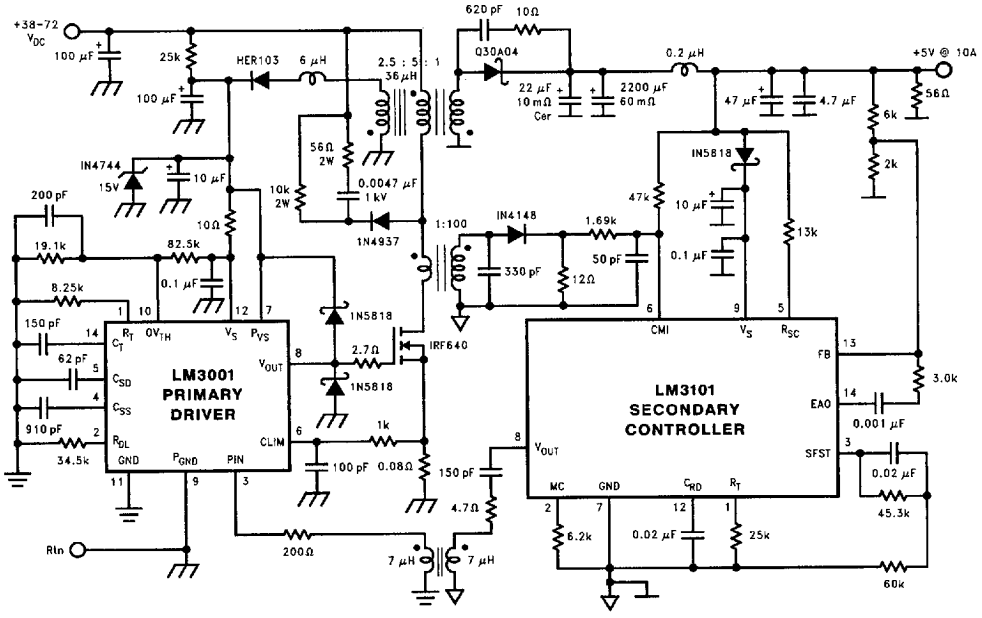
The peak secondary current can be calculated using peak primary current and the turns ratio (this equation is for single output flyback regulators):

$$I_{SEC(PK)} = I_{PRI(PK)} \bullet (N_P/N_S) = 2.18 \bullet 8.5 = 18.43A \rightarrow 20A.$$

The maximum average current through the secondary and the diode, when the switch is off, is the maximum load and current divided by the inverse of the duty cycle:

$$I_{SEC(OFF)} = I_{LOAD}/(1 - D_{(MAX)}) = 10A/0.72 = 13.90A \approx 15A.$$

Typical Application (Continued)



TL/H/11435–18

FIGURE 13. Telecom Current Mode Flyback Regulator

The maximum average secondary current for the entire period is the maximum load current (10A).

The maximum reverse-bias voltage on the output rectifier is:

$$V_{RV} = V_{IN(MAX)} \bullet (N_S/N_P) + V_O + V_F = (185V)\,(1/8.5) + 5.7V = 27.42V \approx 30V.$$

A suitable diode for this circuit is the SR1606, which has a reverse voltage rating of 60V and an average current rating of 16A.

Application Hints

TELECOM CONVERTER

The schematic of a flyback regulator, used in Telecom Applications, is shown in *Figure 13*. The circuit has many of the component values that are in the offline converter. Notable exceptions are the power transformer, in which the turns-ratio and primary inductance has changed (due to the change in the input voltage range), and the Power MOSFET, which has a lower on-resistance and a lower breakdown voltage rating.

The most significant difference in the circuit design is the change in the mode of operation—from voltge mode to current mode. For current mode operation, the LM3101 Mode Control pin (MC—pin 2) is connected to ground by a 6 kΩ resistor, and the Control Mode pin (CMI—pin 6) is connected to the current sense transformer through a half-wave rectifier circuit and a low-pass filter. The filter is needed to remove the leading edge spike on the current waveform, caused by the rectifier recovery and interwinding capacitance of the power transformer.

Smaller component differences include reducing the current sensing resistor in the primary side ground path (to allow for the larger primary current), and removing a primary side snubber circuit (due to smaller peak voltages at the drain). Also, the output rectifier and Power MOSFET snubbers are modified.

Application Hints (Continued)

PULSE FEEDBACK SECTION

During steady-state operation, the LM3101 delivers pulse-width modulated signals to the feedback circuit. The feedback circuit will convert that signal into a series of AC-coupled pulse signals and apply them to the LM3001 via the pulse transformer (the first positive-edged pulse from the LM3101 will cause the LM3001 to disconnect its internal oscillator from its PWM and Output Driver circuits). The feedback pulses will trigger the LM3001 Output Driver to apply PWM drive signals to the Power MOSFET gate. The timing diagram in *Figure 14* demonstrates the feedback communication.

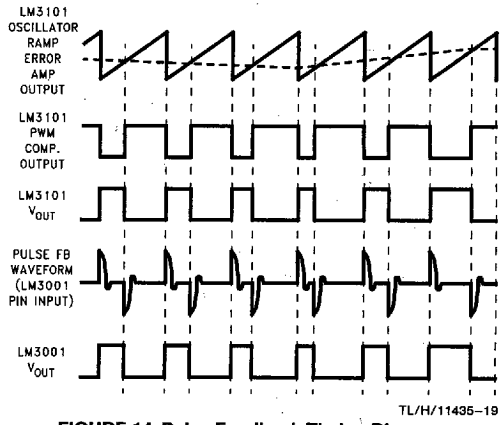


FIGURE 14. Pulse Feedback Timing Diagram

PULSE INTERFACE CIRCUIT

The pulse interface circuit provides isolation for the feedback circuit of the Offline Flyback Regulator. The differentiator circuit converts the PWM waveform into a pulse train. The differentiator delivers to the pulse transformer a train of 1 V_{PK}, 15 ns wide pulses. The core should have high permeability (typically 10,000) at the switching frequency to allow the transfer of energy with a very small transformer (size). This one-to-one transformer transfers the pulse train to the LM3001 via a 200Ω resistor, which is used mainly to filter noise from the system.

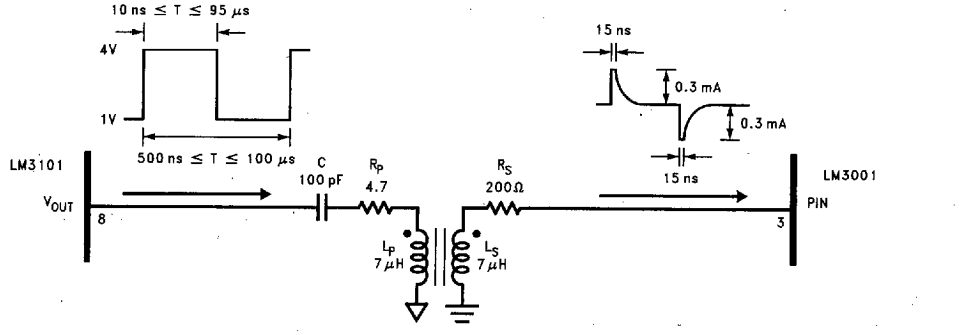


FIGURE 15. Pulse Interface Circuit

Application Hints (Continued)

CURRENT LIMIT

As previously mentioned, the primary current can be monitored by inserting a resistor between the source of the Power MOSFET and ground (See General Circuit Operation section). This generates a voltage which is compared to the reference voltages of the pulse-by-pulse current limit comparator (0.38V) or the second level current limit comparator (0.6). As an example, using a 0.1Ω will allow a peak primary current of 3.8A to activate the pulse-by-pulse current limit. A peak primary current of 6A will activate the total shutdown current limit. Also mentioned before, after the second level current limit threshold has been reached, there will be a time delay before the circuit powers up again. This shutdown delay is controlled by the Shutdown Delay capacitor (the equation for this is in the Current Limit section of the Functional Description section). In the example, a shutdown delay capacitor of 1 μF and a timing resistor of 8 kΩ produces a time delay of 10 ms before the regulator starts up again:

$$T_{SD} = 1.25 \bullet 1\ \mu F \bullet 8\ k\Omega = 10\ ms$$

The voltage generated across the current-sensing resistor needs to be filtered before it is applied to Current Limit circuit input. The filtering is needed because of current spikes, caused by the transformer leakage inductance, during the turn-on of the Power MOSFET. The filter that is used in the regulator in the General Circuit Operation section is a RC low pass filter with a 0.62 μs time constant. This filter is fast enough to allow proper operation of this function, but will screen unwanted transient signals. Note that the lower the leakage inductance the transformer has, the faster the filter can be.

Usually, it is the filter that determines the response time of the current limit activation. If the filter can be made fast enough (less than 40 ns) due to low leakage inductance, then the response time of the current limit circuit comes into play. The Current Limit Delay Time is specified at 50 ns for 100 mV of "overdrive" (the term "overdrive" means the amount of voltage over the comparator's threshold voltages). However, the speed or response time in which the current limit circuit acts and shuts down the output depends on the amount of "overdrive" caused by an excessive primary current. However, the amount of voltage driving the current limit input directly affects the speed or response time of the current limit circuit. The higher the overdrive, the faster the output is turned off. The graph below demonstrates the relationship between the overdrive voltage and the speed of the current limit circuit. An overdrive of approximately 30 mV produces a response time of 58 ns, whereas a 250 mV overdrive generates a response time of less than 50 ns.

OVERVOLTAGE THRESHOLD

The supply voltage is monitored by the Overvoltage Shutdown circuit through a resistor divider. The current needed to bias the divider is delivered by the supply voltage. It is stated in the Overvoltage/Undervoltage Shutdown section that minimum bias current to insure proper operation is approximately 10 μA. This minimum bias current sets the maximum value of the resistor in the bottom leg of the divider. While there is not a maximum bias current limit as the LM3001 is concerned, the bias current should be kept as small as possible in order that the supply current is kept small.

BYPASS CAPACITORS

Due to the high speed and currents of this IC, high frequency noise can be generated very easily, causing erratic operation of the regulator. Hence, bypass capacitors must be used to eliminate the high frequency noise from interrupting the operation of the circuit. Capacitor values of 0.1 μF and 10 μF should be selected. The bypass capacitors should be placed as near as possible to the IC.

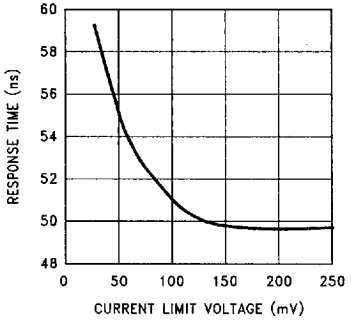


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FIGURE 16. Current Limit Response Time

Application Hints (Continued)

LM3001 WITH OPTO-COUPLER FEEDBACK

The LM3001 Primary-Side PWM Driver can also receive opto-coupler feedback as shown in *Figure 17*. A LM4041-ADJ Voltage Reference drives the opto-coupler's photodiode. The Error Amplifier of the LM4041 accepts a sample of the output voltage, from the resistor divider of R_1 and R_2, and supplies a drive current to the opto-coupler. Resistor, R_D, limits the maximum photodiode current. The RC network (C_C and $R_1 \parallel R_2$) provides compensation to the circuit.

The feedback signal from the opto-coupler is injected into the CLIM pin (pin 6). The opto-coupler's phototransistor, in an emitter follower configuration, supplies a current that produces a DC offset voltage at pin 6. A resistor, R_{CS}, generates a voltage proportional to the primary or switch current. These voltages are summed at pin 6. Referring to the LM3001 Block Diagram (on pg. 1), this summing voltage is compared to a 380 mV reference by the Pulse-by-Pulse Current Limit Comparator (see *Figure 18*). The R_F–C_F network provides filtering of the leading edge spikes.

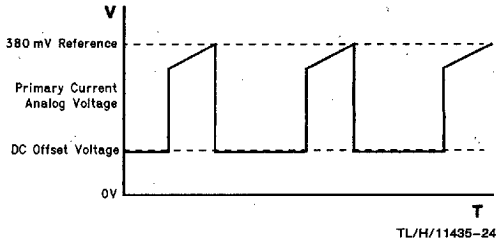

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FIGURE 18. Opto-Coupler Feedback Waveforms

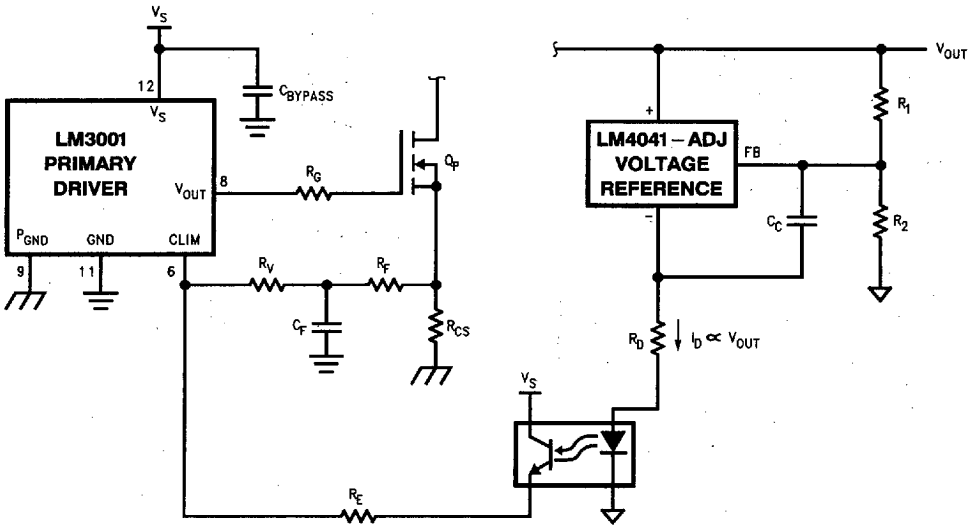

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FIGURE 17. Opto-Coupler Feedback Circuit

Application Hints (Continued)

LM3001 PCB LAYOUT

Due to the high speed of the LM3001 output driver, careful layout of the printed circuit board is essential. The ground plane should be divided into a power ground section (see *Figure 19*), connected to the PGND pin (pin 9) and an analog signal ground region, connected to the GND pin (pin 11). The separate ground sections are connected internally. The power ground region should have connected to it all paths carrying the high di/dt currents, such as the input return and the input capacitor negative lead.

High frequency bypassing is also a necessity. A 0.1 μF ceramic capacitor should be inserted between the output driver supply pin (P_{VS} – pin 7) and the P_{GND} pin. The analog signal supply pin (pin 12) should also be bypassed to its GND pin (V_S – pin 11) with a 0.1 μF ceramic capacitor. The bypass capacitors should be placed as near as possible to the IC, with the shortest possible lead length.

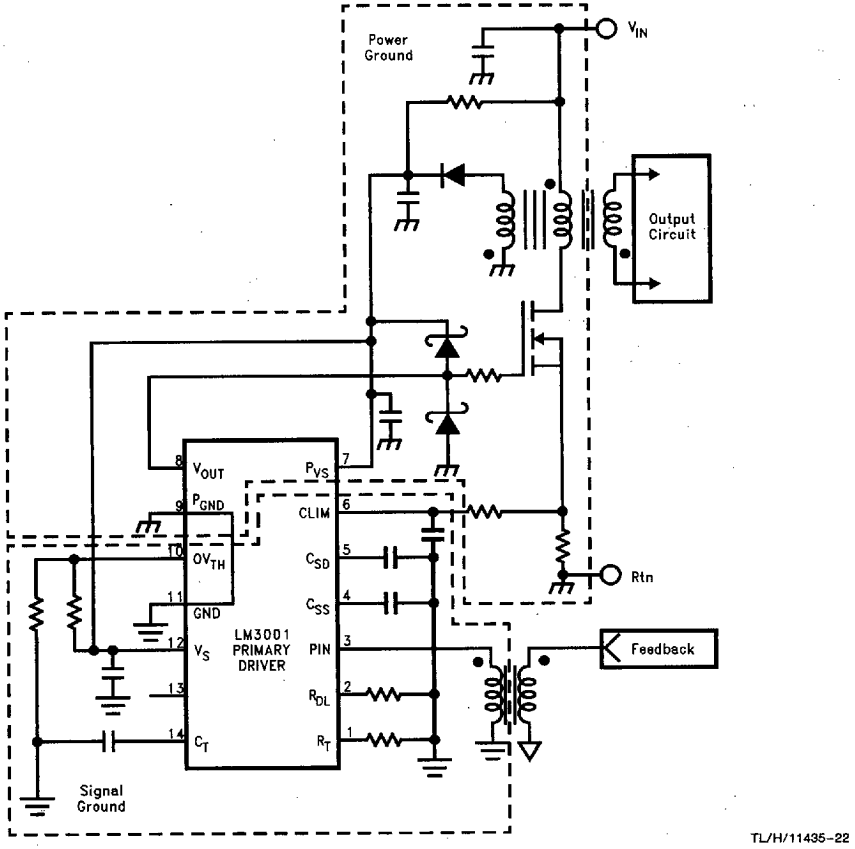

FIGURE 19. LM3001 PCB Layout