



9-BIT HOLD REGISTER

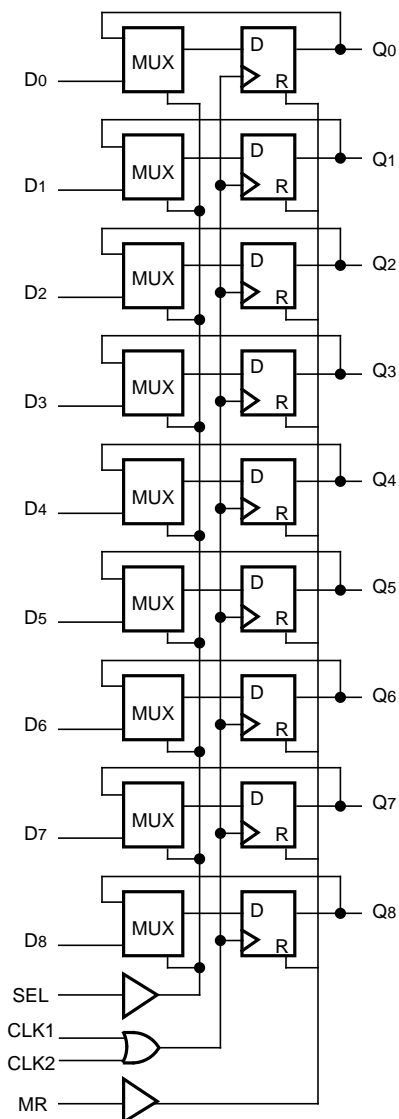
**SY10E143
SY100E143**

- 700MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 9 bits wide for byte-parity applications
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75kΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E143
- Available in 28-pin PLCC package

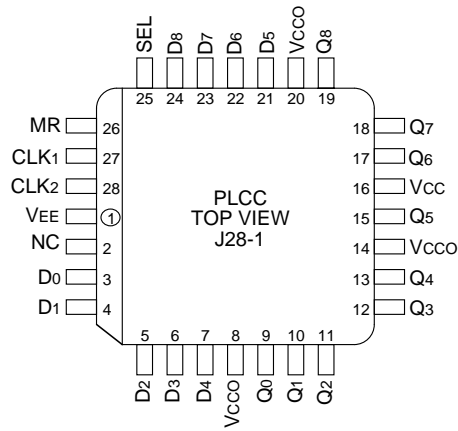
The SY10/100E143 are high-speed 9-bit hold registers designed for use in new, high-performance ECL systems. The E143 can hold current data or load new data. The nine inputs, D₀-D₈, accept parallel input data.

The SEL (Select) control pin serves to determine the mode of operation; either HOLD or LOAD. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK₁ or CLK₂. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E143 is designed for applications requiring high-speed registers, pipeline registers, synchronous operation, and is also suitable for byte-wide parity.



Pin	Function
D ₀ -D ₈	Parallel Data Inputs
SEL	Mode Select Input
CLK ₁ , CLK ₂	Clock Inputs
MR	Master Reset
Q ₀ -Q ₈	Data Outputs
NC	No Connection
V _{CC0}	V _{CC} to Output



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E143JC	J28-1	Commercial	SY10E143JC	Sn-Pb
SY10E143JCTR ⁽²⁾	J28-1	Commercial	SY10E143JC	Sn-Pb
SY100E143JC	J28-1	Commercial	SY100E143JC	Sn-Pb
SY100E143JCTR ⁽²⁾	J28-1	Commercial	SY100E143JC	Sn-Pb
SY10E143JZ ⁽³⁾	J28-1	Commercial	SY10E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E143JZTR ^(2, 3)	J28-1	Commercial	SY10E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E143JZ ⁽³⁾	J28-1	Commercial	SY100E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E143JZTR ^(2, 3)	J28-1	Commercial	SY100E143JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

SEL	MODE
L	LOAD
H	HOLD

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

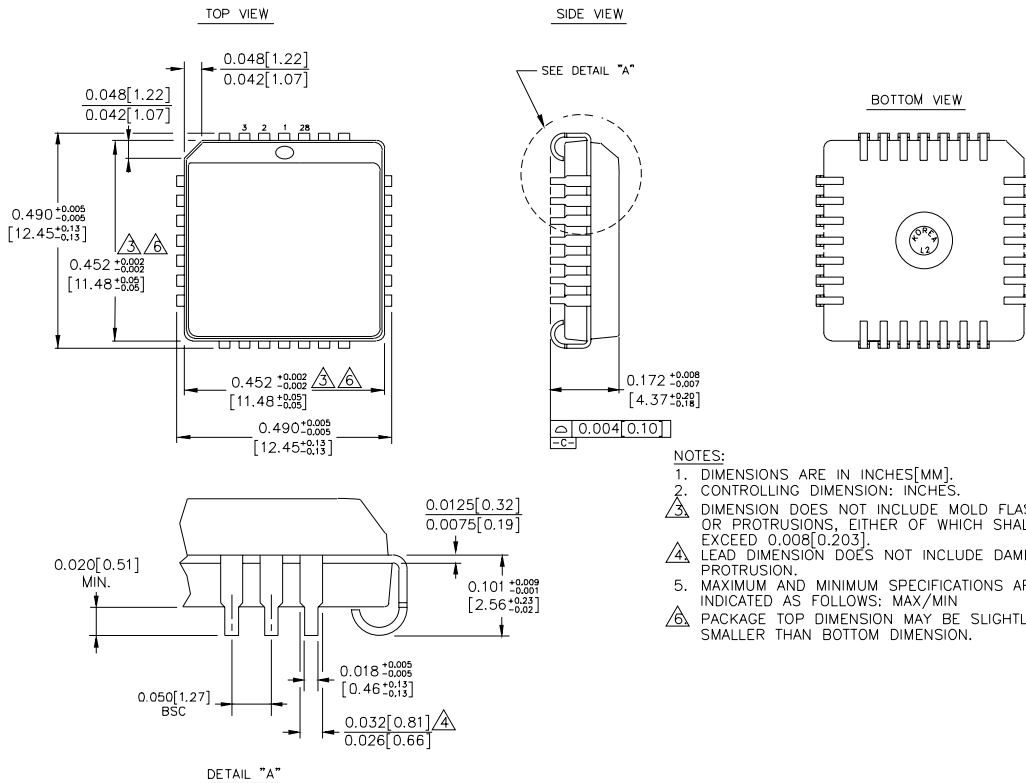
Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
		10E	120	145	120	145	120	145				
		100E	120	145	120	145	138	165				

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{MAX}	Max. Toggle Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t _{PD}	Propagation Delay to Output CLK MR	600	800	1000	600	800	1000	600	800	1000	ps	—
		600	800	1000	600	800	1000	600	800	1000		
t _S	Set-up Time D SEL	50	-100	—	50	-100	—	50	-100	—	ps	—
		300	150	—	300	150	—	300	150	—		
t _H	Hold Time D SEL	300	100	—	300	100	—	300	100	—	ps	—
		75	-150	—	75	-150	—	75	-150	—		
t _{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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