DESCRIPTION

Demonstration circuit 481 is a monolithic step-down DC/DC switching converter featuring the LT1976. The board is optimized for 3.3V output at up to 1A load current for an input voltage range of 4V to 60V. *Minimum on-time restrictions and 3.3V output may limit the steady state maximum input voltage to 42V (up to 47V for some boards) before pulse skipping occurs*. With its wide input voltage range, 1.5A internal power switch, 100µA supply current (at input voltages above 14V), 200kHz switching frequency and thermally enhanced package, the LT1976 is a very versatile and powerful IC for DC/DC converters that require compact space, high efficiency at both heavy and light loads and high input voltage.

The LT1976 200kHz switching frequency allows all of the components to be small, surface mount devices. Synchronization with an external clock of up to 700kHz is possible. The current-mode control topology creates fast transient response and good loop stability with a minimum number of external components. The low resistance internal power switch (0.2Ω) achieves high efficiencies of up to 90%. The $\overline{SHDN}$ pin can be used to program undervoltage lockout or place the part in micropower shutdown, reducing supply current to less than 1µA by driving the pin low. Burst Mode™ reduces zero load current to under 100µA at most input voltages (see Figure 3) while maintaining a regulated output. A power good comparator and a timing delay can be used for additional system diagnostics and sequencing. The soft start function reduces inrush current at soft start and output voltage overshoot.

The LT1976 datasheet gives a complete description of the part, operation and applications information. The datasheet must be read in conjunction with this Quick Start Guide for demonstration circuit 481. In particular, the datasheet section on 'Thermal Calculations' is important for estimating whether a given application's combination of input voltage, load current and frequency will cause the LT1976 to exceed it's absolute maximum rated junction temperature. The LT1976 is assembled in a small 16-pin thermally enhanced package with exposed pad where proper board layout is essential for maximum thermal performance. See the datasheet section 'Layout Considerations'.

Design files for this circuit board are available. Call the LTC factory.

Burst Mode is a trademark of Linear Technology Corporation.

Table 1. Typical Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Steady State Input Voltage Range	V_{OUT} = 3.3V, $I_{OUT} \leq$ 1A	4–42V
Maximum Transient Input Voltage		60V
V_{OUT}	V_{IN} = 4V to 60V, $I_{OUT} \leq$ 1A	3.3V ± 3%
Maximum Output Current	V_{OUT} = 3.3V	1A
Output Voltage Ripple	V_{IN} = 12V, I_{OUT} = 1A, V_{OUT} = 3.3V	$34mV_{PK-PK}$
	V_{IN} = 42V, I_{OUT} = 1A, V_{OUT} = 3.3V	$42mV_{PK-PK}$
Switching Frequency	V_{IN} = 4V to 42V, $I_{OUT} \leq$ 1A	200kHz
Efficiency	V_{IN} = 12V, I_{OUT} = 1A, V_{OUT} = 3.3V	80%
	V_{IN} = 42V, I_{OUT} = 1A, V_{OUT} = 3.3V	72%

QUICK START PROCEDURE

Demonstration circuit 481 is easy to set up to evaluate the performance of the LT1976. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: Make sure that the input voltage does not exceed 60V.

NOTE: The synchronization, shutdown, and power good functions are optional and their terminals can be left floating (disconnected) if their functions are not being used.

NOTE: Do not hot-plug the input voltage terminal VIN. The absolute maximum voltage on VIN is 60V and hot-plugging a power supply through wire leads to the demonstration circuit can cause the voltage on the extremely low-ESR ceramic input capacitor to ring to twice its DC value. This is due to high currents instantaneously generated in the inductive supply leads from an input voltage step on the low-ESR ceramic input capacitor. A bulky higher-ESR capacitor, and an additional inductive filter can be added to the circuit to dampen hot-plug transient ringing. *See Application Note 88 for more details.* In order to protect the IC, a transient voltage suppressor diode can be added between VIN and GND terminals to absorb any high voltage transient ringing that may occur due to hot-plugging.

NOTE: Connect the power supply (with power off), load, and meters as shown in Figure 1.

1. After all connections are made, turn on input power and verify that the output voltage is 3.3V.

   NOTE: If the output voltage is too low, temporarily disconnect the load to make sure that the load is not set too high.

2. Once the proper output voltages are established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

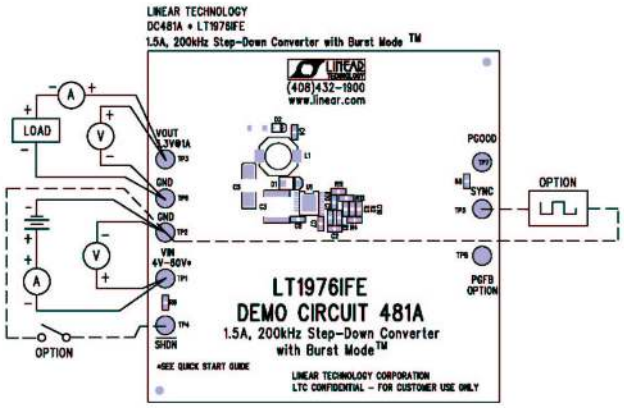


Figure 1. Proper Measurement Equipment Setup

FUNCTIONS & OPTIONS

BURST MODE

Burst Mode operation reduces light load quiescent current by disabling switching for a number of switch cycles and reducing supply current briefly until switching begins again. Bursts of switch pulses are enough to maintain output voltage regulation at light load. Figure 3 shows the supply current versus input voltage. At input voltages above 12V, zero load supply current is less than 110µA.

Burst Mode extends battery life in applications with long periods of inactivity. The tradeoff of having Burst Mode is creating increased output voltage ripple at light load. For loads that require extremely well-regulated output voltages, additional filtering may be used on the output to achieve extremely low output voltage ripple. At higher input voltages (above $35V_{IN}$), Burst Mode may occur below load currents as high as 300mA to 500mA.

OUTPUT VOLTAGE

The components assembled on the board are optimized for a wide input voltage range and a 3.3V

output. The feedback resistors (R2, R3) can be changed to adjust the output voltage according to the following equation:

$V_{OUT} = 1.24 \times (1 + R2/R3)$

For output voltages below 3V, the boost pin requires a higher voltage than the output can supply. An alternate source for boost such as the input voltage, a bias supply, or an external supply is required on the boost pin. Please see the datasheet for details.

For output voltages greater than 5V, the optional 'blocking' zener diode D3 can be used to reduce the boost voltage across C4 to some lower voltage between 3V and 5V. The diode transfers power dissipation from inside the LT1976 to the diode on the demonstration circuit, outside the LT1976, allowing higher ambient temperature operation of the part. Maintaining boost voltage between 3V and 5V maximizes efficiency and optimizes control of the power switch. It is recommended that a CMHZ5236B zener diode is used in D3 when V_{OUT} = 12V. To properly install D3, the small trace shorting the anode to the cathode of D3 on the board must be opened (an Exacto knife works well) before D3 is soldered to the board. In the 'Thermal Calculations' section of the datasheet, the new value for boost voltage (V_{OUT}–V_Z) should be accounted for when calculating junction temperature.

$P_{BOOST} = (V_{OUT}\text{-}V_Z)*V_{OUT}*(I_{OUT}/36)/V_{IN}$

POWER GOOD FEEDBACK OPTION

For systems that rely upon having a well-regulated power source or follow a particular power-up sequence, the LT1976 provides a power good flag with timed delay programmed by C8 when the power good feedback pin (PGFB) exceeds 90% of V_{REF} (1.25V). R10 (0 ohm short) ties PGFB and the feedback pin (FB) together. Therefore, the power good (PG) pin returns a 'good' signal when the output voltage has reached 90% of its final value. Figure 11 and Figure 12 show the power good logic output turning on after a programmed delay during startup.

The power good feedback pin can also be tied to the input voltage, an external source, or a resistor divider on any of these sources. Removing R10 breaks the connection between PGFB and FB.

The Power Good Feedback (PGFB Option) terminal is optional and is not stuffed on the board. The power good terminal node can be connected to the power good feedback (PGFB) pin by placing a 0Ω resistor in R11. The PGFB Option should be used when Power Good Feedback is required from a source other than the feedback pin. Be sure to remove the connection between PGFB and FB by removing R10 as mentioned above. Connect the desired Power Good Feedback source to the PGFB Option terminal and either short the terminal to PGFB pin with a 0Ω resistor in R11 or place a resistor divider from PGFB to GND with R11 and R12.

SHUTDOWN AND UNDERVOLTAGE LOCKOUT

The $\overline{SHDN}$ pin has a 200k pull-up resistor (R9) tied to V_{IN}. For normal operation, the $\overline{SHDN}$ terminal can be left floating. However, connecting the $\overline{SHDN}$ terminal to GND will place the IC in micropower shutdown. If the shutdown function is not being used, the pull-up resistor can be replaced with a 0Ω resistor.

For undervoltage lockout, the two-resistor divider network must be placed between V_{IN} and $\overline{SHDN}$ and between $\overline{SHDN}$ and GND. The top resistor can be placed in R9. The bottom resistor can be placed to the right of the SHDN terminal (the solder mask may have to be removed.

Please see the data sheet section '*Shutdown Function and Undervoltage Lockout*' for more details.

SOFT START

Soft start removes the inrush current surge and limits output voltage overshoot by controlling the output voltage ramp-up rate. A single capacitor, C7, holds the peak current level clamp low, allowing it to slowly rise upon startup. When a short circuit, overload, or shutdown condition occurs, the

soft start capacitor resets to zero and provides soft start during restart. Switchers that do not have soft start may transition from zero output to full output voltage by taking as much current as possible from the source and casting it into the output capacitor and load. This surge of current, only restricted by maximum peak switch current levels, can both drag down a battery source voltage and cause overshoot in the output voltage.

For the shortest possible startup time, remove the soft start capacitor from the circuit. Maximum inrush current can reach the level of 3A (the maximum switch current limit). Expect to see a significant increase in output voltage overshoot.

Figure 11 and Figure 12 show the soft startup of DC481 and the limited inrush current during startup.

SYNCHRONIZATION

The synchronization frequency range for the LT1976 is 235kHz to 700kHz. Use a logic level sync signal with a duty cycle between 10% and 90% connected directly to the SYNC pin. Keep in mind that synchronization at high frequencies may reduce the effect of slope compensation. High sync frequencies combined with high duty cycles (above 50%) may result in unexpected loop instability.

COMPENSATION

Demonstration Circuit 481 has a frequency compensation network that is optimized for the tantalum output capacitor C5, the wide input voltage range 4V to 60V (42V steady state), and 3.3V output. Improved loop bandwidth can be achieved for various output voltages, output capacitors, and input voltage ranges by adjusting R1, C2, and C1. A feedforward capacitor (C10) and a resistor (R4 for short circuit feedback pin protection when C10 is used) are located in parallel with R2. Removing these components from the feedback loop may result in compromised loop stability. The use of alternate output capacitors such as ceramics or PosCaps may require changes to the compensation components. For more information, see the 'Frequency Compensation' section in the Applications Information in the datasheet, Application Note 19, or Application Note 76.

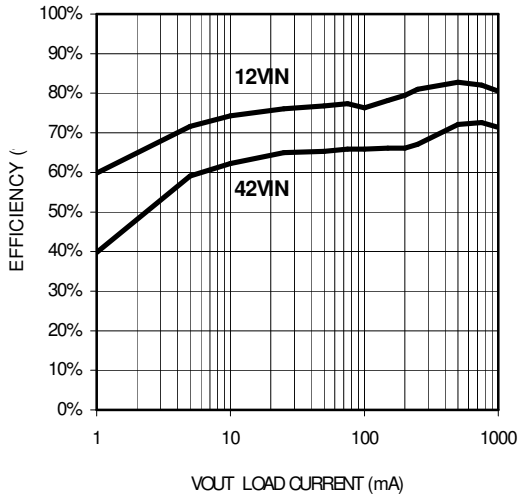


Figure 2. DC481 Typical Efficiency (T_A = 25°C, V_{OUT} = 3.3V)

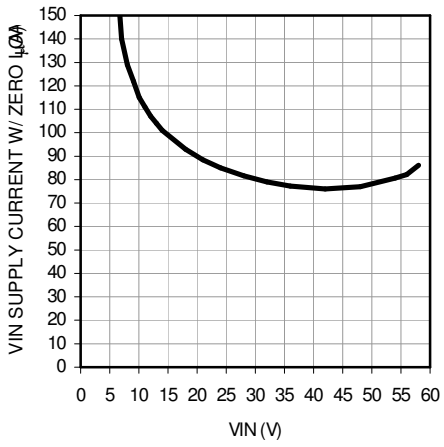


Figure 3. DC481 Typical Supply Current (I_{OUT} = 0A, T_A = 25°C, V_{OUT} = 3.3V)

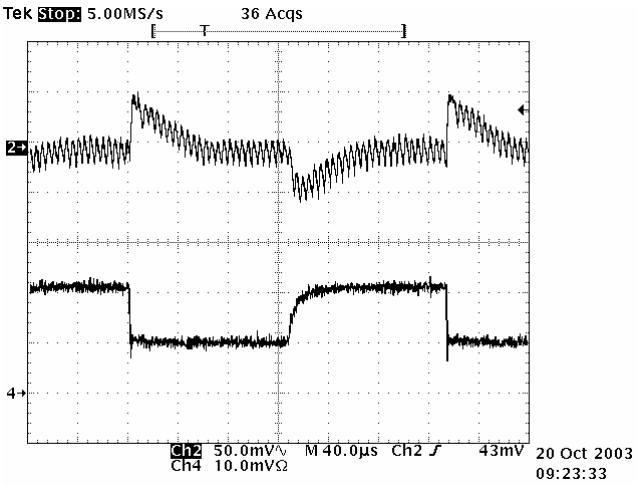


Figure 4. DC481 Typical Step Load Response (I_{OUT} = 500mA to 1A, V_{IN} = 12V, T_A = 25°C, V_{OUT} = 3.3V) CH2 is V_{OUT} (AC) CH4 is I_{OUT} (500mA/10mVΩ)

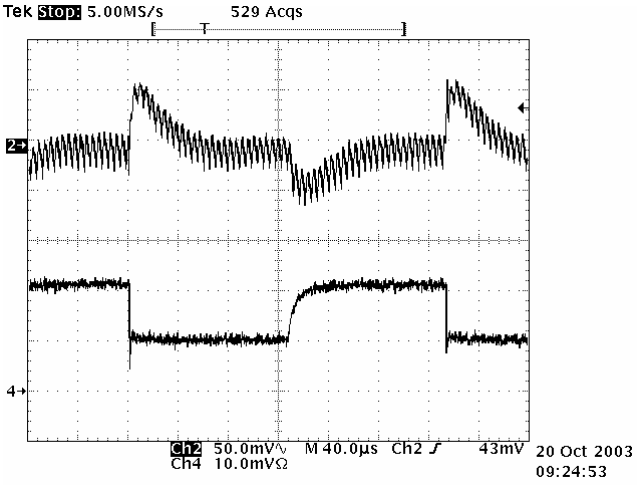


Figure 5. DC481 Typical Step Load Response (I_{OUT} = 500mA to 1A, V_{IN} = 42V, T_A = 25°C, V_{OUT} = 3.3V) CH2 is V_{OUT} (AC) CH4 is I_{OUT} (500mA/10mVΩ)

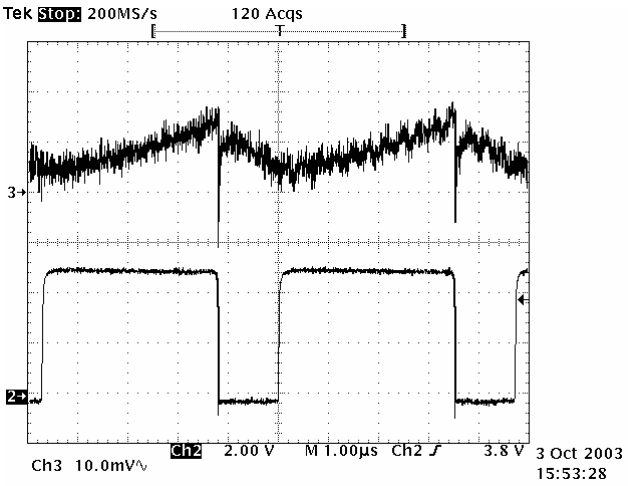


Figure 6. DC481 Typical Output Voltage Ripple (I_{OUT} = 500mA, V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25°C) CH3 is V_{OUT} ripple (AC), CH2 is V_{SW}

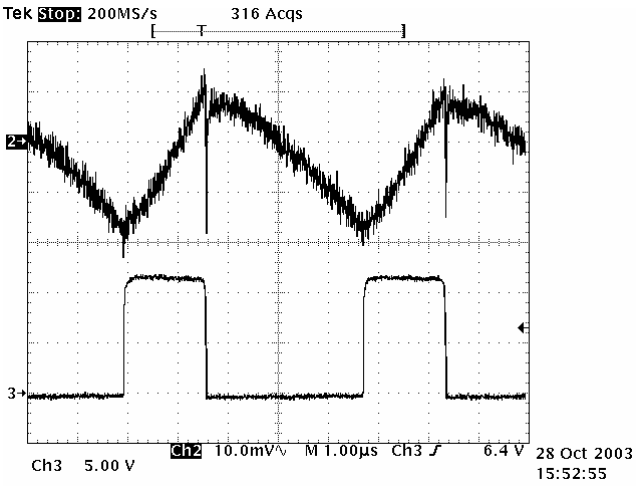


Figure 7. DC481 Typical Output Voltage Ripple (I_{OUT} = 1A, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C) CH2 is V_{OUT} ripple (AC), CH3 is V_{SW}

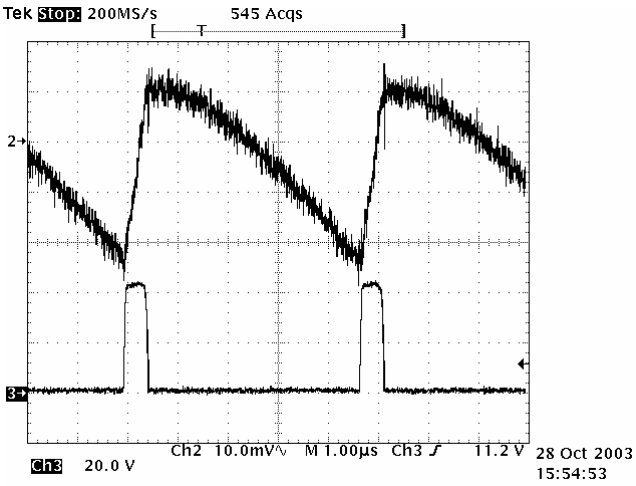


Figure 8. DC481 Typical Output Voltage Ripple (I_{OUT} = 1A, V_{IN} = 42V, V_{OUT} = 3.3V, T_A = 25°C) CH2 is V_{OUT} ripple (AC), CH3 is V_{SW}

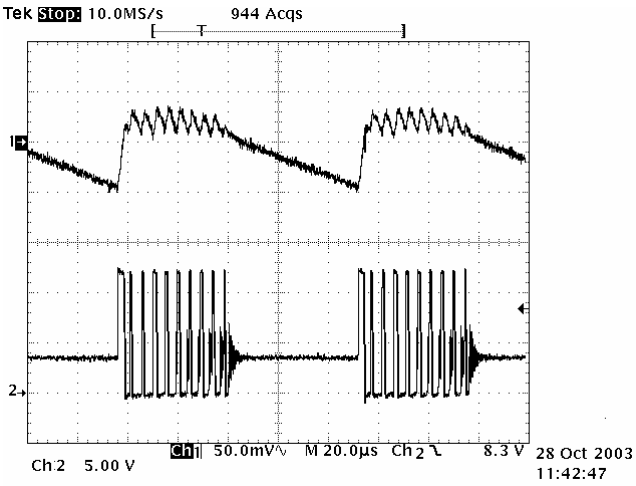


Figure 9. DC481 Typical Output Voltage Ripple in Burst Mode (I_{OUT} = 100mA, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C) CH1 is V_{OUT} ripple (AC), CH2 is V_{SW}

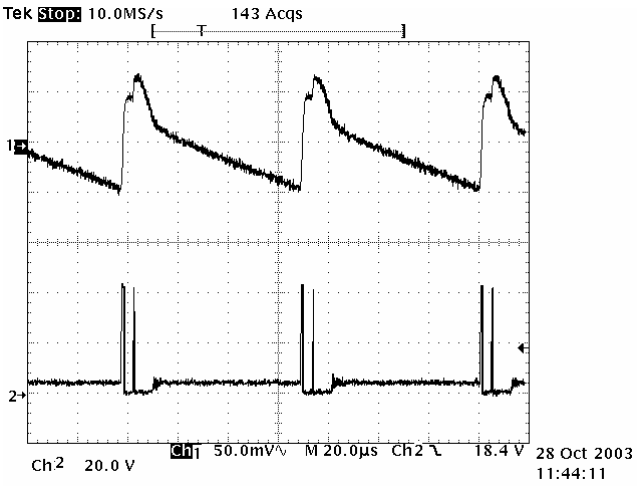


Figure 10. DC481 Typical Output Voltage Ripple in Burst Mode (I_{OUT} = 100mA, V_{IN} = 42V, V_{OUT} = 3.3V, T_A = 25°C) CH1 is V_{OUT} ripple (AC), CH2 is V_{SW}

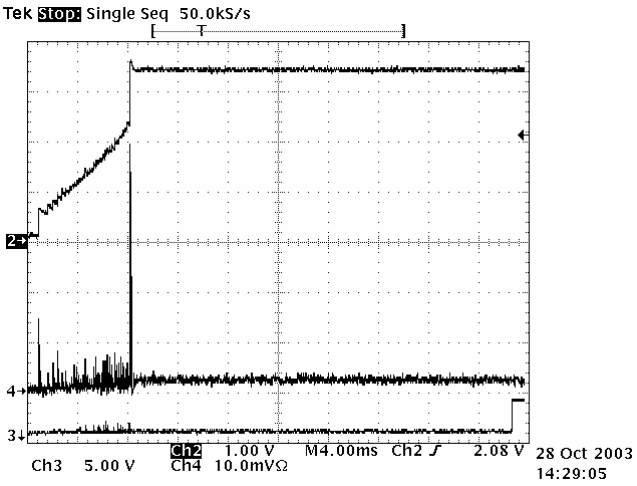


Figure 11. DC481 Soft Startup (R_{LOAD} = 3.3Ω, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C) CH2 is V_{OUT}, CH3 is Power Good, CH4 is I_{IN} (200mA/10.0mVΩ)

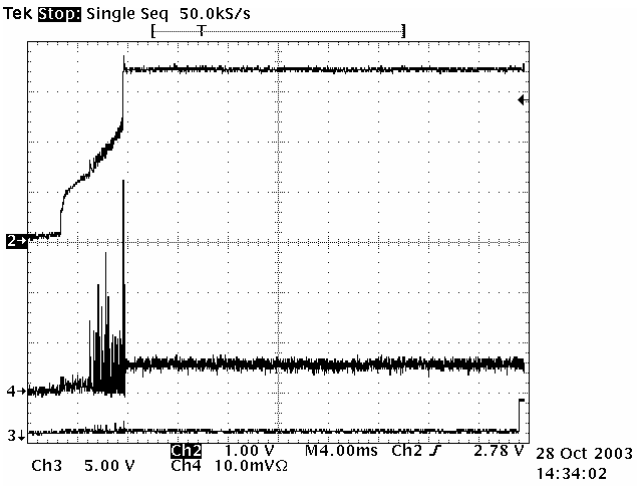


Figure 12. DC481 Soft Startup (R_{LOAD} = 7Ω, V_{IN} = 42V, V_{OUT} = 3.3V, T_A = 25°C) CH2 is V_{OUT}, CH3 is Power Good, CH4 is I_{IN} (100mA/10.0mVΩ)

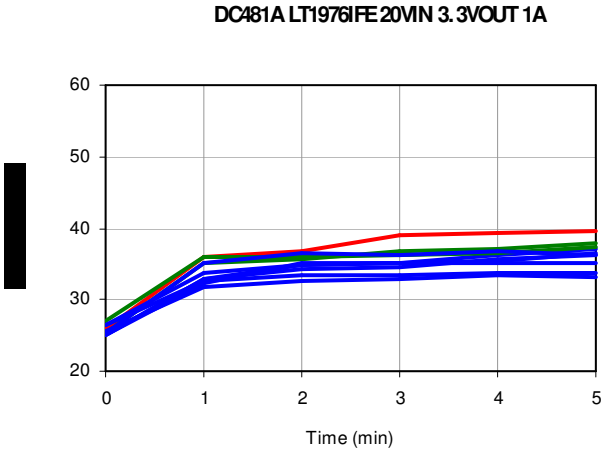


Figure 13. Five Minute Thermal Profile of DC481×10 (I_{OUT} = 1A, V_{IN} = 20V, T_A = 25°C, V_{OUT} = 3.3V)

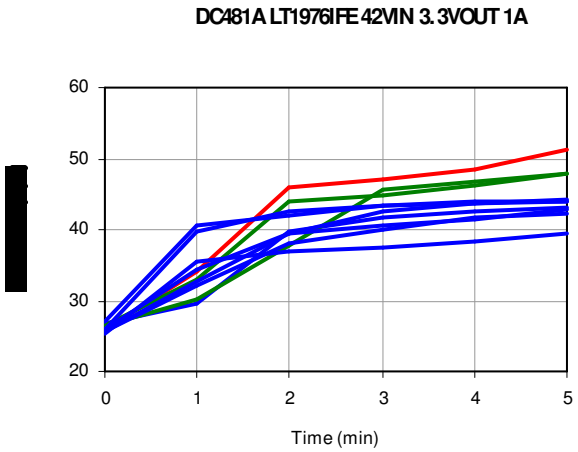


Figure 14. Five Minute Thermal Profile of DC481×10 (I_{OUT} = 1A, V_{IN} = 42V, T_A = 25°C, V_{OUT} = 3.3V)

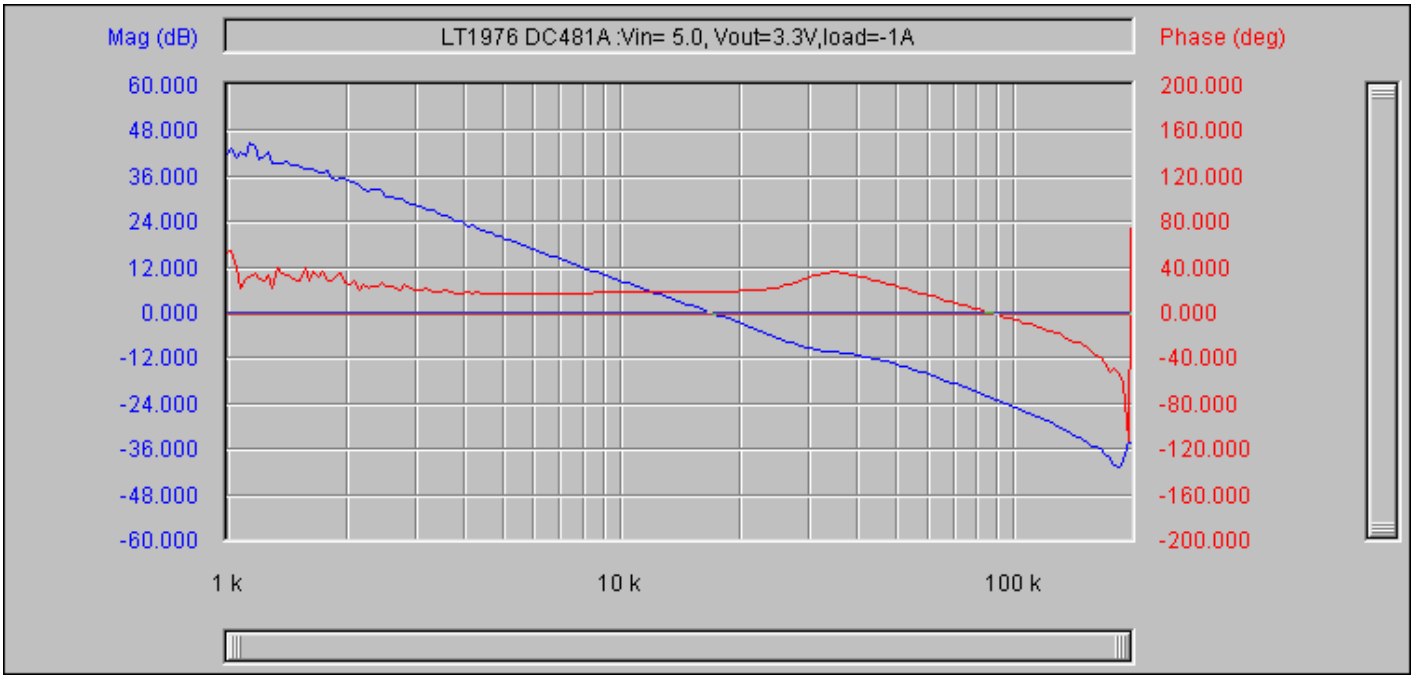


Figure 15. Bode Plot (Phase and Gain I_{OUT} = 1A, V_{IN} = 5V, T_A = 25°C, V_{OUT} = 3.3V)

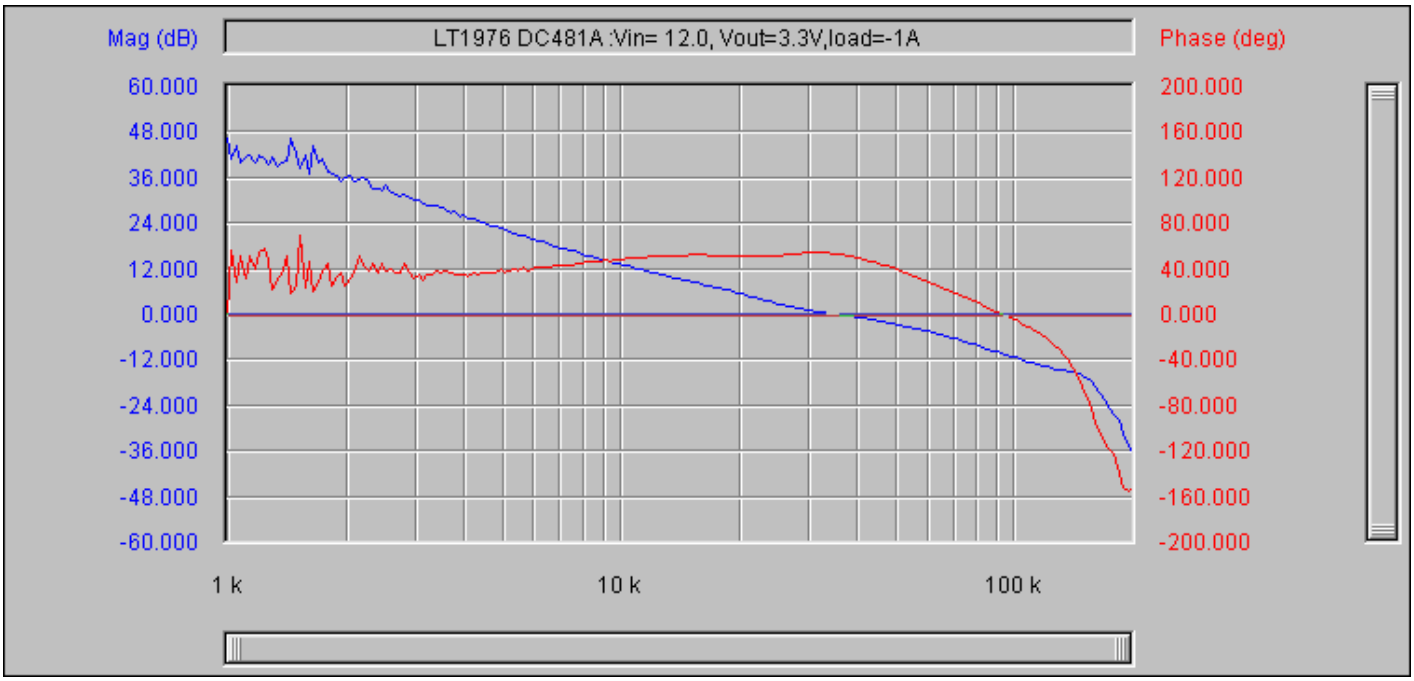


Figure 16. Bode Plot (Phase and Gain I_{OUT} = 1A, V_{IN} = 12V, T_A = 25°C, V_{OUT} = 3.3V)

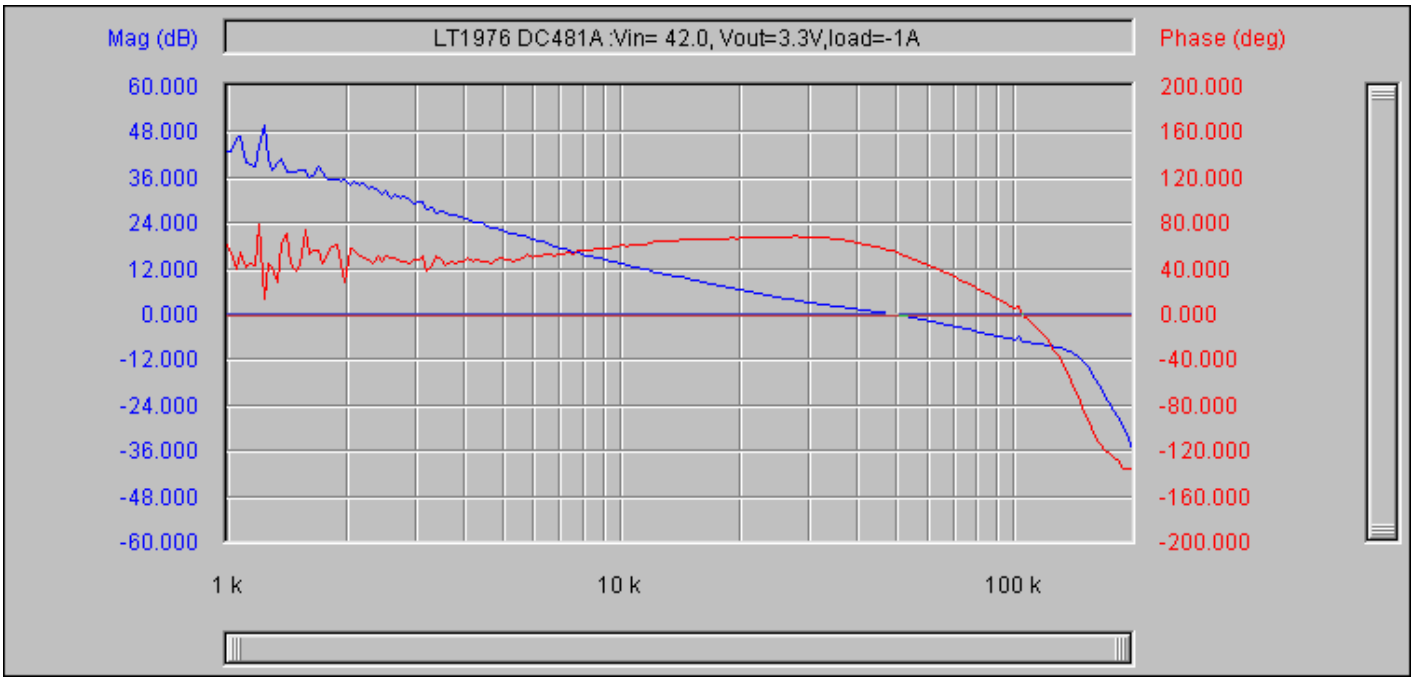
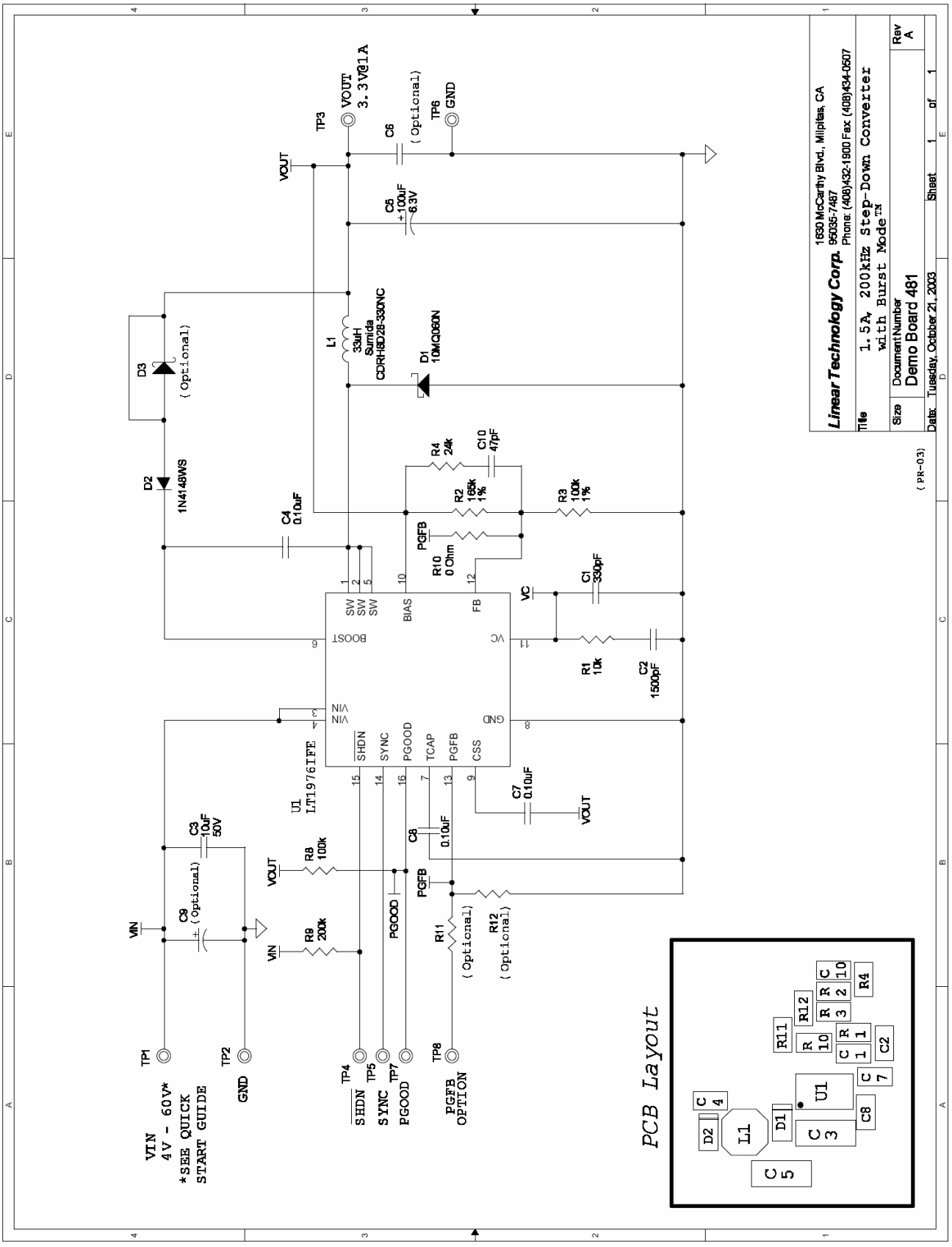
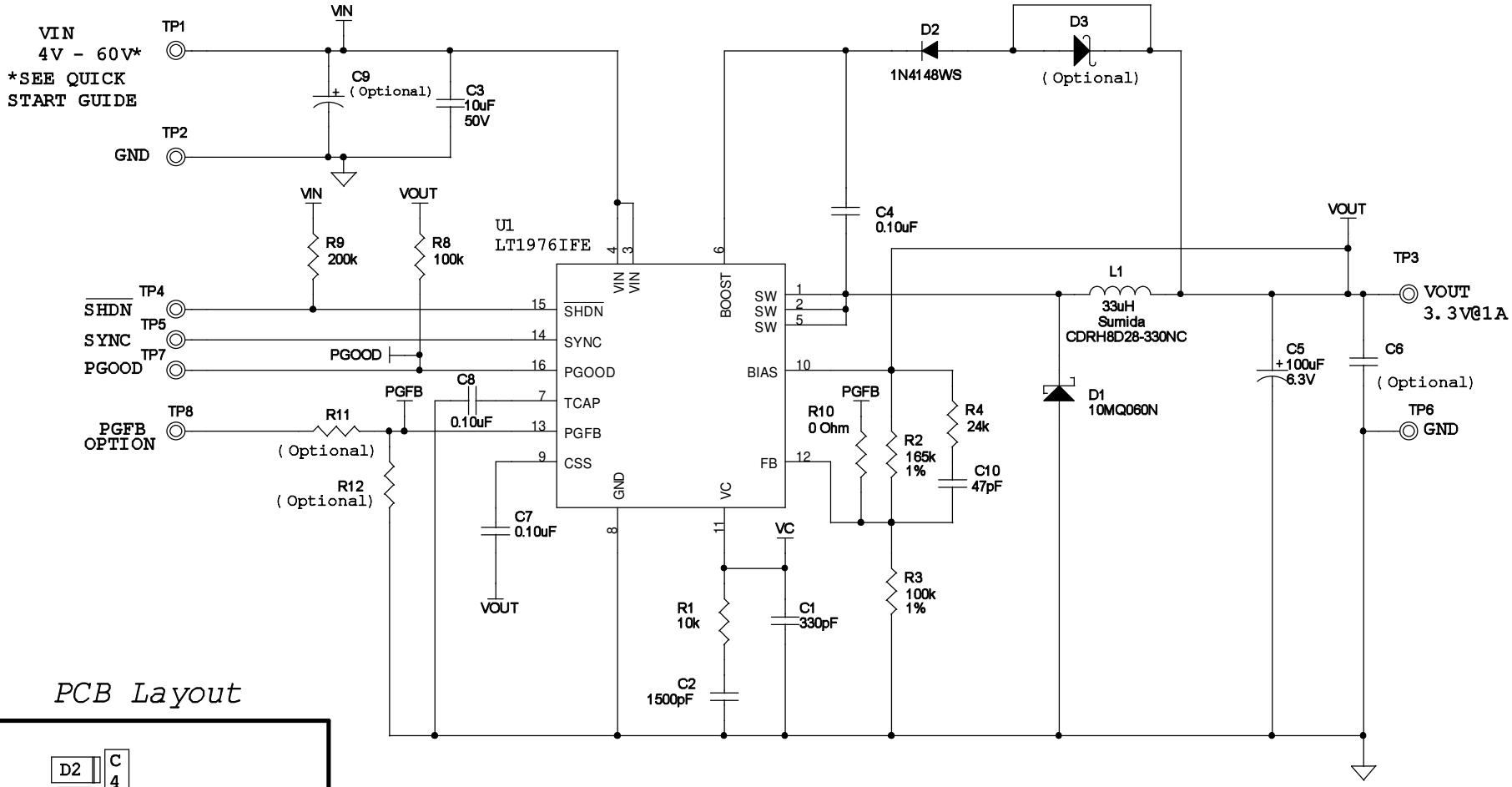
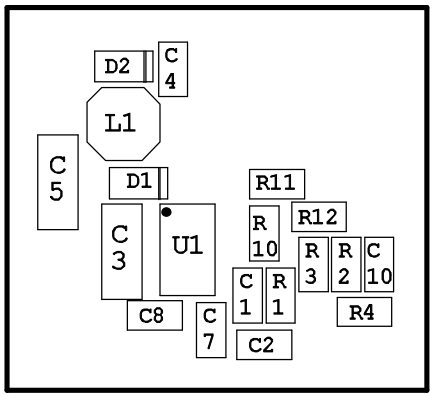


Figure 17. Bode Plot (Phase and Gain I_{OUT} = 1A, V_{IN} = 42V, T_A = 25°C, V_{OUT} = 3.3V)


VIN
4V - 60V*
*SEE QUICK START GUIDE
GND
SHDN
SYNC
PGOOD
PGFB OPTION
VOUT 3.3V@1A
(Optional)
U1 LT1976IFE
SW
BIAS
FB
VC
BOOST
VIN
SHDN
SYNC
PGOOD
TCAP
PGFB
CSS
GND
L1 33uH Sumida CDRH6D28-330NC
D1 10MQ060N
D2 1N4148WS
D3 (Optional)
C1 330pF
C2 1500pF
C3 10uF 50V
C4 0.10uF
C5 100uF 6.3V
C6 (Optional)
C7 0.10uF
C8 0.10uF
C9 (Optional)
R1 10k
R2 165k 1%
R3 100k 1%
R4 24k
C10 47pF
R8 100k
R9 200k
R10 0 Ohm
R11 (Optional)
R12 (Optional)
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8
Linear Technology Corp.
1630 McCarthy Blvd., Milpitas, CA 95035-7487
Phone: (408)432-1900 Fax: (408)434-0507
Title: 1.5A, 200kHz Step-Down Converter with Burst Mode™
Size: Document Number Demo Board 481
Rev A
Date: Tuesday, October 21, 2003
Sheet 1 of 1
(PR-03)
PCB Layout



PCB Layout



(PR-03)

Linear Technology Corp.
1630 McCarthy Blvd., Milpitas, CA
95035-7487
Phone: (408)432-1900 Fax: (408)434-0507

Title	1.5A, 200kHz Step-Down Converter with Burst Mode™	
Size	Document Number: Demo Board 481	Rev A
Date: Tuesday, December 02, 2003	Sheet 1 of 1	

Linear Technology Corporation

LT1976IFE

Bill Of Material

Item	*Qty*	*Reference*	*Part Description*	*Manufacture / Part #*
1	1	C1	Cap., NPO 330pF 50V 10%	AVX 06035A331KAT1A
2	1	C2	Cap., X7R 1500pF 25V 10%	AVX 06033C152KAT1A
3	1	C3	Cap., X7R 10uF 50V 20%	TDK C5750X7R1H106M
4	3	C4,C7,C8	Cap., X7R 0.10uF 16V 20%	Taiyo Yuden EMK107BJ104M
5	1	C5	Cap., Tant. 100uF 6.3V 20%	AVX TPSC107M006R075
6	0	C6 (Optional)	OPT.	
7	0	C9 (Optional)	OPT.	
8	1	C10	Cap., NPO 47pF 50V 10%	AVX 06035A470KAT1A
9	1	D1	Schottky Rect., 2.1Amp\60V	IR 10MQ060N
10	1	D2	Diode, 75V/200mW	Diodes Inc. 1N4148WS
11	0	D3 (Optional)	OPT.	
12	1	L1	Inductor, 33uH	Sumida CDRH8D28-330NC
13	1	R1	Res., Chip 10k 0.1W 5%	AAC CR16-103JM
14	1	R2	Res., Chip 165k 0.1W 1%	AAC CR16-1653FM
15	1	R3	Res., Chip 100k 0.1W 1%	AAC CR16-1003FM
16	1	R4	Res., Chip 24k 0.1W 5%	AAC CR16-243JM
17	1	R8	Res., Chip 100k 0.1W 5%	AAC CR16-104JM
18	1	R9	Res., Chip 200k 0.06W 5%	AAC CR16-204JM
19	1	R10	Jumper, Chip 0 Ohm 1/16W 1AMP	AAC CJ06-000M
20	0	R11,R12 (Optional)	OPT.	
21	7	TP1-TP7	Turret, Testpoint	Mill Max 2501-2
22	0	TP8 (Optional)	OPT.	
23	1	U1	I.C., Step-Down Reg.	Linear Tech. Corp. LT1976IFE
24	1		PRINTED CIRCUIT BOARD	DEMO CIRCUIT #481A
25	1		STENCIL	STENCIL 481A