WMS7140/1

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NONVOLATILE DIGITAL POTENTIOMETERS

WITH UP/DOWN (3-WIRE) INTERFACE,

10KOHM, 50KOHM, 100KOHM RESISTANCE

16 TAPS

WITH OPTIONAL OUTPUT BUFFER



1. GENERAL DESCRIPTION

The WMS714x is a 16 non-volatile linear digital potentiometers available in $10K\Omega$, $50K\Omega$ and $100K\Omega$ resistance values. The WMS7140/1 can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications.

The output of each potentiometer is determined by the wiper position, which varies in linearly between V_A and V_B terminal according to the content stored in the volatile Tap Register (TR) which is programmed through Up/Down (Increment/Decrement) interface. The channel has one non-volatile memory location (NVMEM0) that can be directly written to by users through the Up/Down interface. Power-on recall is also built in so the content of the NVMEM0 to Tap Register is automatically loaded.

The WMS7140/1 devices pin out the resistor wiper directly. The WMS7141 devices feature an output buffer with 3mA minimum drive capability.

All the WMS7140/1 devices are single channel devices offered in 8-pin PDIP, SOIC and MSOP packages. The WMS7140/1 devices operate over a wide operating voltage ranging from 2.7V to 5.5V.

2. FEATURES

- · Drop-in replacements for many popular parts
- Available output buffer for WMS7141 devices
- Single linear-taper channel
- 16 taps
- 10K, 50K and 100K end-to end resistance
- V_{SS} to V_{DD} terminal voltages
- Non-volatile storage of wiper positions with power-on recall
- Data storage and potentiometer control through Up/Down (3-wire) interface
- Endurance 100,000 write cycles
- Data retention 100 years
- Package options:
 - o 8-pin PDIP, SOIC or MSOP
- Industrial temperature range: -40° ~ 85°C
- Single supply operation 2.7V to 5.5V



3. BLOCK DIAGRAM

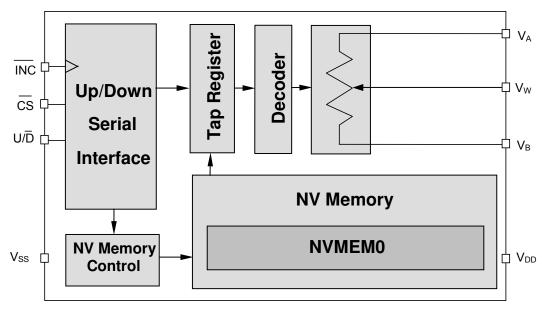


FIGURE 1 – WMS7140 BLOCK DIAGRAM (Rheostat Mode)

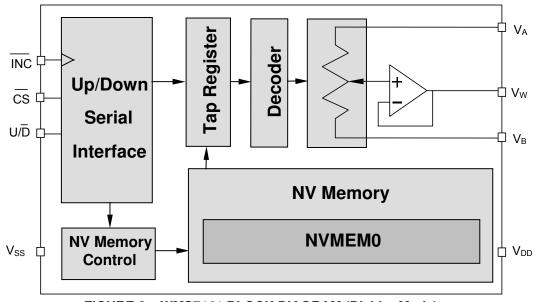


FIGURE 2 – WMS7141 BLOCK DIAGRAM (Divider Mode)

WMS7140/1

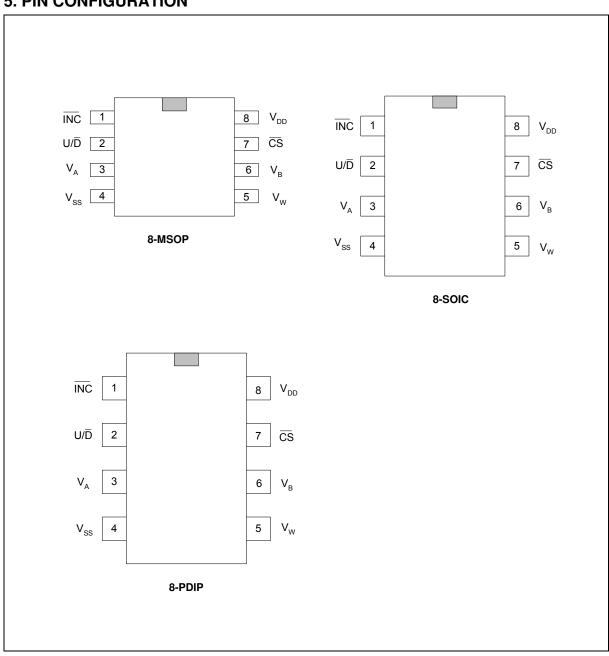


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5. PIN CONFIGURATION





6. PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Pin Name	I/O	Description
INC	I	Increment Control. A High-Low transition of $\overline{\text{INC}}$ when $\overline{\text{CS}}$ is low will move the wiper up or down for one increment based on the $\overline{\text{U/D}}$ input
U/D	I	Up/Down control Input. High state will cause the wiper to move to the V_{B} terminal, Low state to the V_{A} terminal
V _A	-	High terminal of WinPot
V _{SS}	i	Ground pin, logic ground reference
V_{DD}	ı	Power Supply
CS	Ι	Chip Select. When \overline{CS} is HIGH, the part is deselected and the device will be in the standby mode. \overline{CS} LOW enables the part, placing it in the active power mode
V_B	-	Low terminal of WinPot
V _W	0	Wiper terminal of WinPot (can be buffered), its position on the resistor array is controlled by the inputs on \overline{INC} , U/\overline{D} , and \overline{CS}



7. FUNCTIONAL DESCRIPTION

The WMS7140/1, a nonvolatile digitally programmable potentiometers with 16 taps, with or without output buffer, is designed to operate as both a potentiometer or a variable resistor depending upon the output configuration selected.

The chip can store up to one 8-bit word in a nonvolatile memory (NVMEM0) in order to set the tap register value when the device is powered up.

The WMS7140/1 is controlled by a serial Up-Down (3-wire) interface that allows setting the tap register value as well as storing data in the nonvolatile memory.

7.1. POTENTIOMETER AND RHEOSTAT MODES

The WMS7140/1 can operate as either a rheostat or as a potentiometer (voltage divider). When in the potentiometer configuration there are two possible modes. One is done using WMS7140 Winpot device without the output buffer and the other mode is done with WMS7141 WinPot device with the output buffer.

7.1.1. Rheostat Configuration

The WMS7140/1 acts as a two terminal resistive element in the rheostat configuration where one terminal can be connected to either the end point pins of the resistor (V_A and V_B) and the other terminal is the wiper (V_W) pin. This configuration controls the resistance between the two terminals and the resistance can be adjusted by sending the corresponding tap register setting to the WMS7140/1 or can also be set by loading a pre-set tap register value from nonvolatile memory NVMEM0 upon power up.

7.1.2. Potentiometer Configuration

In potentiometer configuration an input voltage is applied to either one of the end point pins (V_A or V_B). The voltage on the wiper pin will be proportional to the voltage difference between V_A and V_B and the wiper setting. The resistance cannot be directly measured in this configuration.

7.2. Non-Volatile Memory (NVMEM)

The WMS7140/1 has one NVMEM position available for storing the potentiometer setting. The NVMEM position can be directly written via the Up/Down interface. The potentiometer is loaded with the value stored in the NVMEM0 on power up.



7.3. SERIAL DATA INTERFACE

The Up/Down family has a 3-wire Serial Data Interface consisting of CS, INC, U/D pins. Only UP/DOWN operations can be performed. The key features of this interface include:

- Increment/Decrement operations on the tap register (TR)
- Direct refresh of tap register (TR) from internal NVMEM
- Nonvolatile storage of the present tap register value into the NVMEM and automatic recall at power up
- For WMS7141 devices, output buffer amplifier

7.4. OPERATION OVERVIEW

The wiper position or the Tap Register(TR) setting can only be changed by the UP/DOWN operation with the combination of \overline{CS} , U/ \overline{D} , and \overline{INC} signals. When \overline{CS} is low, the part will be activated and the TR setting can be changed by toggling \overline{INC} , and TR will move up when U/ \overline{D} is High and move down when U/ \overline{D} is Low. The TR setting will be stored into the user NVMEM automatically each time \overline{CS} goes high while \overline{INC} holds high. Otherwise, if \overline{INC} is low when \overline{CS} goes high, the TR setting will not be stored. The NVMEM content will be automatically loaded into TR at Power On. The user NVMEM can be tested through the voltage measurement on the wiper pin after saving TR setting into the NVMEM and reloading into the TR. When the TR setting is already at LOW, further DOWN operations won't change the setting. Similarly, when TR setting is at HIGH, further UP operations won't change the setting.

When CS is held HIGH, the part will be in Standby mode and the TR setting will not be changed. The operating modes of Up/Down are summarized below.

CS	U/D	INC	Operation
Low	High	High to Low	Wiper toward V _A
Low	Low	High to Low	Wiper toward V _B
Low to High	Х	High	Store Wiper Position
Low to High	Х	Low	No Store, Return to Standby
High	х	х	Standby

Note: x means don't care



8. TIMING DIAGRAMS

Conditions: V_{DD} = +2.7V to 5.5V, V_A = V_{DD} , V_B = 0V, T = 25°C

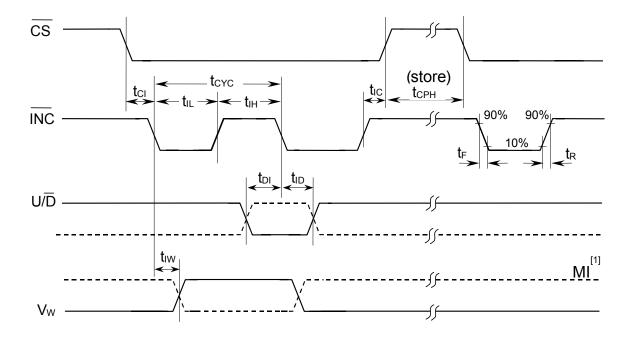


FIGURE 3 -WMS7140/1 TIMING DIAGRAM

Note:

[1] MI in the AC Timing diagram (Figure 3) refers to the minimum incremental change in the wiper output due to a change in the wiper position.



TABLE 10 – TIMING PARAMETERS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
CS to INC Setup	t _{CI}	100		ns
U/D to INC Setup	t _{DI}	50		ns
U/D to INC Hold	t _{ID}	100		ns
INC LOW Period	t _{IL}	250		ns
INC HIGH Period	t _{IH}	250		ns
INC Inactive to CS Inactive	t _{IC}	1		μS
CS Deselect Time (NO STORE)	t _{CPH}	100		ns
CS Deselect Time (STORE)	t _{CPH}	15 (2.7V)		ms
INC to V _W Change	t _{IW}		5	μS
INC Cycle Time	t _{CYC}	1		μS
INC Input Rise and Fall Time	t _R , t _F		500	μS
Power-Up to Wiper Stable	t _{PU}		1	ms
		0.2	50	V/ms
V _{CC} Power-Up rate	$t_R V_{CC}$	(13ms	(54μs	
		0-2.7V)	0-2.7V)	



9. ABSOLUTE MAXIMUM RATINGS

TABLE 11 – ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)[1]

Conditions	Values
Junction temperature	150°C
Storage temperature	-65° to +150°C
Voltage applied to any pad	$(V_{ss} - 0.3V)$ to $(V_{DD} + 0.3V)$
$V_{DD} - V_{SS}$	-0.3 to 7.0V

TABLE 12 - OPERATING CONDITIONS (PACKAGED PARTS)

Conditions	Values
Commercial operating temperature range	0°C to +70°C
Extended operating temperature	-20°C to +70°C
Industrial operating temperature	-40°C to +85°C
Supply voltage (V _{DD})	+2.7V to +5.5V
Ground voltage (V _{SS})	OV

^[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions



10. ELECTRICAL CHARACTERISTICS

TABLE 12 – ELECTRICAL CHARACTERISTICS (Packaged parts)

DADAMETERS	CVMDOL	BAINI	TVD	MAY	LINITO	CONDITIONES
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS
Rheostat Mode		T	T		T	
Nominal Resistance	R	-20		+20	%	T=25°C, V _W open
Different Non Linearity [2]	DNL	-1		+1	LSB	
Integral Non Linearity [2]	INL	-1		+1	LSB	
Tempo ¹	$\Delta R_{AB}/\Delta T$		300		ppm/°C	
Wiper Resistance [2]	R_W		50		Ω	V_{DD} =5V, I= V_{DD}/R_{Total}
			80		Ω	V_{DD} =2.7V, I= V_{DD}/R_{Total}
Wiper Current	I_{W}	-1		1	mA	
Divider Mode						
Resolution	N	8			Bits	
Different Non Linearity [2]	DNL	-1	±0.2	+1	LSB	
Integral Non Linearity [2]	INL	-1	±0.2	+1	LSB	
Temperature Coefficient [1]	$\Delta V_w/\Delta T$		+20		ppm/°C	Code = 80h
Full Scale Error	V _{FSE}	-1		0	LSB	Code = Full Scale
Zero Scale Error	V _{ZSE}	0		1	LSB	Code = Zero Scale
Resistor Terminal			•			
Voltage Range	V_A, V_B, V_W	V_{SS}		V_{DD}	V	
Terminal Capacitance [1]	C _A , C _B		30		pF	
Wiper Capacitance [1]			30		pF	
Dynamic Characteristics [1]						
	BW _{10K}		1.5		MHz	V _{DD} =5V, V _B =VSS
Bandwidth –3dB	BW _{50K}		300		KHz	Code = 80h
	BW _{100K}		200		KHz	
Settling Time to 1 LSB	Ts		80	100	uS	
Analog Output (Buffer enable	es)					
Amp Output Current	I _{OUT}	3			mA	V _O =1/2 scale
Amp Output Resistance	Rout		1	10	Ω	I _L = 100uA
Total Harmonic Distortion [1]	THD			0.08	%	V_A =2.5V, V_{DD} =5V, f=1kHz, V_{IN} =1 V_{RMS}
Digital Inputs/Outputs						
Input High Voltage	V_{IH}	0.7V _{DD}			V	
Input Low Voltage	V _{IL}			$0.3V_{DD}$	V	



PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS
Output Low Voltage	V_{OL}			0.4	V	I _{OL} =2mA
Input Leakage Current	I _{LI}	-1		+1	uA	$\overline{\text{CS}} = V_{\text{DD}}, \text{Vin} = \text{Vss} \sim V_{\text{DD}}$
Output Leakage Current	I _{Lo}	-1		+1	uA	$\overline{\text{CS}} = \text{V}_{\text{DD}}, \text{Vin} = \text{V}_{\text{SS}} \sim \text{V}_{\text{DD}}$
Input Capacitance [1]	C _{IN}		25		pF	V _{DD} =5V, fc = 1Mhz
Output Capacitance [1]	C _{OUT}		25		pF	V _{DD} =5V, fc = 1Mhz
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Operating Current	I _{DDR}		0.5	1	mA	All ops except NVMEM program
Operating Current	I _{DDW}		1	2	mA	During Non-volatile memory program
Standby Current	I _{SA} [3]		0.5	1	mA	Buffer is active, NOP, no load
Standby Current	I _{SB} ^[4]		0.1	1	uA	Buffer is inactive, Power Down, No load
Power Supply Rejection Ratio	PSRR			1	LSB/V	V _{DD} =5V±10%, Code=80H

Notes:

[1] Not subject to production test.

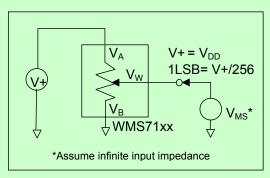
[2] LSB = $(V_A - V_B) / (T - 1)$; DNL = $(V_{i+1} - V_i) / LSB$; INL = $(V_i - i*LSB) / LSB$; where i = [0, (T -1)] and T = # of taps of the device.

[3] WMS71x1 only.

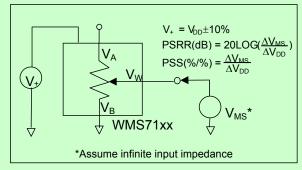
[4] WMS71x0 only.

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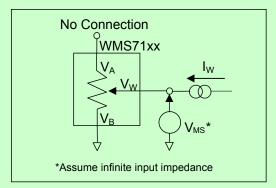
10.1 TEST CIRCUITS



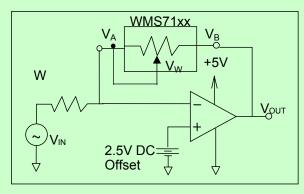
Potentiometer divider nonlinearity error test circuit (INL, DNL)



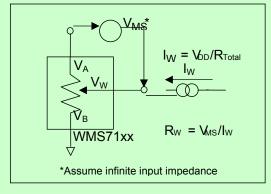
Power supply sensitivity test circuit (PSS, PSRR)



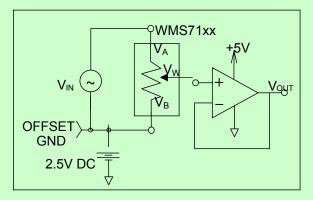
Resistor position nonlinearity error test circuit (Rheostat Operation: R-INL, R-DNL)



Capacitance test circuit



Wiper resistance test circuit



Gain vs. frequency test circuit

FIGURE 4 - TEST CIRCUITS



11. TYPICAL APPLICATION CIRCUITS

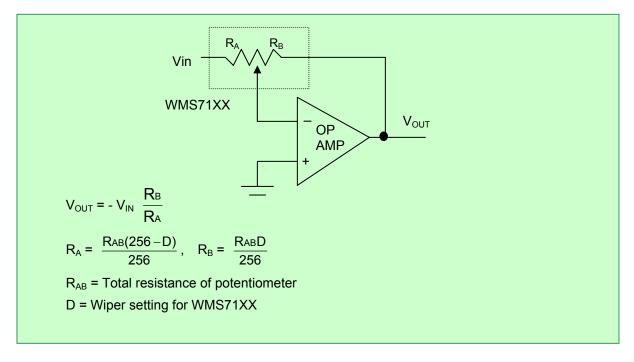


FIGURE 5 - PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE WMS7140/1

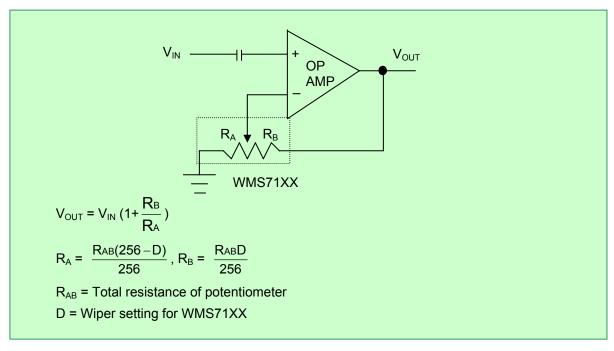


FIGURE 6 – PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE WMS7140/1

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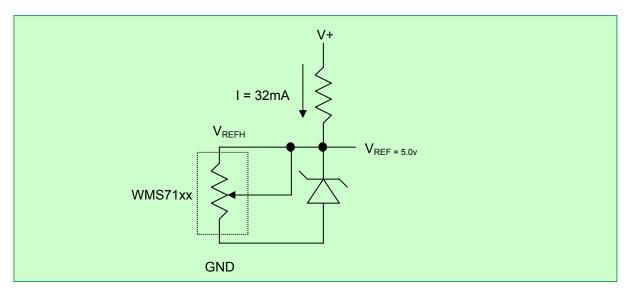


FIGURE 7 - WMS7140/1 TRIMMING VOLTAGE REFERENCE

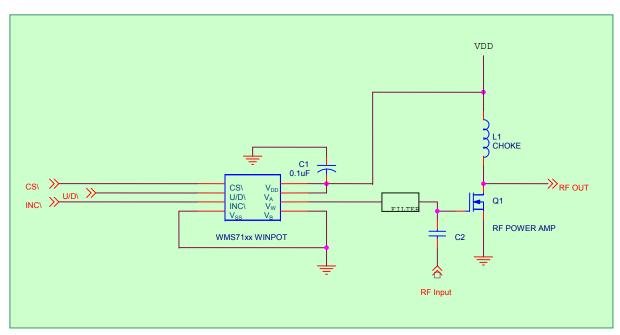


FIGURE 8 – WMS7140/1 RF AMP CONTROL



11.1. LAYOUT CONSIDERATIONS

Use a $0.1\mu F$ bypass capacitor as close as possible to the V_{DD} pin. This is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the V_{DD} and V_{SS} pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

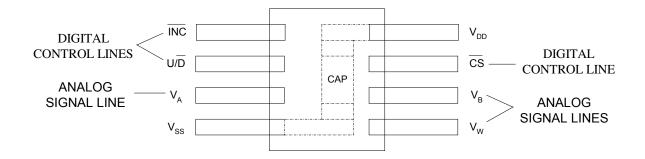


FIGURE 9 - WMS7140/1 LAYOUT



12. PACKAGE DRAWINGS AND DIMENSIONS

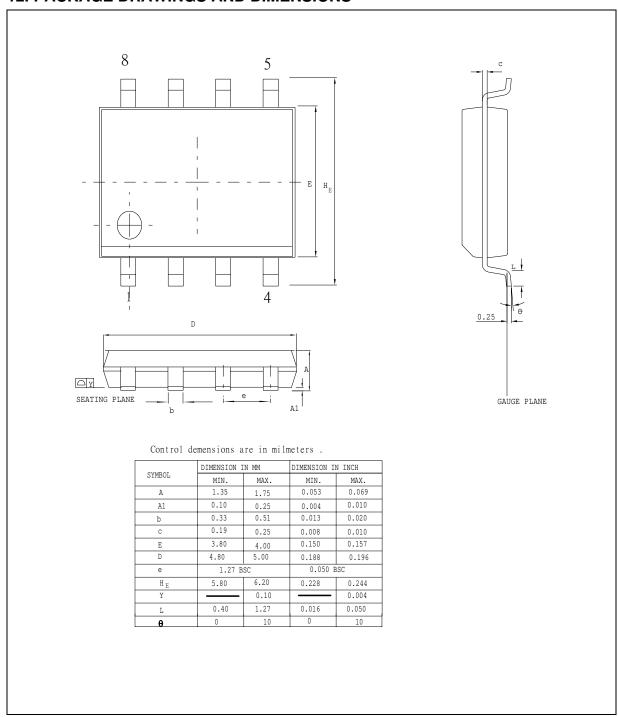


FIGURE 10: 8L 150MIL SOIC

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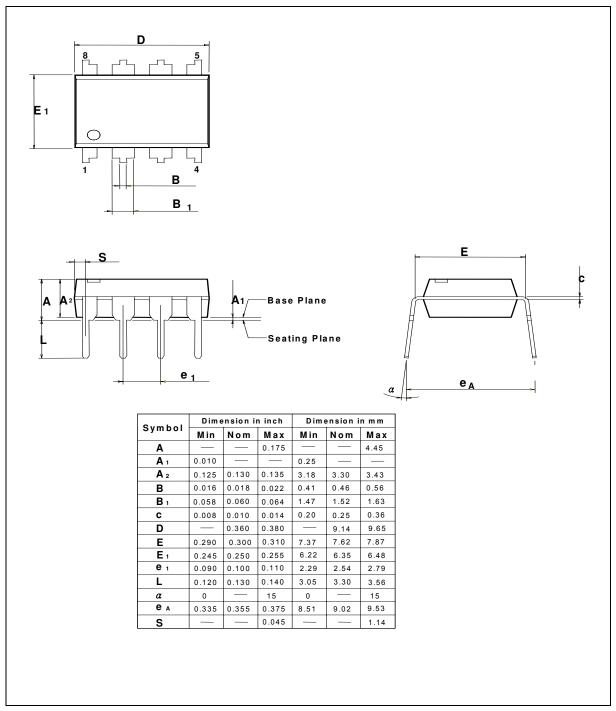


FIGURE 11: 8L 300MIL PDIP

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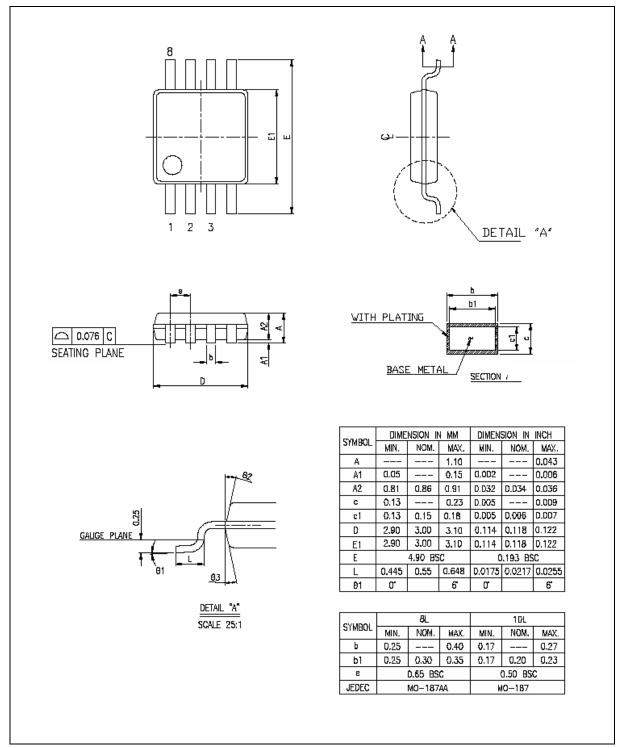
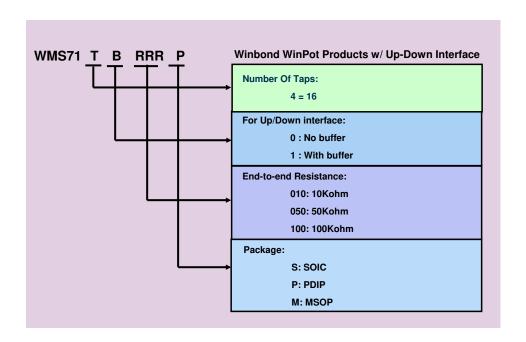


FIGURE 12: 8L 3MM MSOP



13. ORDERING INFORMATION

Winbond's WinPot Part Number Description:



Output Buffer	End-to-End Resistance	SOIC	PDIP	MSOP
NO	10K	WMS7140 010S	WMS7140 010P	WMS7140 010M
	50K	WMS7140 050S	WMS7140 050P	WMS7140 050M
	100K	WMS7140 100S	WMS7140 100P	WMS7140 100M
YES	10K	WMS7141 010S	WMS7141 010P	WMS7141 010M
	50K	WMS7141 050S	WMS7141 050P	WMS7141 050M
	100K	WMS7141 100S	WMS7141 100P	WMS7141 100M

Notes:

Part number with white background: Available for sampling and mass production.

Part numbers with shaded background: Call factory for availability.

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

WMS7140/1



14. VERSION HISTORY

VERSION	DATE	DESCRIPTION			
1.0	June 2003	Initial issue			
1.1	April 2005	Revise disclaim section			

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