Rochester Electronics®

Datasheet

# 74ABT244

## *Octal Buffer/Line Driver with 3-STATE Outputs*

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

FOR REFERENCE ONLY

December 2007

# 74ABT244
# Octal Buffer/Line Driver with 3-STATE Outputs

## Features

- Non-inverting buffers
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50pF and 250pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High-impedance, glitch-free bus loading during entire power up and power down cycle
- Nondestructive, hot-insertion capability
- Disable time less than enable time to avoid bus contention

## General Description

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

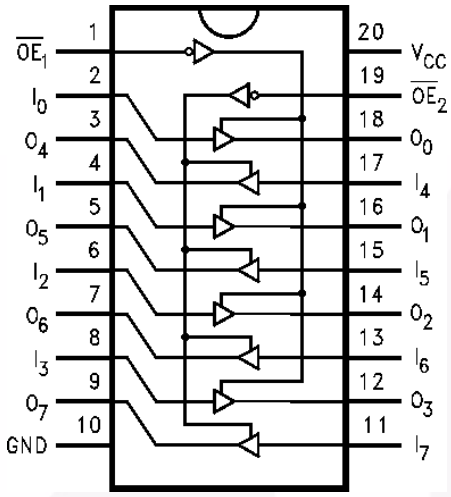
## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ABT244CSC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ABT244CSJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ABT244CMSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74ABT244CMTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | Output Enable Input (Active LOW) |
| $I_0$–$I_7$ | Inputs |
| $O_0$–$O_7$ | Outputs |

## Truth Table

| $\overline{OE}_1$ | $I_{0–3}$ | $O_{0–3}$ | $\overline{OE}_2$ | $I_{4–7}$ | $O_{4–7}$ |
|---|---|---|---|---|---|
| H | X | Z | H | X | Z |
| L | H | H | L | H | H |
| L | L | L | L | L | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_A$ | Ambient Temperature Under Bias | –55°C to +125°C |
| $T_J$ | Junction Temperature Under Bias | –55°C to +150°C |
| $V_{CC}$ | $V_{CC}$ Pin Potential to Ground Pin | –0.5V to +7.0V |
| $V_{IN}$ | Input Voltage(1) | –0.5V to +7.0V |
| $I_{IN}$ | Input Current(1) | –30mA to +5.0mA |
| $V_O$ | Voltage Applied to Any Output | |
| | Disabled or Power-Off State | –0.5V to 5.5V |
| | HIGH State | –0.5V to $V_{CC}$ |
| | Current Applied to Output in LOW State (Max.) | twice the rated $I_{OL}$ (mA) |
| | DC Latchup Source Current | –500mA |
| | Over Voltage Latchup (I/O) | 10V |

**Note:**

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_A$ | Free Air Ambient Temperature | –40°C to +85°C |
| $V_{CC}$ | Supply Voltage | +4.5V to +5.5V |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate | |
| | Data Input | 50mV/ns |
| | Enable Input | 20mV/ns |

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CC}$ | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | Recognized HIGH Signal | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | Recognized LOW Signal | | | 0.8 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | Min. | $I_{IN}$ = –18mA | | | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | | Min. | $I_{OH}$ = –3mA | 2.5 | | | V |
| | | | | $I_{OH}$ = –32mA | 2.0 | | | |
| $V_{OL}$ | Output LOW Voltage | | | $I_{OL}$ = 64mA | | | 0.55 | V |
| $I_{IH}$ | Input HIGH Current | | Max. | $V_{IN}$ = 2.7V[3] | | | 1 | µA |
| | | | | $V_{IN}$ = $V_{CC}$ | | | 1 | |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | Max. | $V_{IN}$ = 7.0V | | | 7 | µA |
| $I_{IL}$ | Input LOW Current | | Max. | $V_{IN}$ = 0.5V[3] | | | –1 | µA |
| | | | | $V_{IN}$ = 0.0V | | | –1 | |
| $V_{ID}$ | Input Leakage Test | | 0.0 | $I_{ID}$ = 1.9µA, All Other Pins Grounded | 4.75 | | | V |
| $I_{OZH}$ | Output Leakage Current | | 0–5.5V | $V_{OUT}$ = 2.7V, $\overline{OE}_n$ = 2.0V | | | 10 | µA |
| $I_{OZL}$ | Output Leakage Current | | 0–5.5V | $V_{OUT}$ = 0.5V, $\overline{OE}_n$ = 2.0V | | | –10 | µA |
| $I_{OS}$ | Output Short-Circuit Current | | Max. | $V_{OUT}$ = 0.0V | –100 | | –275 | mA |
| $I_{CEX}$ | Output High Leakage Current | | Max. | $V_{OUT}$ = $V_{CC}$ | | | 50 | µA |
| $I_{ZZ}$ | Bus Drainage Test | | 0.0 | $V_{OUT}$ = 5.5V, All Others GND | | | 100 | µA |
| $I_{CCH}$ | Power Supply Current | | Max. | All Outputs HIGH | | | 50 | µA |
| $I_{CCL}$ | Power Supply Current | | Max. | All Outputs LOW | | | 30 | mA |
| $I_{CCZ}$ | Power Supply Current | | Max. | $\overline{OE}_n$ = $V_{CC}$, All Others at $V_{CC}$ or Ground | | | 50 | µA |
| $I_{CCT}$ | Additional $I_{CC}$/Input | Outputs Enabled | Max. | $V_I$ = $V_{CC}$ – 2.1V | | | 2.5 | mA |
| | | Outputs 3-STATE | | Enable Input $V_I$ = $V_{CC}$ – 2.1V | | | 2.5 | mA |
| | | Outputs 3-STATE | | Data Input $V_I$ = $V_{CC}$ – 2.1V, All Others at $V_{CC}$ or Ground | | | 50 | µA |
| $I_{CCD}$ | Dynamic $I_{CC}$ No Load[3] | | Max. | Outputs OPEN, $\overline{OE}_n$ = GND[2], One-Bit Toggling, 50% Duty Cycle | | | 0.1 | mA/ MHz |

**Notes:**

2. For 8-bit toggling, $I_{CCD}$ < 0.8mA/MHz.
3. Guaranteed, but not tested.

## DC Electrical Characteristics

SOIC package.

| Symbol | Parameter | $V_{CC}$ | Conditions $C_L = 50pF$, $R_L = 500\Omega$ | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | $T_A = 25°C$[4] | | 0.5 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | $T_A = 25°C$[4] | –1.3 | –0.8 | | V |
| $V_{OHV}$ | Minimum HIGH Level Dynamic Output Voltage | 5.0 | $T_A = 25°C$[6] | 2.7 | 3.1 | | V |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | $T_A = 25°C$[5] | 2.0 | 1.5 | | V |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | $T_A = 25°C$[5] | | 1.1 | 0.8 | V |

**Notes:**

4. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
5. Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$). Guaranteed, but not tested.
6. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics

SOIC and SSOP package.

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50pF$ | | | $T_A = –55°C$ to $+125°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50pF$ | | $T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50pF$ | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ | Propagation Delay Data to Outputs | 1.0 | 2.5 | 3.6 | 1.0 | 5.3 | 1.0 | 3.6 | ns |
| $t_{PHL}$ | | 1.0 | 2.3 | 3.6 | 1.0 | 5.0 | 1.0 | 3.6 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | 3.5 | 6.0 | 0.8 | 6.5 | 1.5 | 6.0 | ns |
| $t_{PZL}$ | | 1.5 | 3.6 | 6.0 | 1.2 | 7.9 | 1.5 | 6.0 | |
| $t_{PHZ}$ | Output Disable Time | 1.7 | 3.5 | 5.6 | 1.2 | 7.6 | 1.7 | 5.6 | ns |
| $t_{PLZ}$ | | 1.7 | 3.3 | 5.6 | 1.0 | 7.9 | 1.7 | 5.6 | |

## Extended AC Electrical Characteristics

SOIC package.

| Symbol | Parameter | $T_A$–40°C to +85°C, $V_{CC}$ = 4.5V–5.5V, $C_L$ = 50pF, 8 Outputs Switching[7] | | | $T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5V–5.5V, $C_L$ = 250pF, 1 Output Switching[8] | | $T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5V–5.5V, $C_L$ = 250pF, 8 Outputs Switching[9] | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $f_{TOGGLE}$ | Max Toggle Frequency | | 100 | | | | | | MHz |
| $t_{PLH}$ | Propagation Delay, Data to Outputs | 1.5 | | 5.0 | 1.5 | 6.0 | 2.5 | 8.5 | ns |
| $t_{PHL}$ | | 1.5 | | 5.0 | 1.5 | 6.0 | 2.5 | 8.5 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | | 6.5 | 2.5 | 7.5 | 2.5 | 10.0 | ns |
| $t_{PZL}$ | | 1.5 | | 6.5 | 2.5 | 7.5 | 2.5 | 12.0 | |
| $t_{PHZ}$ | Output Disable Time | 1.0 | | 5.6 | (10) | | (10) | | ns |
| $t_{PLZ}$ | | 1.0 | | 5.6 | | | | | |

**Notes:**

7. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
8. This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
9. This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
10. The 3-STATE delays are dominated by the RC network (500Ω, 250pF) on the output and have been excluded from the datasheet.

## Skew

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50pF$, 8 Outputs Switching[13] | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250pF$, 8 Outputs Switching[14] | Units |
|---|---|---|---|---|
| | | Max. | Max. | |
| $t_{OSHL}$[11] | Pin to Pin Skew, HL Transitions | 0.8 | 1.8 | ns |
| $t_{OSLH}$[11] | Pin to Pin Skew, LH Transitions | 0.8 | 1.8 | ns |
| $t_{PS}$[15] | Duty Cycle, LH–HL Skew | 1.0 | 2.5 | ns |
| $t_{OST}$[11] | Pin to Pin Skew, LH/HL Transitions | 1.0 | 2.5 | ns |
| $t_{PV}$[12] | Device to Device Skew, LH/HL Transitions | 1.5 | 3.0 | ns |

**Notes:**

11. Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW ($t_{OSHL}$), LOW-to-HIGH ($t_{OSLH}$), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW ($t_{OST}$). The specification is guaranteed but not tested.
12. Propagation delay variation for a given set of conditions (i.e., temperature and $V_{CC}$) from device to device. This specification is guaranteed but not tested.
13. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)
14. These specifications guaranteed but not tested. The limits represent propagation delays with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
15. This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

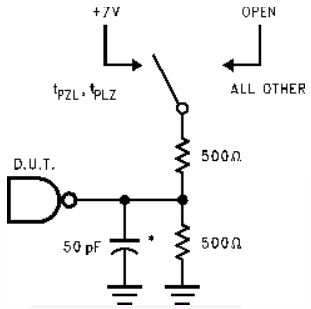
## Capacitance

| Symbol | Parameter | Conditions $T_A = 25°C$ | Typ. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC} = 0V$ | 5.0 | pF |
| $C_{OUT}$[16] | Output Capacitance | $V_{CC} = 5.0V$ | 9.0 | pF |

**Note:**

16. $C_{OUT}$ is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

## AC Loading




*Includes jig and probe capacitance

**Figure 1. Standard AC Test Load**

## AC Waveforms

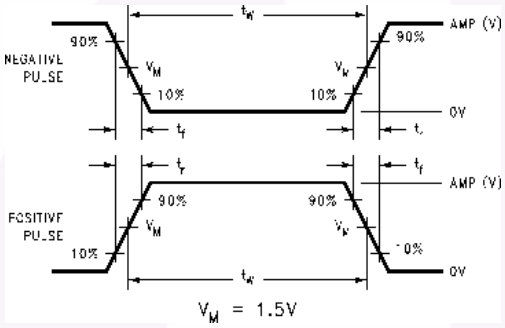



**Figure 2. Test Input Signal Levels**

| Amplitude | Rep. Rate | $t_W$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500ns | 2.5ns | 2.5ns |

**Figure 3. Test Input Signal Requirements**

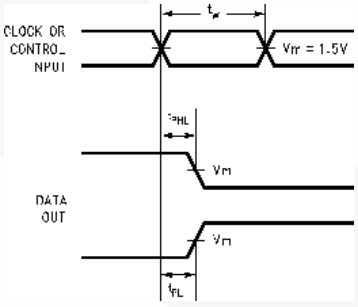



**Figure 4. Propagation Delay, Pulse Width Waveforms**

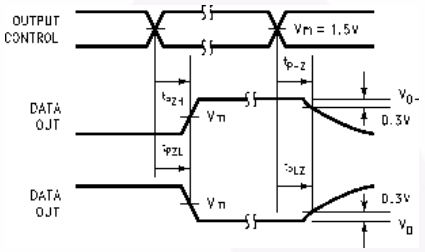



**Figure 5. 3-STATE Output HIGH and LOW Enable and Disable Times**

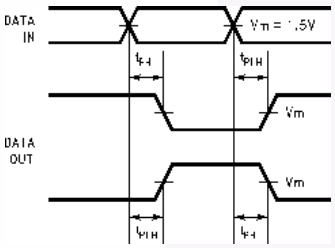



**Figure 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

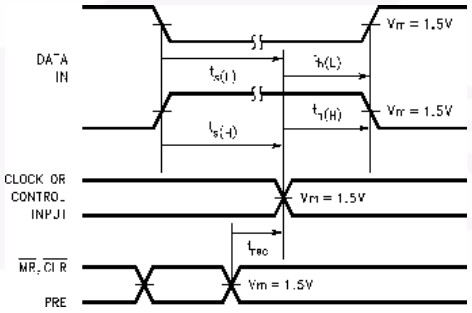



**Figure 7. Setup Time, Hold Time and Recovery Time Waveforms**

## Physical Dimensions

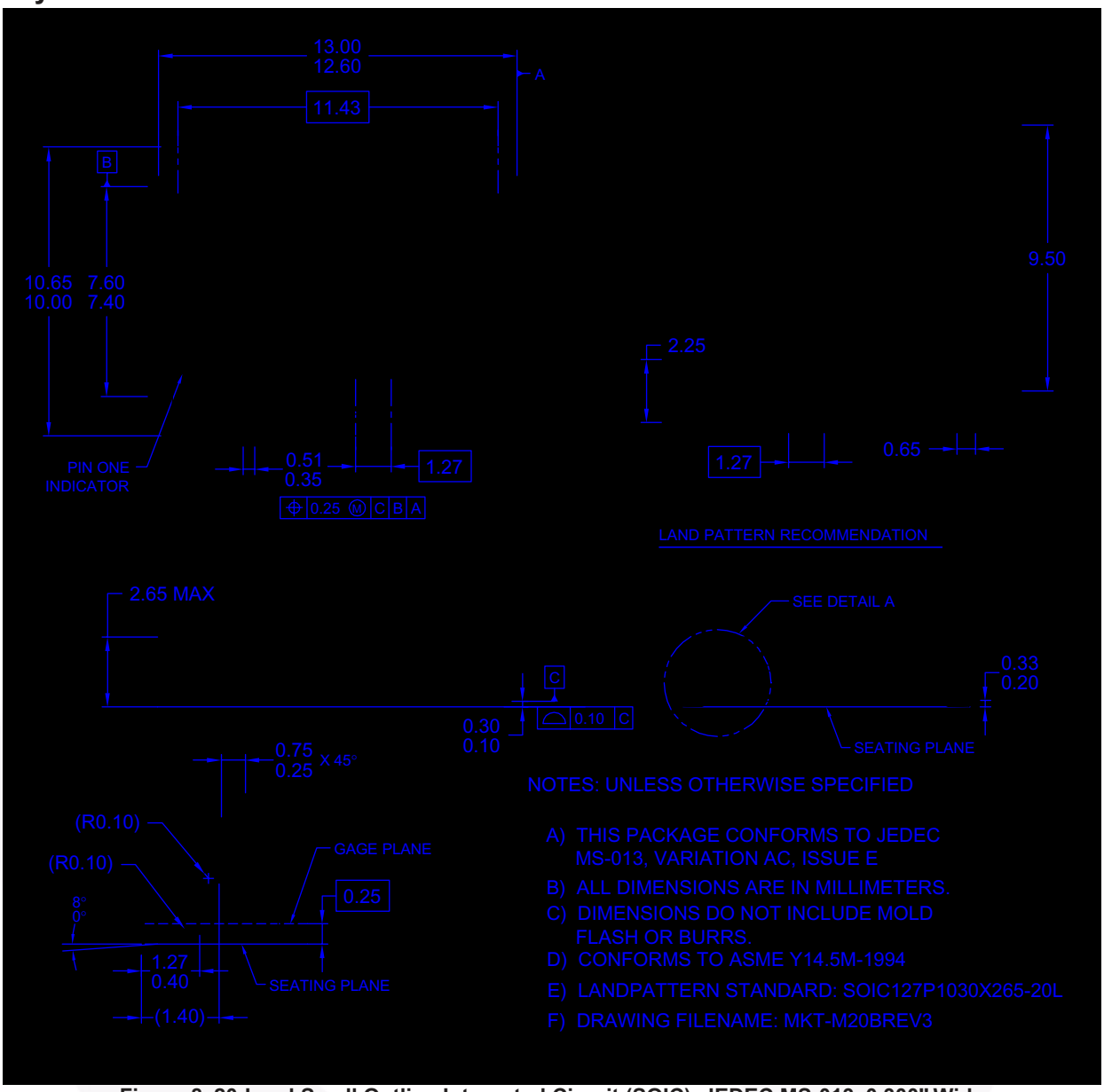



**Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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## Physical Dimensions (Continued)

**Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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## Physical Dimensions (Continued)

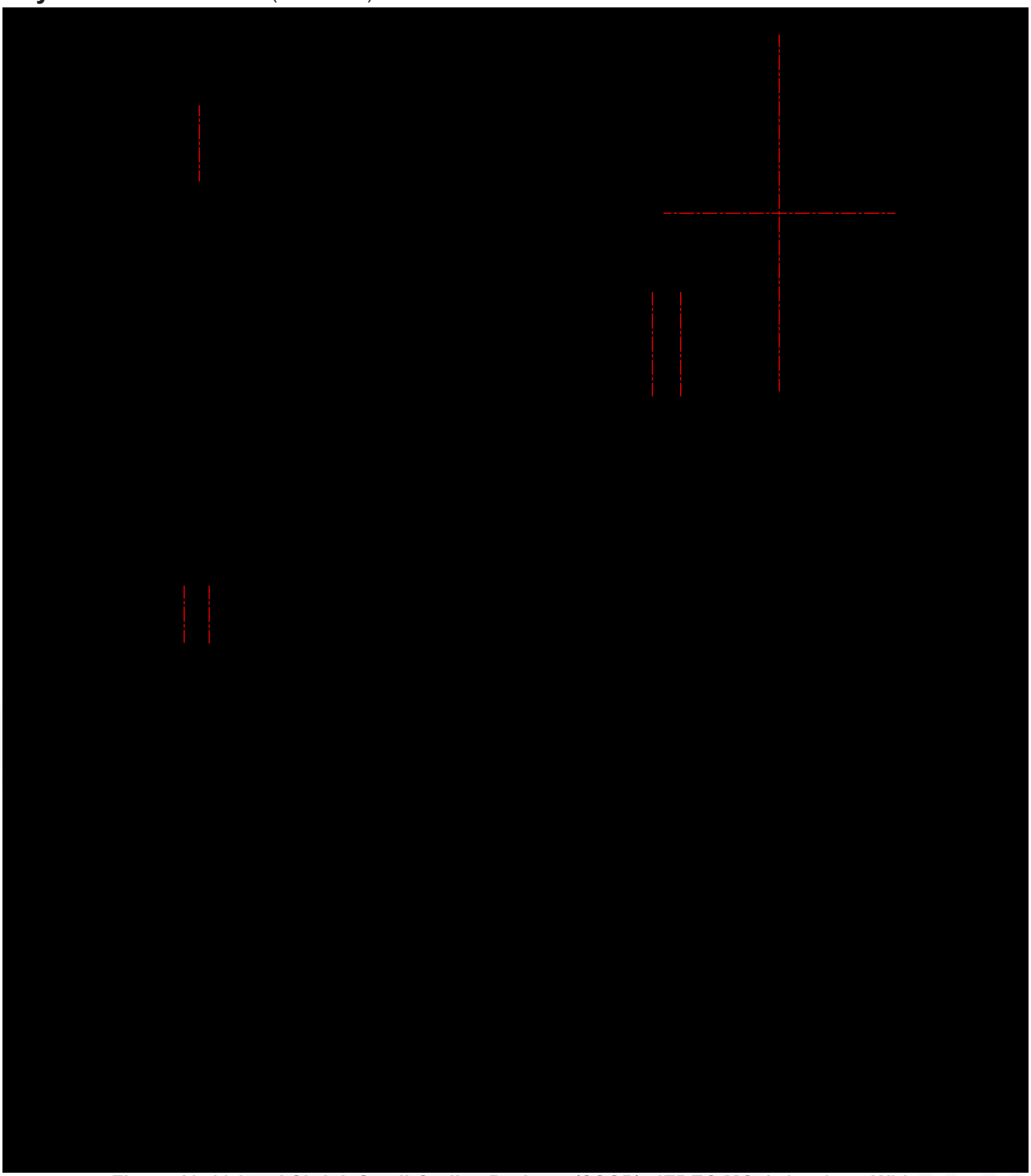

**Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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## Physical Dimensions (Continued)

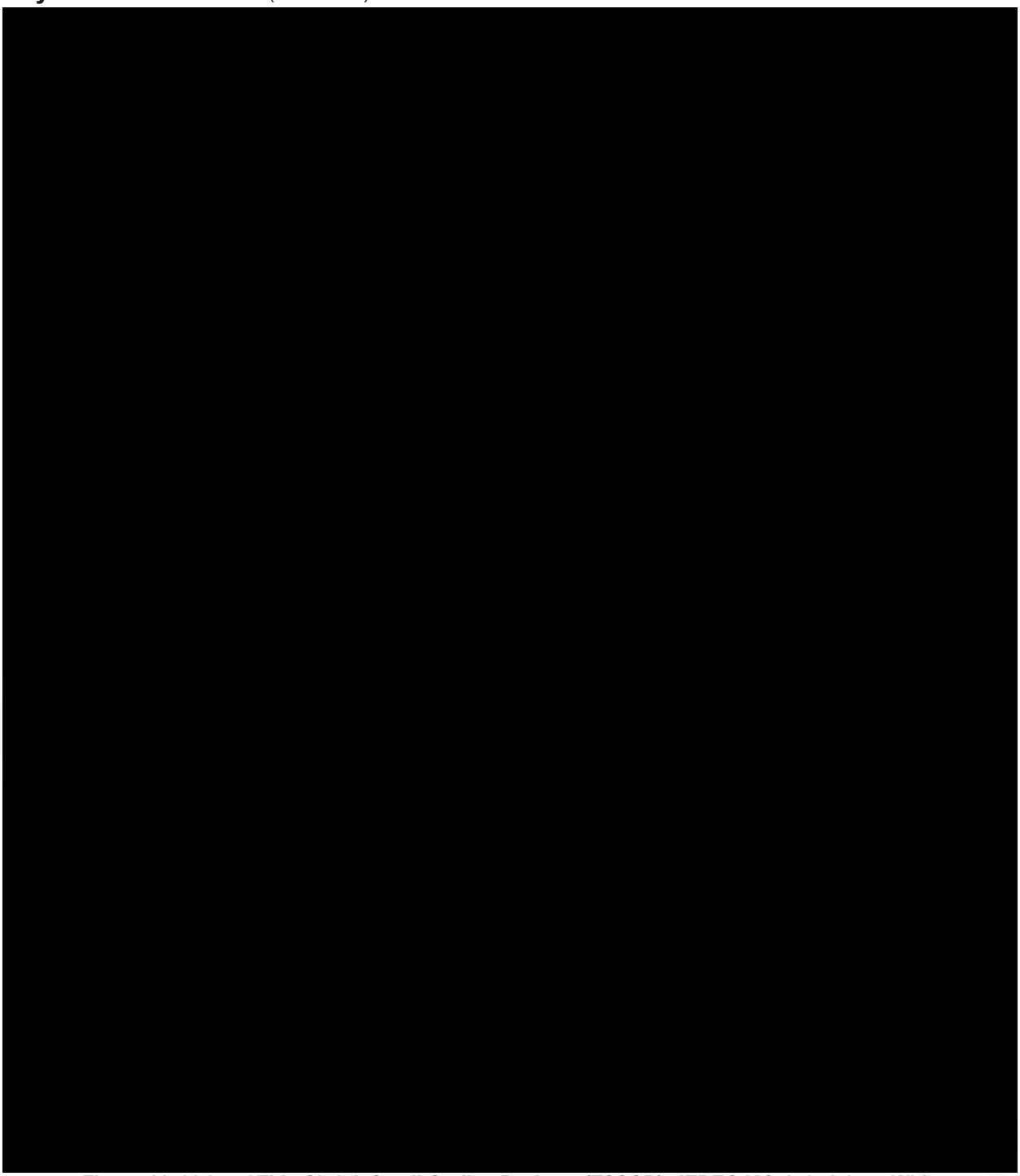

**Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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