5A Constant Frequency Hysteretic Synchronous Regulator

Description

The NX9415 is synchronous buck switching converter in a multi chip module designed for step-down DC to DC converter applications. It is optimized to convert bus voltages from 8V to 22V to as low as 0.8V output voltage. The output current can be up to 5A. An internal regulator converts bus voltage to 5V, which provides a voltage supply to the internal logic and driver circuits. The NX9415 operates from 200 kHz to 2.2MHz and employs loss-less current limiting by sensing the R_{DSON} of synchronous MOSFET followed by hiccup feature. Feedback under voltage protection triggers hiccup.

Other features of the device are: internal Schottky diode, thermal shutdown, 5V gate drive, adaptive deadband control, internal digital soft start, 5VREG under-voltage lock out and shutdown capability via the comp pin. NX9415 is available in 4x4 MCM package.

Features

- Single Supply Voltage From 8V to 22V
- Internal 5V Regulator
- Programmable Frequency Up to 2.2MHz
- Internal Digital Soft Start Function
- Internal Boost Schottky Diode
- Prebias Startup
- Less than 50 nS Adaptive Deadband
- Current Limit Triggers Hiccup by Sensing R_{DSON} of Synchronous MOSFET
- Pb-free and RoHS Compliant

Applications

- Low Profile On board DC to DC Application
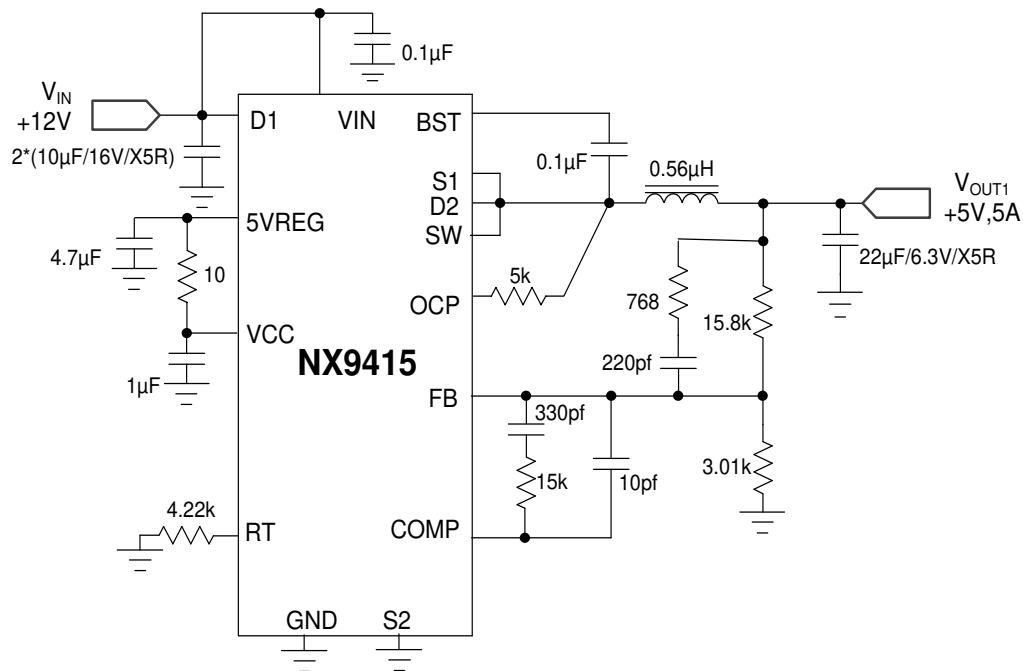- LCD TV
- Hard Disk Drive
- ADSL Modem

Figure 1 · **Typical Application of NX9415**
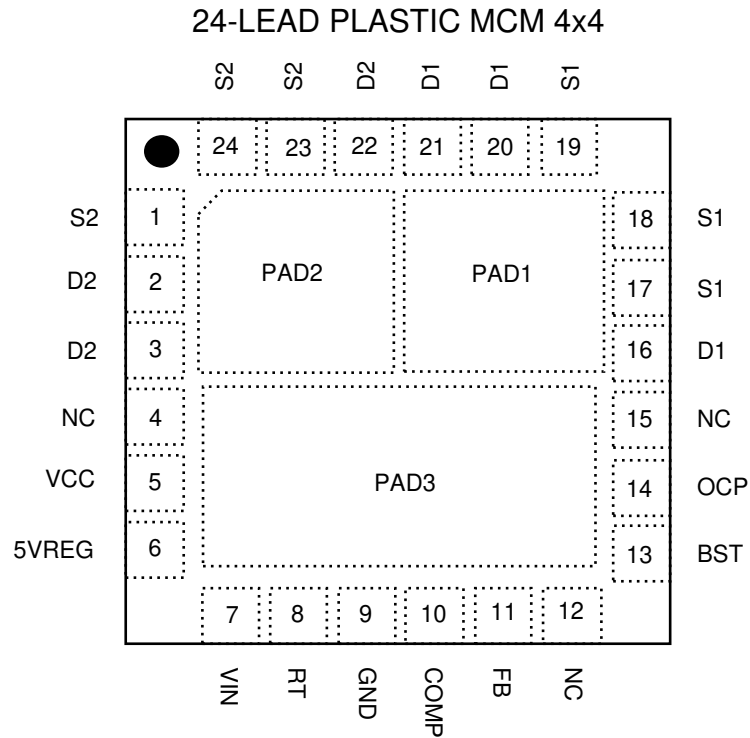
Pin Configuration and Pinout

24-LEAD PLASTIC MCM 4x4

Figure 2 · **Pinout**

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
0°C to 70°C	RoHS Compliant Pb-free	4X4 MCM-24L	NX9415CM	Bulk / Tube
			NX9415CMTR	Tape and Reel

Pin Description

| Pin Number	Pin Designator	Description
1, 23-24	S2	Source of low side MOSFET and needs to be connected to power ground.
2-3,22, PAD2	D2	Drain of low side MOSFET.
4, 12, 15, PAD3	NC	Not used pin. Connecting these pins to ground is recommended.
5	VCC	Voltage supply for internal analog circuit and driver
6	5VREG	An internal 5V regulator. A high frequency 4.7µF/X5R ceramic capacitor must be connected from this pin to the GND pin as close as possible.
7	VIN	Voltage supply for the internal 5V regulator.
8	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.
9	GND	Ground.
10	COMP	This pin is the output of the error amplifier and is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
11	FB	This pin is the error amplifier inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
13	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1µF must be connected from this pin to SW pin.
14	OCP	This pin is connected to the D2 of the low side MOSFET and is the input of the over current protection (OCP) comparator. A fixed internal current flows to the external resistor which sets the OCP voltage across the R_{DSON} of the low side MOSFET. Current limit point is this voltage divided by the R_{DSON}.
16, 21-20, PAD1	D1	Drain of high side MOSFET
17-19	S1	Source of high side MOSFET and provides return path for the high side driver.

Block Diagram
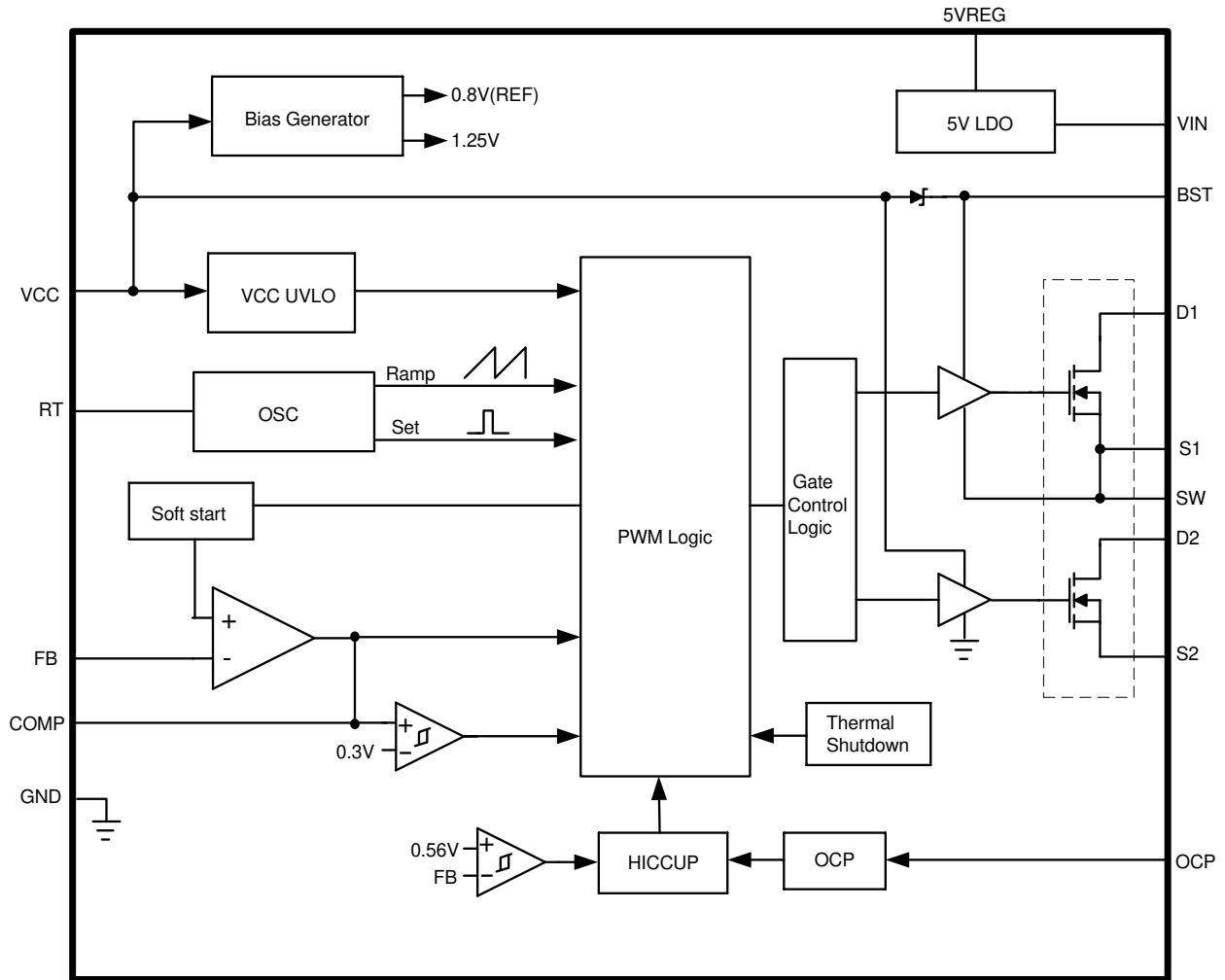
Figure 3 · **Simplified Block Diagram of NX9415**

Absolute Maximum Ratings

Note: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
5VREG,VCC to GND & BST to SW voltage	-0.3	6.5	V
VIN to GND Voltage	-	25	V
S1 to GND	-2	30	V
D1 to S1, D2 to S2	-	30	V
All other pins	-0.3	VCC+0.3, or 6.5	V
Storage Temperature Range	-65	150	°C
Operating Junction Temperature Range	-40	125	°C
Peak Reflow Temperature (40 seconds)		260 (+0, -5)	°C
ESD Susceptibility		2	kV
Power Dissipation	Internally Limited by OTP		

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	30	°C/W
θ_{JC}	2.5	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN = 12V, and T_A = 0 to 70°C. Following are the bypass capacitors: C_{VIN} = 1µF, C_{5VREG} = 4.7µF, and all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Reference Voltage						
VREF	Ref Voltage			0.8		V
	Ref Voltage line regulation	VIN= 9V to 22V		0.4		%
5VREG						
	5VREG Voltage range		4.75	5	5.25	V
	5VREG Line Regulation	VIN= 9V to 22V		10		mV
	5VREG Max Current			50		mA

Electrical Characteristics - continued

Unless otherwise specified, these specifications apply over VIN = 12V, and T_A = 0 to 70°C. Following are the bypass capacitors: C_{VIN} = 1µF, C_{5VREG} = 4.7µF, and all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Supply Voltage (VIN)						
VIN	VIN Voltage Range		9		22	V
	Input Voltage Current (Static)	No switching		4.8		mA
	Input Voltage Current (Dynamic)	R_{RT}= 4.22kΩ		10		mA
VIN UVLO						
VIN_UVLO	VIN-Threshold	V_{IN} Rising		6.5		V
VIN_Hyst	VIN-Hysteresis	V_{IN} Falling		0.6		V
Under Voltage Lockout						
VCC_UVLO	VCC Threshold	VCC Rising		3.9		V
VCC_Hyst	VCC Hysteresis	VCC Falling		0.2		V
SS						
T_{ss}	Soft Start time	F_S= 2.2MHz		400		µs
Oscillator (RT)						
F_S	Frequency	R_{RT} = 4.22kΩ		2250		kHz
V_{RAMP}	Ramp Amplitude Voltage			1.5		V
	Max Duty Cycle	F_S= 2.2MHz		71		%
	Min Controllable On Time				150	ns
Error Amplifiers						
	Transconductance			2000		µmho
I_B	Input Bias Current			10		nA
	COMP SD Threshold			0.3		V
FBUVLO						
	Feedback UVLO threshold			0.6		V
	Over temperature Threshold			150		°C
	Hysteresis			20		°C
OCP						
	OCP current			37		µA
Internal Schottky Diode						
	Forward voltage drop	Forward current = 20mA		350		mV
Output Stage						
	High Side MOSFET RDSON			31		mΩ
	Low Side MOSFET RDSON			31		mΩ
	Output Current			5		A

Typical Application

- Input Voltage = 12V, Output Voltage ~ 5V@ 5A, Working Frequency ~ 2.2MHz
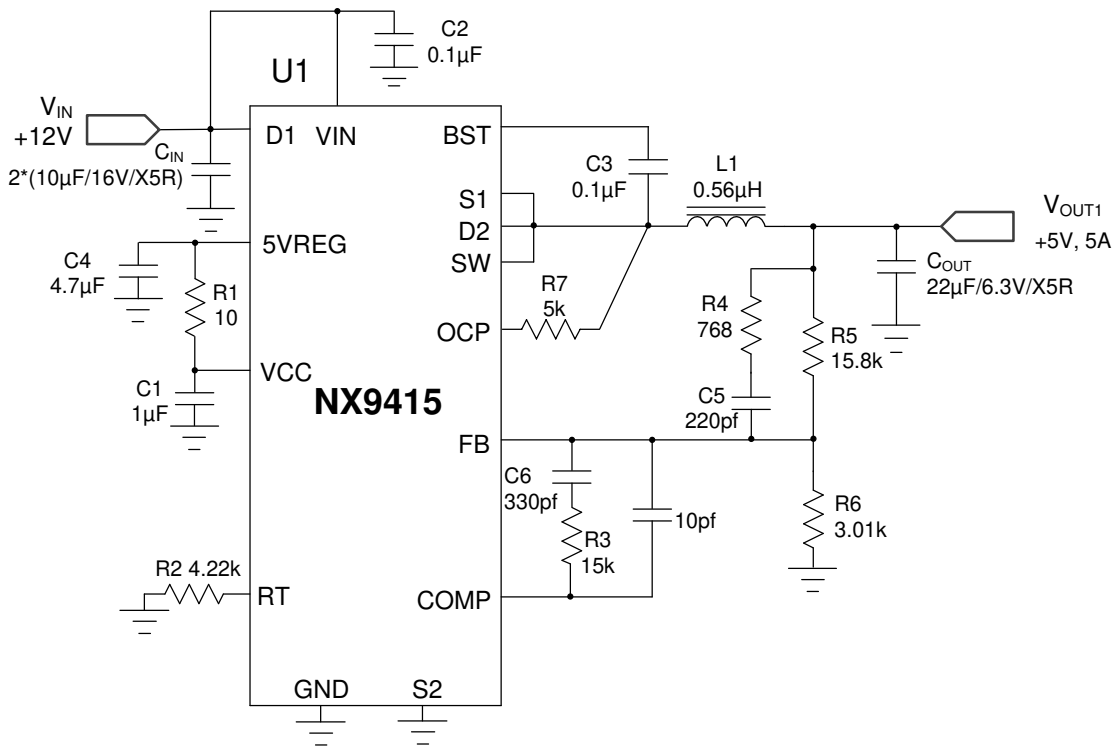
Figure 4 · **Demo Board Schematic**

Bill of Materials

Item	Quantity	Reference	Value	Manufacturer
1	1	C1	1µF	
2	2	C2,C3	0.1µF	
3	1	C4	4.7µF/6.3V/X5R	
4	1	C5	220pf	
5	1	C6	330pf	
6	2	CIN	10µF/16V/X5R	
7	1	COUT	22µF/6.3V/X5R	
8	1	L1	DO1813P-561HC	Coilcraft
9	1	R1	10Ω	
10	1	R2	4.22kΩ	
11	1	R3	15kΩ	
12	1	R4	768Ω	
13	1	R5	15.8kΩ	
14	1	R6	3.01kΩ	
15	1	R7	5kΩ	
16	1	U1	NX9415CM	Microsemi

Theory of Operation

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. A typical internal current source of 37µA flowing through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCPSW} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over-current occurs.
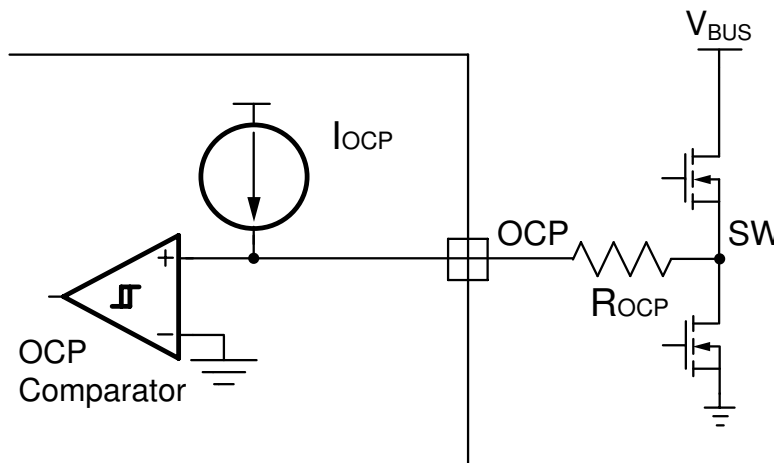
Figure 5 · **Over Current Protection**

The over current limit can be set by the following equation:

$$I_{SET} = \frac{I_{OCP} \times R_{OCP}}{K \times R_{DSON}}$$

K is temperature coefficient of R$_{DSON}$, the recommended value is 1.4.

Demoboard Waveforms
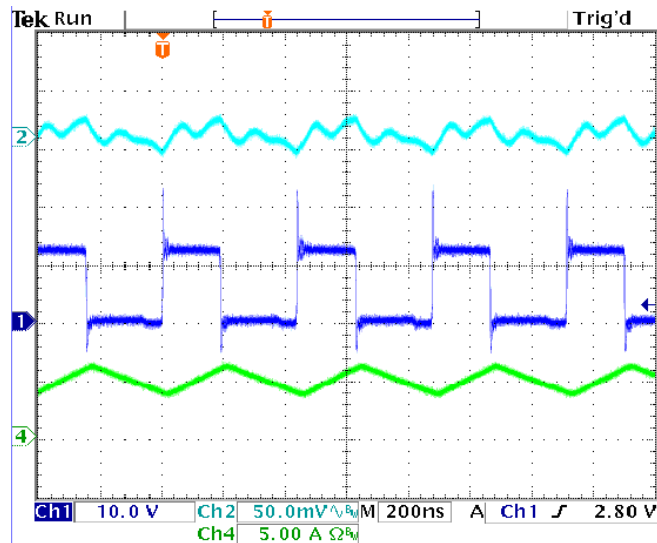
Figure 6 · **Output Ripple (CH1 SW 10V/DIV, CH2 VOUT AC 50mV/DIV, CH4 OUTPUT CURRENT 5A/DIV)**
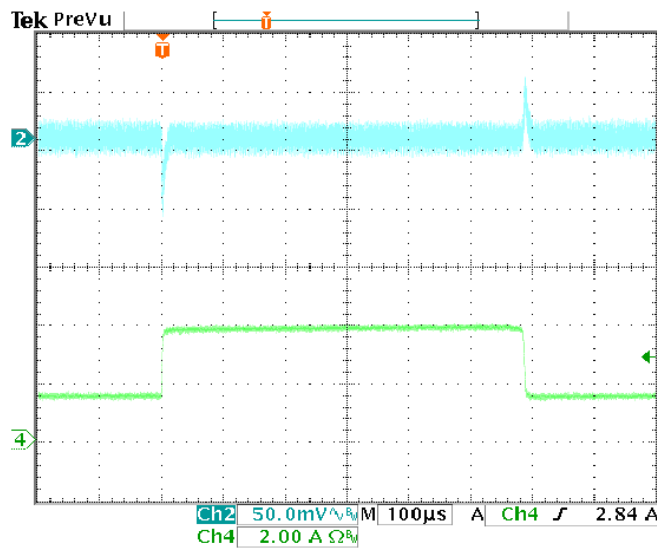
Figure 7 · **Output Voltage Transient Response (CH2 VOUT AC 50mV/DIV, CH4 OUTPUT CURRENT 5A/DIV)**
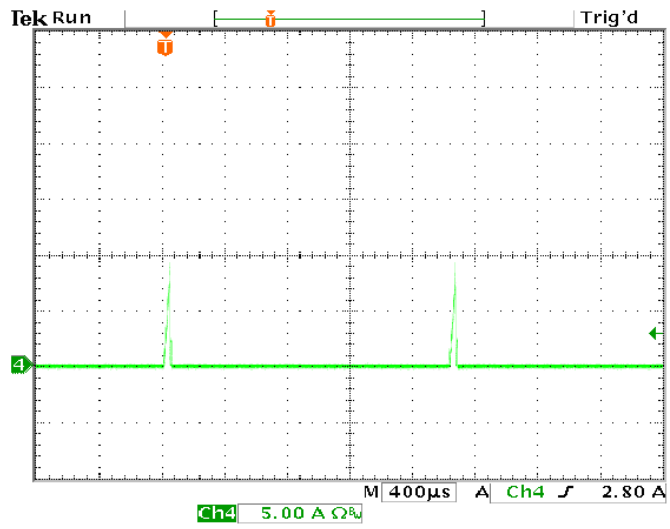
Figure 8 · **Over Current Protection(CH4 OUTPUT CURRENT 5A/DIV)**
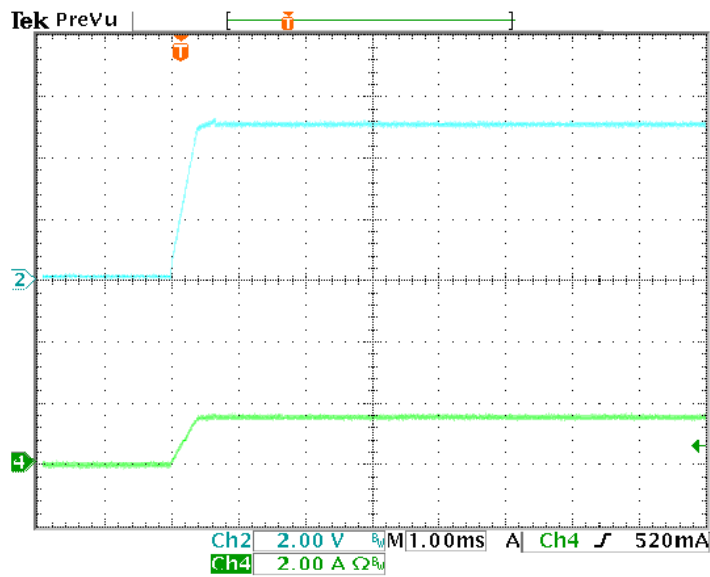
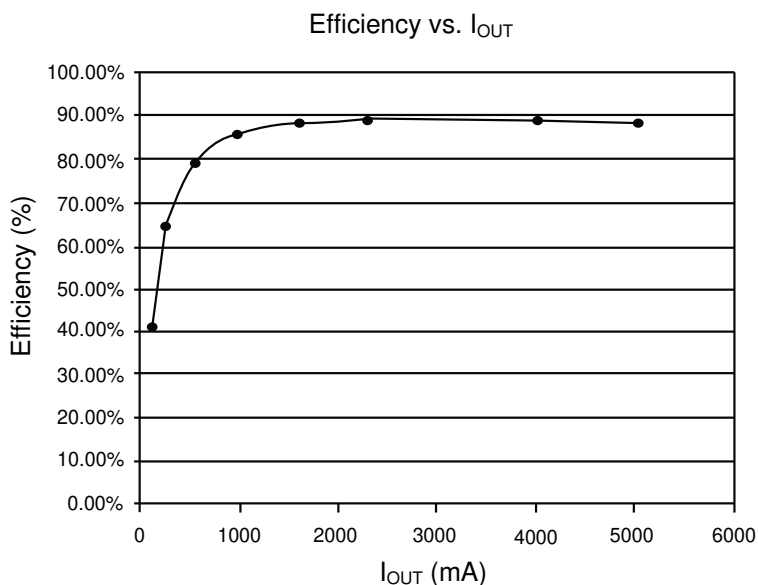Figure 9 · **Startup (CH2 VOUT 2V/DIV, CH4 CURRENT 2A/DIV)**

Efficiency vs. I_{OUT}

Figure 10 · **Output Efficiency @V$_{OUT}$=5V, V$_{IN}$=12V**

Application Information

Symbol Used In Application Information:

Symbol	Description
VIN	Input voltage
V$_{OUT}$	Output voltage
I$_{OUT}$	Output current
ΔV$_{RIPPLE}$	Output voltage ripple
F$_S$	Working frequency
ΔI$_{RIPPLE}$	Inductor current ripple

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{VIN - V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S}$$

$$I_{RIPPLE} = K \times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state (DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both conditions. The amount of voltage ripple during the DC load condition is determined by the following equation:

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

Where ESR is the output capacitors' equivalent series resistance, C_{OUT} is the value of output capacitors. Typically when ceramic capacitors are selected as output capacitors, DC ripple spec is easy to be met, but multiple ceramic capacitors are required at the output to meet transient requirement.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has $180^°$ phase shift, and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than $50^°$ and the gain crossing 0dB with 20dB/decade.

Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III Compensator Design

For low ESR output capacitors, typically such as Sanyo Os-Con and Poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator.

The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R_2 + R_3) \times C_3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R_3 \times C_3}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}}$$

Where, F_{Z1}, F_{Z2}, F_{P1}, and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10. The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m \times Z_f}{1 + g_m \times Z_{in} + Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: $R_4 >> 2/gm$. And it would be desirable if $R_1||R_2||R_3 >> 1/gm$ can be met at the same time.
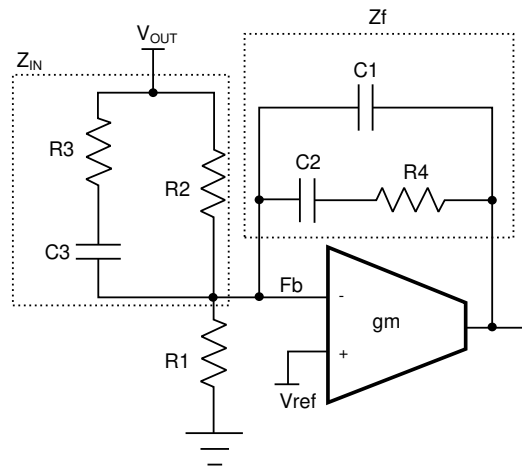

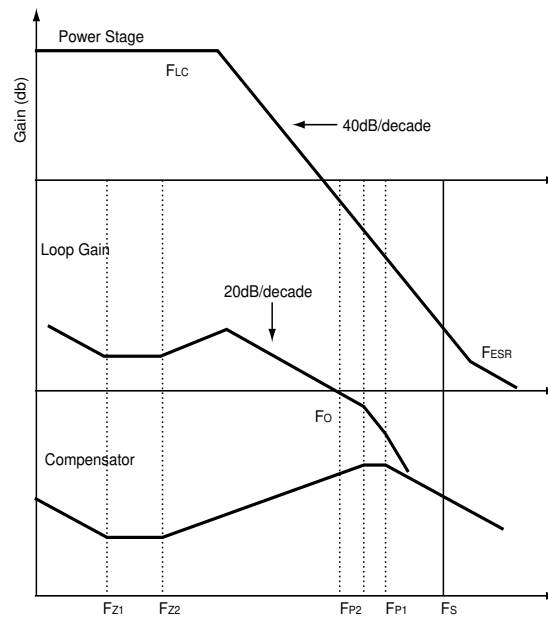Figure 11 · **Type III Compensator using Transconductance Amplifier**

Figure 12 · **Bode Plot of Type III Compensator**

B. Type II Compensator Design

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 12. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1 + R_2} \times R_3$$

$$F_Z = \frac{1}{2 \times \pi \times R_3 \times C_1}$$

$$F_P \approx \frac{1}{2 \times \pi \times R_3 \times C_2}$$

For this type of compensator, FO has to satisfy $F_{LC} < F_{ESR} << F_O <= 1/10 \sim 1/5 F_s$.
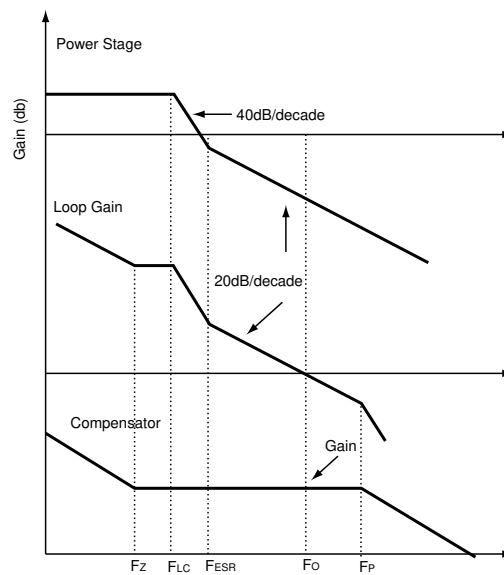
Figure 13 · **Bode Plot of Type II Compensator**
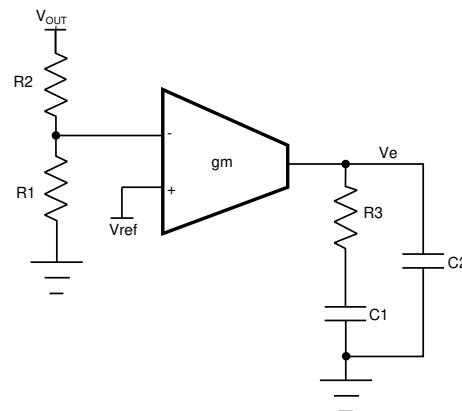
Figure 14 · **Type II Compensator with Transconductance Amplifier**

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT}, V_{REF}, and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}}$$

Where, R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider. See compensator design for R_1 and R_2 selection.
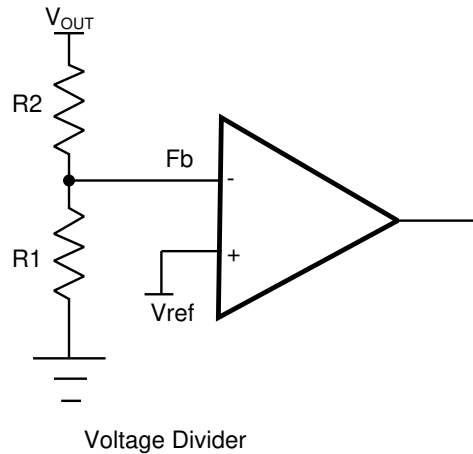
Voltage Divider

Figure 15 · **Voltage Divider**

Frequency Selection

The frequency can be set by external RT resistor. The relationship between frequency and RT pin is shown as follows:
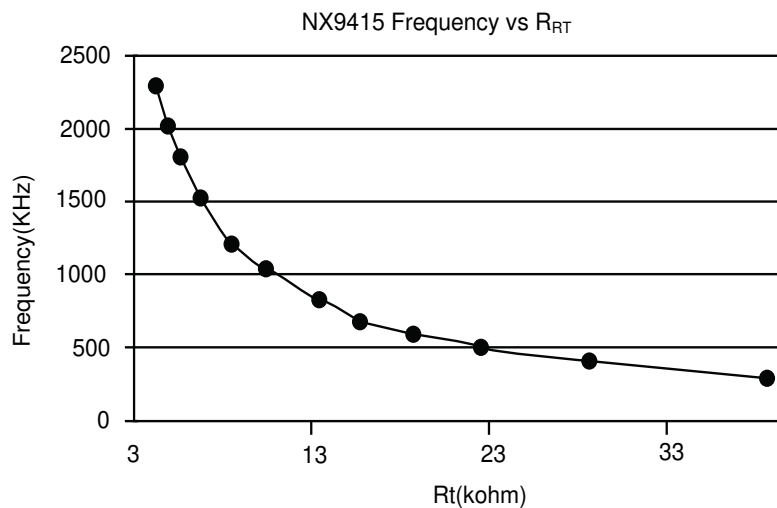
Figure 16 · **Frequency Versus RT Resistor**
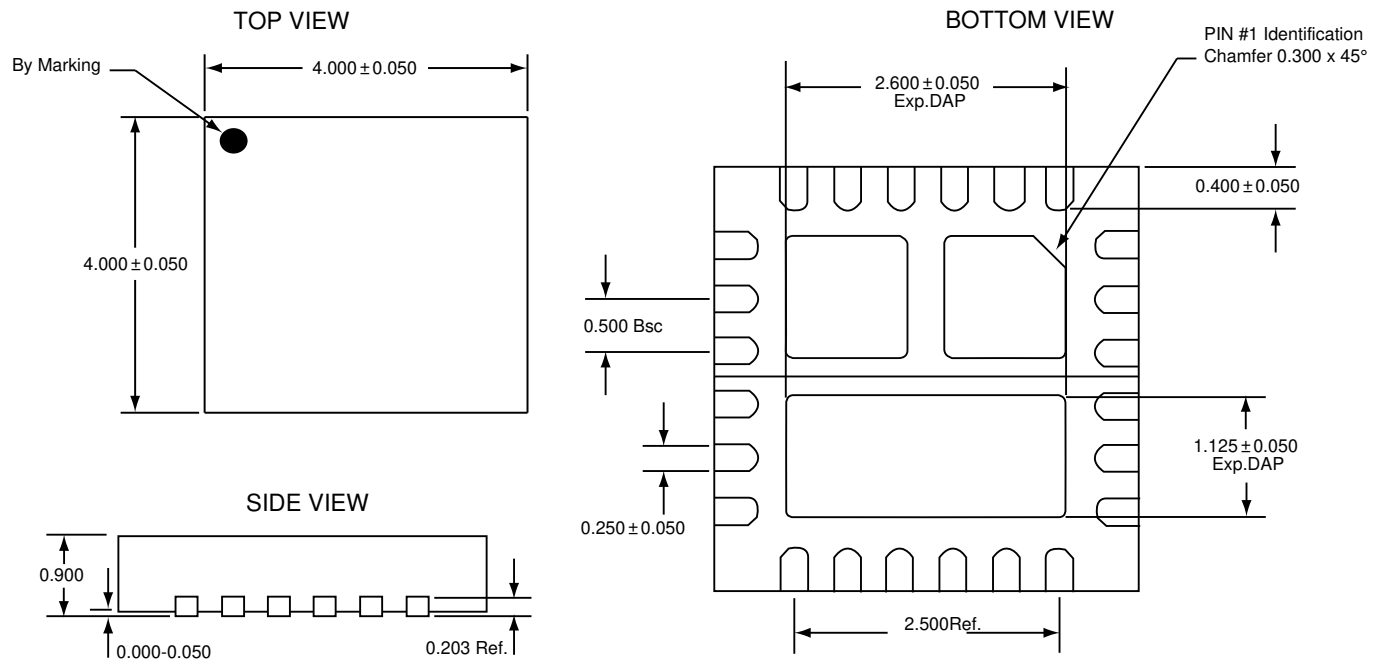
MCM 24 PIN 4 x 4 PACKAGE OUTLINE DIMENSIONS

Figure 17 · Package Dimensions

Note: All dimensions are displayed in millimeters.