DLP® Digital Controller for the DLP1700 DMD

Check for Samples: DLPC100

FEATURES

- **Optimized to Operate With DLPR100 and DLP1700**
- **Single 24-Bit Input Port (RGB or BT656-YUV) With Pixel Clock Support up to 30 MHz**
- **Input Image Size 320 x 240 (QVGA), 480 x 320 (HVGA), or 640 x 480 (VGA)**
- **Three RGB Input Color Bit-Depth Options: RGB888, RGB666, RGB565**
- **Supports 1 Hz to 60 Hz Frame Rates**
- **I²C Control Interface for Device Configuration**
- **Pixel Data Processing:**
  - **Color Space Conversion**
  - **Chroma Interpolation for 4:2:2 to 4:4:4 Conversion**
  - **Color Coordinate Adjustment**
  - **Image Resizing (Scaling)**
  - **De-Interlacing Via Field Scaling**
  - **Frame Rate Conversion**
  - **LED Current Control Adjustment**
  - **Programmable Degamma**
  - **Spatial-Temporal Multiplexing (Dithering)**
  - **Automatic Gain Control**
- **60 MHz Double Data Rate (DDR) DMD Interface**
- **External Memory Support: 100 MHz SDR SDRAM**
- **Serial FLASH Interface**
- **System Control:**
  - **Programmable LED Currents**
  - **DMD Power and Reset Driver Control**
  - **DMD Horizontal and Vertical Image Flip**
  - **Built-in Test Pattern Generation**
- **JTAG with Boundary Scan Test Support**
- **Packaged in 256-Pin Ultra Fineline Ball-Grid Array (uBGA)**

DESCRIPTION

The DLPC100 performs all the image processing and control, along with DMD data formatting, for driving a 0.17 HVGA DMD (DLP1700).

The DLPC100 is one of three components in the 0.17 HVGA Chipset (see Figure 1). Proper function and operation of the DLP1700 requires that it be used in conjunction with the other components of the 0.17 HVGA Chip-Set. Refer to the 0.17 HVGA Chip-Set Data Sheet for further details (TI literature number DLPS017).

In DLP electronics solutions, image data is 100% digital from the DLPC100 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC100 processes the digital input image and converts the data into a format needed by the DMD. The DMD then reflects light to the screen using binary pulse-width-modulation (PWM) for each pixel mirror.

Commands can be input to the DLPC100 over an I²C interface.

The digital input interface switching levels, for image data, is nominally 1.8 V, 2.5 V, or 3.3 V. The switching level used is selected by setting pin INTFPWR to 1.8 V, 2.5 V, or 3.3 V. The input image interface and I²C interface switching levels must be the same.

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.17 HVGA Chip-Set data sheet	DLPS017
DLPR100 Configuration PROM data sheet	DLPS020
DLP1700 0.17 HVGA DMD data sheet	DLPS018

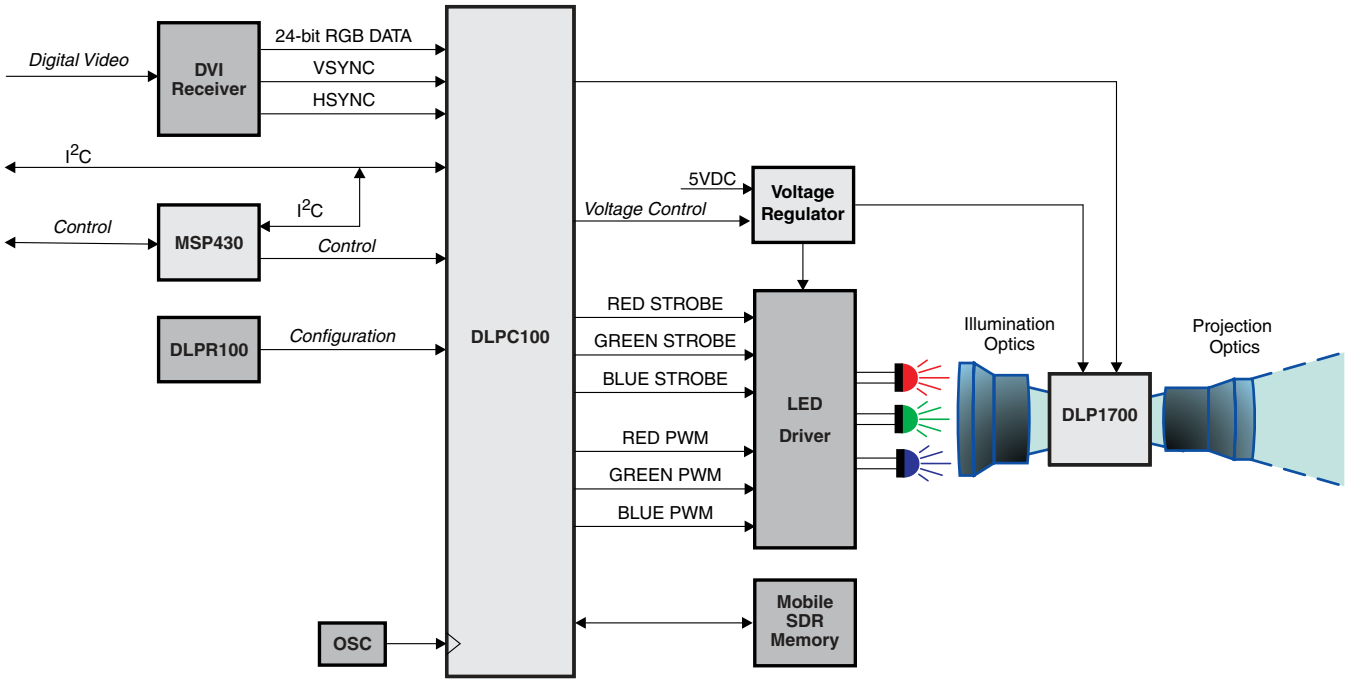


Figure 1. Typical Application

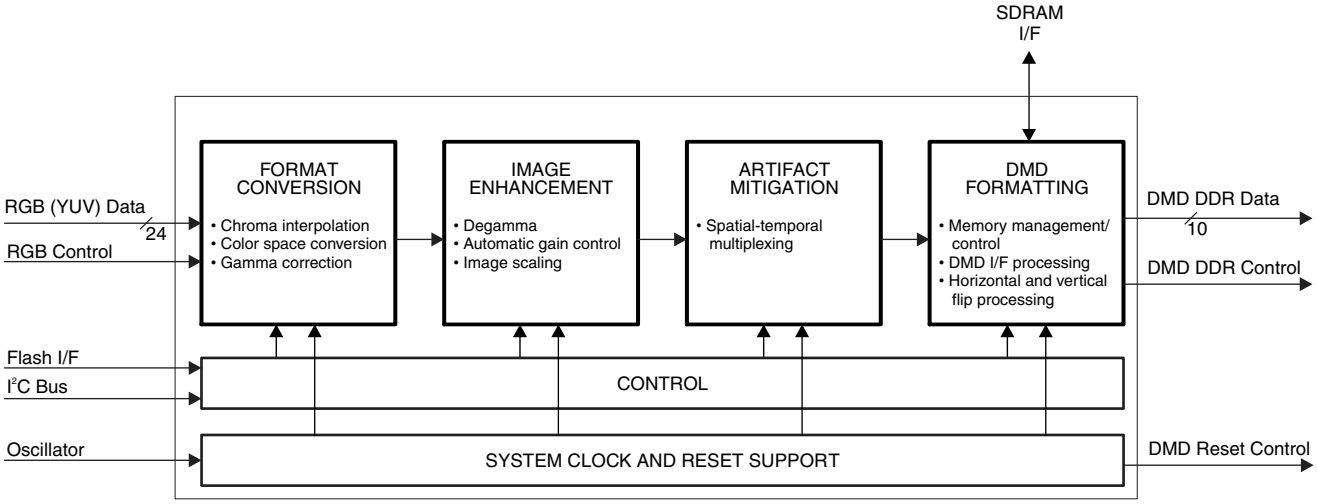


Figure 2. Functional Block Diagram

Projector Image Port Signal Sharing

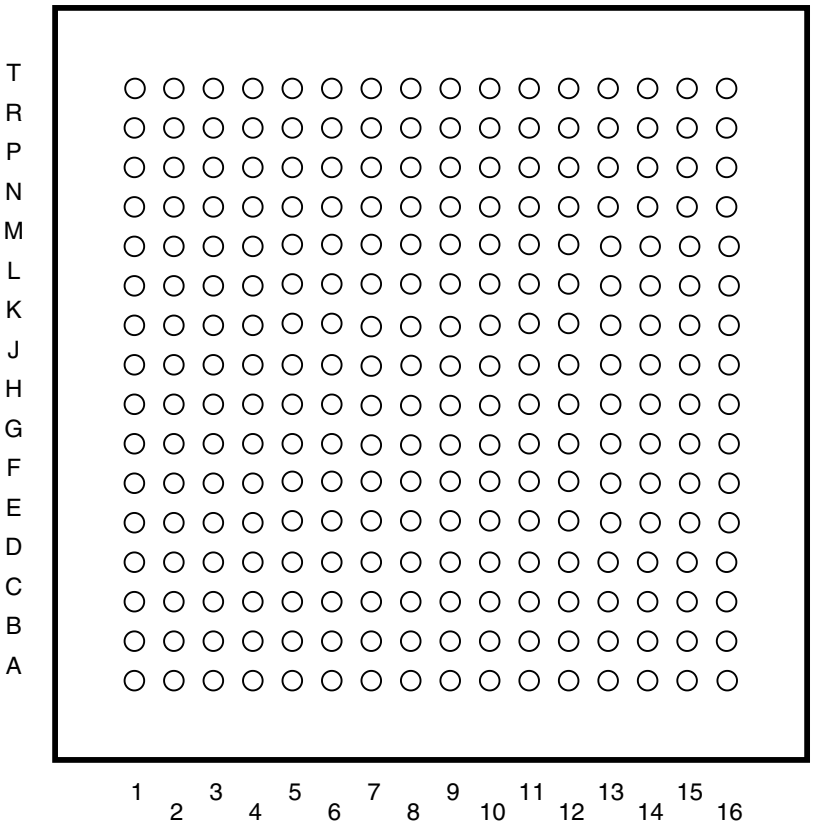
Figure 2 illustrates the basic processing that occurs in the controller. The DLPC100 provides a single input port for graphics and motion video inputs. The signals listed below support two input interface modes. Thus some signals have different uses depending on the input interface mode being used.

Below are the two input image interface modes, signal descriptions, and pins needed on the DLPC100. describes all the signals in the DLPC100.

- BT.656, 9 pins
  - PDATA(7-0) – Projector Data
  - PCLK – Projector Clock (rising edge to capture input data)
- Parallel Bus, 20 pins or 22 pins or 28 pins
  - PDATA(15-0) or PDATA(17-0) or PDATA(23-0) – Projector Data
  - HSYNC – Horizontal Sync
  - VSYNC – Vertical Sync
  - DATEN – Data En (active high)
  - PCLK – Projector Clock (rising edge, or falling edge, to capture input data)

The Terminal Functions table describes the input/output characteristics of signals that interface to the DLPC100 by functional groups. Signals are referenced by names shown in the Pico Projector Formatter Reference Schematic, TI drawing 2509552. The voltage characteristics of various I/O types are described in the I/O Characteristics table.

ZCT PACKAGE
(BOTTOM VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O TYPE	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
CFG_DATA	H2	I1	CFG_DCLK	Data input from DLPR100 device
CFG_DCLK	H1	O1	CFG_DCLK	DLPR100 data clock
CFG_ASDO	C1	O1	CFG_DCLK	Serial data output. This pin sends address and control information to the DLPR100 during configuration.
MSEL_2	G12	I1	Asynch	Mode selection signals. (Must be tied low for proper operation)
MSEL_1	H12	I1	Asynch	Mode selection signals. (Must be tied high for proper operation)
MSEL_0	H13	I1	Asynch	Mode selection signals. (Must be tied low for proper operation)
$\overline{CE}$	J3	I1	Asynch	Configuration chip enable. Active low.
$\overline{CFG}$	H5	I1	Asynch	Configuration control. Configuration will start when a low to high transition is detected at this pin.
NSTATUS	F4	B1	CFG_DCLK	Configuration status pin.
CFG_DONE	H14	B1	CFG_DCLK	Configuration Done status pin. Signal goes high at the end of configuration.
Board Level Test & Debug				
JTAG_TDI	H4	I2	JTAG_TCK	JTAG, serial data in
JTAG_TCK	H3	I3	N/A	JTAG, serial data clock
JTAG_TMS	J5	I2	JTAG_TCK	JTAG, test mode select
JTAG_TDO	J4	O1	JTAG_TCK	JTAG, serial data out
System Interfaces				
CLK_IN	E16	I4	N/A	Input oscillator clock (60 MHz)
$\overline{RESET}$	L8	I5	Async	Device reset (active low)
PWRGOOD	T3	I5	Async	System power good indicator
P_SCL	R3	B2	N/A	I^2C clock
P_SDA	L3	B2	N/A	I^2C data
I2C_ADDR_SEL	R9	I4	Async	I^2C address selection (low = device address x36)
Reserved	M16	I4	Async	Reserved. Must be tied to GND for DLPC100.
Reserved	G15	I4	Async	Not used. Pin reserved for future use.
Test/Debug Interfaces				
SpareIn_B8	B8	I1,4,5	N/A	Reserved. Should be tied to GND to minimize power.
SpareIn_B9	B9			
SpareIn_E1	E1			
SpareIn_E15	E15			
SpareIn_E2	E2			
SpareIn_M1	M1			
SpareIn_M15	M15			
SpareIn_M2	M2			
SpareIn_A9	A9			
SpareIn_T9	T9			

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
AUXSYNC0	P6	O1,3,4	N/A	TESTx outputs are Reserved for factory testing. AUXSYNC0-4 are available for Pattern Display Synchronization. See associated application note.
TEST1	P11			
TEST2	P14			
TEST3	L14			
TEST4	J13			
TEST5	J15			
TEST6	J16			
TEST7	D16			
AUXSYNC1	G16			
AUXSYNC2	F14			
AUXSYNC3	D15			
AUXSYNC4	C16			
TEST12	C11			
TEST13	C15			
TEST14	B16			
TEST15	F13			
TEST16	D1			
TEST17	F16			
TEST18	F15			
TEST19	G15			
TEST20	G1			
TEST21	M8			
TEST22	N8			

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O TYPE	CLOCK SYSTEM	DESCRIPTION	
NAME	NO.				
Main Video Data & Control					
				PARALLEL RGB	**BT.656**
PCLK	R8	I5	N/A	Clock	Clock
VSYNC_WE	T5	I6	PCLK	Vsync	Unused
HSYNC_CS	R4	I6	PCLK	Hsync	Unused
DATEN_CMD	N3	I6	PCLK	Active data	Unused
Reserved_RFU	T4	O5	PCLK	Unused	Unused
PDATA0	T2	I5	PCLK	Data	Data0
PDATA1	R5	I5	PCLK	Data(1)	Data1
PDATA2	P2	I5	PCLK	Data(1)	Data2
PDATA3	N5	I5	PCLK	Data(1)	Data3
PDATA4	N2	I5	PCLK	Data(1)	Data4
PDATA5	P8	I5	PCLK	Data(1)	Data5
PDATA6	L2	I5	PCLK	Data(1)	Data6
PDATA7	T7	I5	PCLK	Data(1)	Data7
PDATA8	K2	I5	PCLK	Data(1)	Unused
PDATA9	R7	I5	PCLK	Data(1)	Unused
PDATA10	J2	I5	PCLK	Data(1)	Unused
PDATA11	M7	I5	PCLK	Data(1)	Unused
PDATA12	R1	I5	PCLK	Data(1)	Unused
PDATA13	L7	I5	PCLK	Data(1)	Unused
PDATA14	P1	I5	PCLK	Data(1)	Unused
PDATA15	M6	I5	PCLK	Data(1)	Unused
PDATA16	N1	I5	PCLK	Data(1)	Unused
PDATA17	N6	I5	PCLK	Data(1)	Unused
PDATA18	L1	I5	PCLK	Data(1)	Unused
PDATA19	P3	I5	PCLK	Data(1)	Unused
PDATA20	K1	I5	PCLK	Data(1)	Unused
PDATA21	R6	I5	PCLK	Data(1)	Unused
PDATA22	J1	I5	PCLK	Data(1)	Unused
PDATA23	T6	I5	PCLK	Data(1)	Unused
DMD Interface					
DMD_D0	P9	O3	DMD_CLK	DMD data pins. DMD Data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK.	
DMD_D1	R16	O3	DMD_CLK		
DMD_D2	R13	O3	DMD_CLK		
DMD_D3	R12	O3	DMD_CLK		
DMD_D4	R11	O3	DMD_CLK		
DMD_D5	L15	O3	DMD_CLK		
DMD_D6	J14	O3	DMD_CLK		
DMD_D7	L13	O3	DMD_CLK		
DMD_D8	N16	O3	DMD_CLK		
DMD_D9	N15	O3	DMD_CLK		
DMD_DCLK	N12	O3	N/A	DMD data clock	
DMD_LOADB	N9	O3	DMD_CLK	DMD data serial control signal	
DMD_SCTRL	P16	O3	DMD_CLK	DMD data load signal	

(1) 24-bit data is mapped according to RGB565/RGB666/RGB888 pixel format. See Figure 3.

TERMINAL FUNCTIONS (continued)

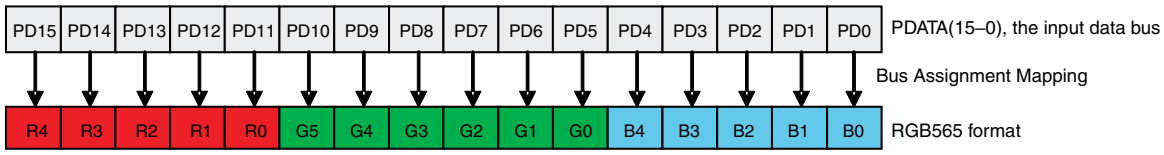
TERMINAL		I/O TYPE	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
DMD_TRC	T10	O3	DMD_CLK	DMD data toggle rate control
DMD_A0	T11	O3	DMD_CLK	DMD reset address 0
DMD_A1	T14	O3	DMD_CLK	DMD reset address 1
DMD_A2	T12	O3	DMD_CLK	DMD reset address 2
DMD_SEL0	K16	O3	DMD_CLK	DMD reset select 0
DMD_SEL1	T15	O3	DMD_CLK	DMD reset select 1
DMD_MODE	R10	O3	DMD_CLK	DMD reset mode
DMD_STROBE	T13	O3	DMD_CLK	DMD reset strobe
DMD_SACBUS	L16	O3	DMD_CLK	DMD serial bus data
DMD_SACCLK	K15	O3	DMD_CLK	DMD serial bus clock
DMD_OEZ	R14	O3	DMD_CLK	DMD reset output enable
DMD_PWR_EN	G5	O3	N/A	DMD power regulator enable
RESERVED	H16	O3	N/A	Pin reserved for future use
RESERVED	H15	I4	N/A	Not used. Pin reserved for future use.
SDRAM Interface				
MEM_A0	D12	O2	MEM_CLK	Multiplexed row and column address 0 for the SDRAM
MEM_A1	B12	O2	MEM_CLK	Multiplexed row and column address 1 for the SDRAM
MEM_A2	B14	O2	MEM_CLK	Multiplexed row and column address 2 for the SDRAM
MEM_A3	C14	O2	MEM_CLK	Multiplexed row and column address 3 for the SDRAM
MEM_A4	D14	O2	MEM_CLK	Multiplexed row and column address 4 for the SDRAM
MEM_A5	A15	O2	MEM_CLK	Multiplexed row and column address 5 for the SDRAM
MEM_A6	A13	O2	MEM_CLK	Multiplexed row and column address 6 for the SDRAM
MEM_A7	B13	O2	MEM_CLK	Multiplexed row and column address 7 for the SDRAM
MEM_A8	A14	O2	MEM_CLK	Multiplexed row and column address 8 for the SDRAM
MEM_A9	B3	O2	MEM_CLK	Multiplexed row and column address 9 for the SDRAM
MEM_A10	A12	O2	MEM_CLK	Multiplexed row and column address 10 for the SDRAM
MEM_A11	D11	O2	MEM_CLK	Multiplexed row and column address 11 for the SDRAM
MEM_BA0	B11	O2	MEM_CLK	Bank select for the SDRAM
MEM_BA1	A11	O2	MEM_CLK	Bank select for the SDRAM
$\overline{\text{MEM\_RAS}}$	C9	O2	MEM_CLK	Row address strobe. Active low.
$\overline{\text{MEM\_CAS}}$	D9	O2	MEM_CLK	Column address strobe. Active low.
MEM_CKE	E9	O2	MEM_CLK	Clock enable. Active high.
$\overline{\text{MEM\_CS}}$	B10	O2	MEM_CLK	Chip select. Active low.
MEM_HDQM	A10	O2	MEM_CLK	Data mask high byte.
MEM_LDQM	D8	O2	MEM_CLK	Data mask low byte
$\overline{\text{MEM\_WE}}$	F8	O2	MEM_CLK	Write enable. Active low.
MEM_CLK	F9	O2	N/A	Memory clock. Generated by internal PLL. 100 MHz
MEM_DQ0	A3	B3	MEM_CLK	Bidirectional data 0 for the SDRAM
MEM_DQ1	B4	B3	MEM_CLK	Bidirectional data 1 for the SDRAM
MEM_DQ2	A5	B3	MEM_CLK	Bidirectional data 2 for the SDRAM
MEM_DQ3	A6	B3	MEM_CLK	Bidirectional data 3 for the SDRAM
MEM_DQ4	B6	B3	MEM_CLK	Bidirectional data 4 for the SDRAM
MEM_DQ5	E6	B3	MEM_CLK	Bidirectional data 5 for the SDRAM
MEM_DQ6	A7	B3	MEM_CLK	Bidirectional data 6 for the SDRAM
MEM_DQ7	C8	B3	MEM_CLK	Bidirectional data 7 for the SDRAM
MEM_DQ8	E8	B3	MEM_CLK	Bidirectional data 8 for the SDRAM

TERMINAL FUNCTIONS (continued)

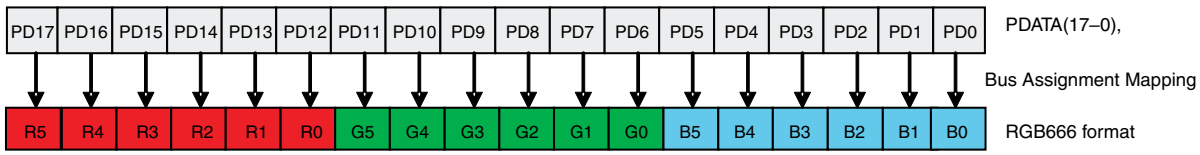
TERMINAL		I/O TYPE	CLOCK SYSTEM	DESCRIPTION
NAME	NO.			
MEM_DQ9	B7	B3	MEM_CLK	Bidirectional data 9 for the SDRAM
MEM_DQ10	E7	B3	MEM_CLK	Bidirectional data 10 for the SDRAM
MEM_DQ11	A2	B3	MEM_CLK	Bidirectional data 11 for the SDRAM
MEM_DQ12	D6	B3	MEM_CLK	Bidirectional data 12 for the SDRAM
MEM_DQ13	B5	B3	MEM_CLK	Bidirectional data 13 for the SDRAM
MEM_DQ14	D5	B3	MEM_CLK	Bidirectional data 14 for the SDRAM
MEM_DQ15	A4	B3	MEM_CLK	Bidirectional data 15 for the SDRAM
LED Driver Interface				
BLU_PWM	C6	O3	CLK_IN	Blue LED PWM signal used to control the LED current
RED_PWM	C3	O3	CLK_IN	Red LED PWM signal used to control the LED current
GRN_PWM	D3	O3	CLK_IN	Green LED PWM signal used to control the LED current
BLU_STROBE	F1	O1	CLK_IN	Blue LED enable
RED_STROBE	G2	O1	CLK_IN	Red LED enable
GRN_STROBE	F2	O1	CLK_IN	Green LED enable
$\overline{\text{LED\_FAULT}}$	A8	I4	Async	LED fault indication. Signal forces LEDDRV_ON low and RGB strobes low
LED_ENABLE	T8	I5	Async	LED enable. Signal forces LEDDRV_ON low and RGB strobes low.
LEDDRV_ON	F3	O1	CLK_IN	LED driver enable
RESERVED	B1	I1	Async	Not used. Reserved for future use.
RESERVED	C2	O1	Async	Not used. Reserved for future use.
Impedance Control(2)				
RUP2		PWR	N/A	Bank 4 control
RDN2		PWR	N/A	Bank 4 control
RUP3		PWR	N/A	Bank 5 control
RDN3		PWR	N/A	Bank 5 control
RUP4		PWR	N/A	Bank 7 control
RDN4		PWR	N/A	Bank 7 control
Power and Ground(2)				
P1P2V		PWR	N/A	1.2 V core power
P2P5V_DPLL		PWR	N/A	2.5 V filtered power for internal PLL
P1P8V		PWR	N/A	1.8 V I/O power
P2P5V		PWR	N/A	2.5 V I/O power
P3P3V		PWR	N/A	3.3 V I/O power
GND		PWR	N/A	Common digital ground
GNDA		PWR	N/A	Common PLL ground

(2) To see how these are connected, see the reference schematic

16-Bit Input Bus, RGB565 (Parallel Bus)



18-Bit Input Bus, RGB666 (Parallel Bus)



24-Bit Input Bus, RGB888 (Parallel Bus Only)

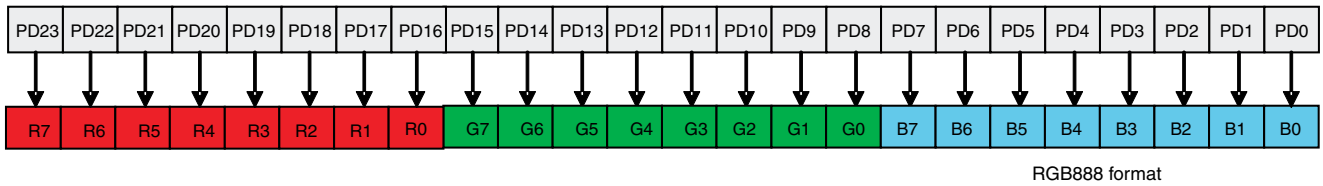


Figure 3. Pixel Mapping

I/O CHARACTERISTICS(1)

all inputs/outputs are LVCMOS

I/O TYPE		CONDITIONS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I1	Input	V_{CCIO} = 2.5 V	-0.3	0.8	1.7	V_{CCIO}+0.3			V
I2	Input	V_{CCIO} = 2.5 V	-0.3	0.8	1.7	V_{CCIO}+0.3			V
I3	Input	V_{CCIO} = 2.5 V, internal pulldown resistor	-0.3	0.8	1.7	V_{CCIO}+0.3			V
I4	Input	V_{CCIO} = 1.8 V	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO}+0.3			V
I5	Input	V_{CCIO} = 1.8 to 3.3 V	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO}+0.3			V
I6	Input	V_{CCIO} = 1.8 to 3.3 V, internal pullup resistor	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO}+0.3			V
O1	Output 8 mA	V_{CCIO} = 2.5 V					0.4	2	V
O2	Output 4 mA	V_{CCIO} = 1.8 V					0.45	V_{CCIO} – 0.45	V
O3	Output 8 mA	V_{CCIO} = 1.8 V					0.45	V_{CCIO} – 0.45	V
O4	Output 4 mA	V_{CCIO} = 1.8 to 3.3 V					0.45	V_{CCIO} – 0.45	V
B1	Bi-directional output, open drain	V_{CCIO} = 2.5 V	-0.3	0.8	1.7	V_{CCIO}+0.3	0.4		V
B2	Bi-directional output, open drain	V_{CCIO} = 1.8 to 3.3 V	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO}+0.3	0.45		V
B3	Bi-directional output, 4 mA	V_{CCIO} = 1.8 V	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO}+0.3	0.45	V_{CCIO} – 0.45	V

(1) Cross reference to IO assignments

POWER AND GROUND PINS

NAME	DESCRIPTION	PIN NUMBER(S)
Input Power and Ground Pins		
VCC12	1.2-V power supply for core logic	F7, F11, G6, G7, G8, G9, G10, H6, H11, J6, J12, K7, K9, K10, K11, L6, M9, M11
VCC25_DPLL	2.5-V power supply for internal PLLs	F5, F12, L5, L12
VCCIO18	1.8-V power supply for I/Os on banks 4-8	A1, A16, C4, C7, C10, C13, E14, G14, K14, M14, P10, P13, T16
FLASHPWR	2.5-V or 3.3-V power supply for bank I/Os (Serial configuration FLASH interface) Bank 1	E3, G3
INTFPWR	1.8V, 2.5V or 3.3V power supply for I/Os on Video Interface Banks 2-3	K3, M3, P4, P7, T1
VCCD_PLL1-4	1.2V power supply for DLL	N4, D13, D4, N13
GND	Common ground	B2, B15, C5, C12, D7, D10, E4, E13, F6, F10, G4, G11, G13, H7, H8, H9, H10, J7, J8, J9, J10, J11, K4, K6, K8, K12, K13, L9, L10, L11, M4, M13, N7, N10, P5, P12, R2, R15
GNDA1-4	Analog ground	M5, E12, E5, M12
Input Signals Tied to a Fixed Level		
GND	Virtual GND output pins that are driven to a low level for noise reduction.	none
On-Chip Series Termination with Calibration(1)		
RDN1, RUP1	Bank 2 - Not connected	L4, K5
RDN2, RUP2	Bank 4 DMD interface support	N11, M10
RDN3, RUP3	Bank 5 DMD interface support	P15, N14
RDN4, RUP4	Bank 7 and 8 memory interface support	E10, E11

(1) The device supports on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the I/O buffer to the external 50 Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match. OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in bank 2, 4, 5, and 7.

Video Input Pixel Interface

TIMING REQUIREMENTS(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	30	MHz
t_t	Transition time, $t_t = t_f/t_r$ PCLK	20% to 80% reference points (signal)	1.0		ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	11		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	11		ns
t_j	Clock period jitter, PCLK	See (2)			ns
t_{su}	Setup time, PDATA(23-0) valid before PCLK	See (3)	3.0		ns
t_h	Hold time, PDATA(23-0) valid after PWCLK	See (3)	3.0		ns
t_{su}	Setup time, VSYNC_WE valid before PCLK	See (3)	3.0		ns
t_h	Hold time, VSYNC_WE valid after PCLK	See (3)	3.0		ns
t_{su}	Setup time, HSYNC_CS valid before PCLK	See (3)	3.0		ns
t_h	Hold time, HSYNC_CS valid after PCLK	See (3)	3.0		ns
t_{su}	Setup time, DATEN_CMD valid before PCLK	See (3)	3.0		ns
t_h	Hold time, DATEN,_CMD valid after PCLK	See (3)	3.0		ns

(1) Contact TI for I²C, LED driver, power-up and power=down timing information.
(2) PCLK may be inverted from that shown in Figure 4. In that case the same specifications in the table are valid except now referenced to the falling edge of the clock. If the falling edge of PCLK is to be used, an I²C command is needed to tell the DLPC100 to use the falling edge of PCLK.
(3) Use the following formula to obtain the jitter. Jitter = [1/frequency – 30 ns]. Setup and hold must still be met.

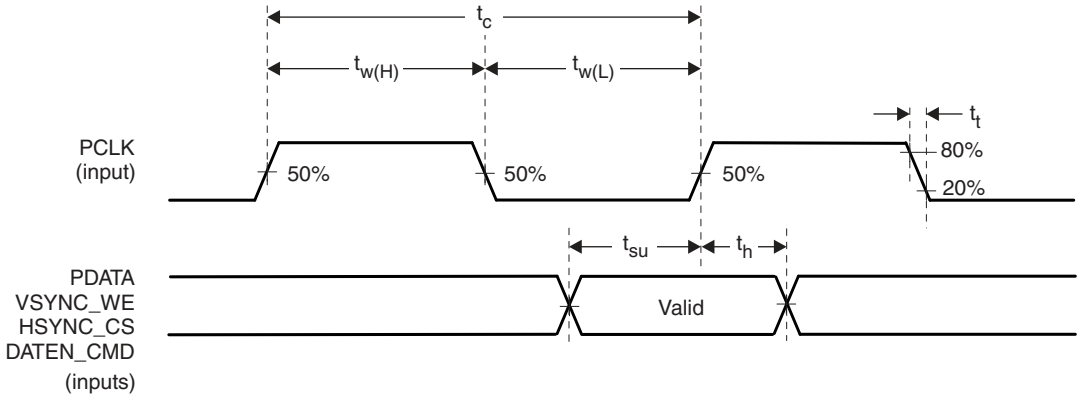


Figure 4. Input Port Interface

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 5). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 6).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 5).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

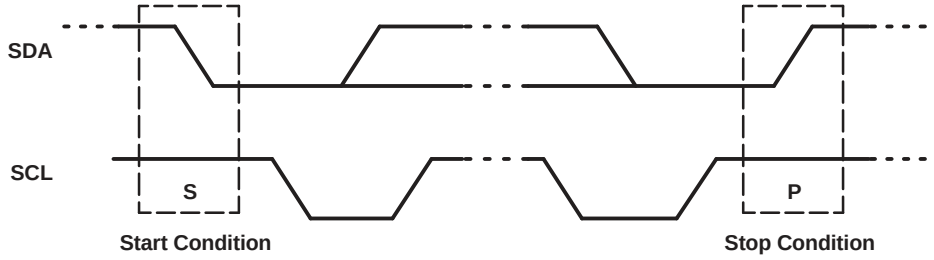


Figure 5. Definition of Start and Stop Conditions

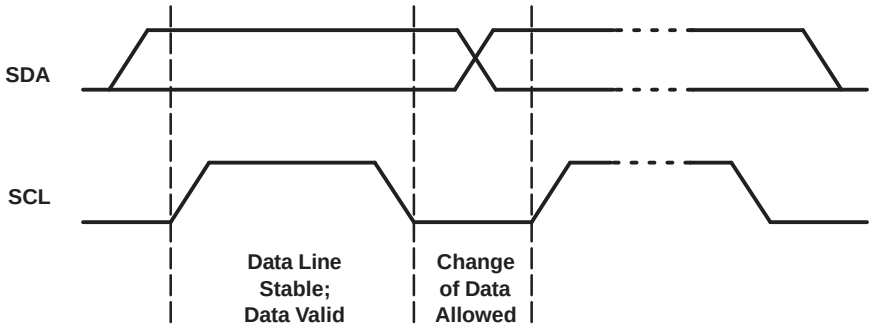


Figure 6. Bit Transfer

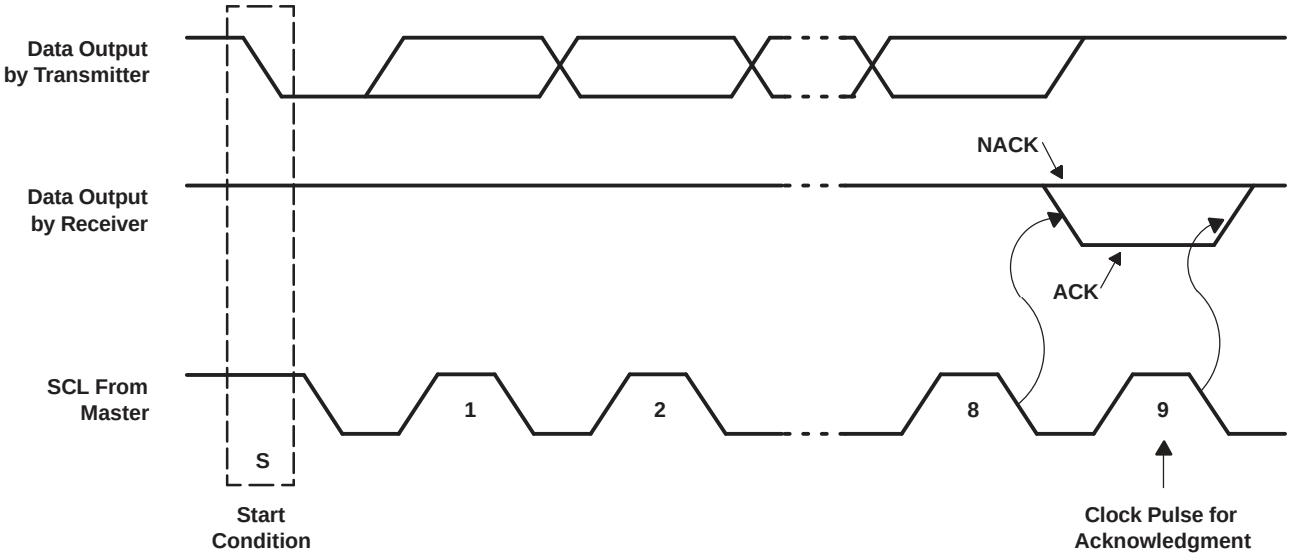
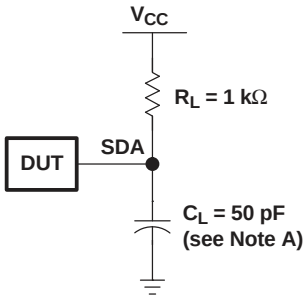


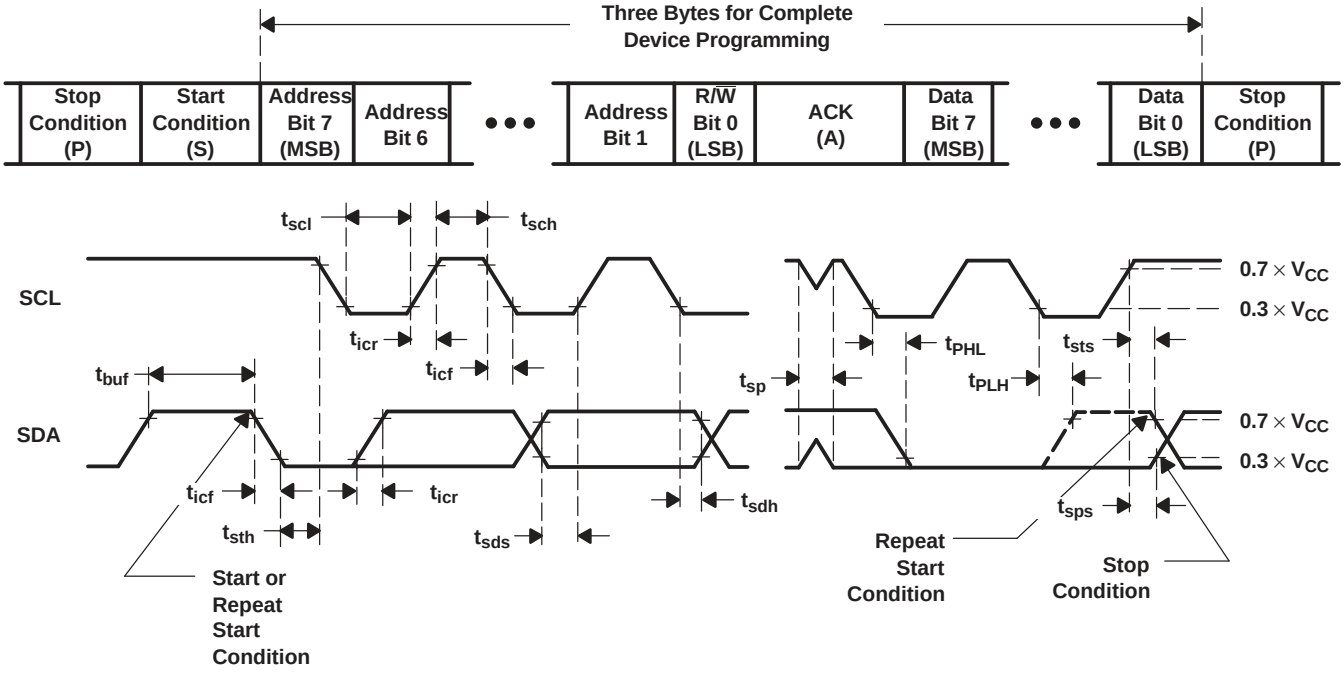
Figure 7. Acknowledgment on I^2C Bus

I²C INTERFACE TIMING REQUIREMENTS

PARAMETER			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		1		ms
t_{scl}	I²C clock low time		1		ms
t_{sp}	I²C spike time			20	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		100		ns
t_{icr}	I²C input rise time		20	300	ns
t_{ocf}	I²C output fall time	50 pF	30	200	ns
t_{buf}	I²C bus free time between Stop and Start conditions		1.3		ms
t_{sts}	I²C Start or repeated Start condition setup		1		ms
t_{sth}	I²C Start or repeated Start condition hold		1		ms
t_{sph}	I²C Stop condition setup		1		ms
t_{vd}	Valid-data time	SCL low to SDA output valid		1	ms
	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	ms
t_{sph}	I²C bus capacitive load		0	100	pF



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 8. I^2C Interface Load Circuit and Voltage Waveforms

I²C Bus Transactions

Data is exchanged between the master and the DLPC100 through write and read commands.

Writes

Data is transmitted to the DLPC100 by sending the device address and setting the least-significant bit to a logic 0. The data bytes are sent after the address and determines which register receives the data that follows the address byte. Data is clocked into the register on the rising edge of the ACK clock pulse. .

Reads

The bus master first must send the DLPC100 address with the least-significant bit set to a logic 0. The read address byte is sent after the device address and read command (x15) and the read address determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the read address byte then is sent by the DLPC100. See Programmers guide for a full description of the register read/write protocol and available registers.

Flash Memory Interface

The DLPC100 controller flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal).

FLASH INTERFACE TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	See (1)	33.3266	33.34	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	29.994	30.006	ns
t_{p_clkjit}	Clock jitter, SPI_CLK	Max f_{clock}		200	ps
t_{p_wh}	Pulse width low, SPI_CLK	50% reference points	10		ns
t_{p_wl}	Pulse width high, SPI_CLK	50% reference points	10		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns
t_{p_su}	Setup Time – SPI_DIN valid before SPI_CLK rising edge	50% reference points	10		ns
t_{p_h}	Hold Time – SPI_DIN valid after SPI_CLK rising edge	50% reference points	0		ns
t_{p_clqv}	SPI_CLK clock low to output valid time – SPI_DOUT & SPI_CSZ	50% reference points		1	ns
t_{p_clqx}	SPI_CLK clock low output hold time – SPI_DOUT & SPI_CSZ	50% reference points	-1		ns

(1) This range include the 200 ppm of the external oscillator

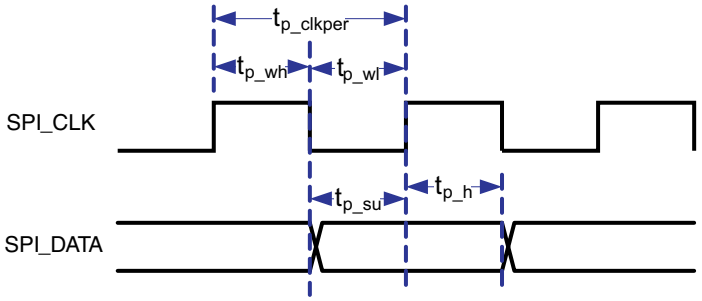


Figure 9. Flash Memory Interface Timing

DMD Interface

The DLPC100 ASIC DMD interface consists of a 60.0 MHz (nominal) DDR output-only interface with LVCMOS signaling.

DMD INTERFACE TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK & DMD_SAC_CLK	See (1)		60.05	MHz
t_{p_clkper}	Clock period, DMD_DCLK & DMD_SAC_CLK	50% reference points	16.5		ns
t_{p_clkjit}	Clock jitter, DMD_DCLK & DMD_SAC_CLK	Max f_{clock}		200	ps
t_{p_wh}	Pulse width low, DMD_DCLK & DMD_SAC_CLK	50% reference points	7.5		ns
t_{p_wl}	Pulse width high, DMD_DCLK & DMD_SAC_CLK	50% reference points	7.5		ns
t_t	Transition time – all signals	20% to 80% reference points	0.3	2.0	ns
tp_su	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB & DMD_TRC relative to both rising and falling edges of DMD_DCLK	50% reference points		1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB & DMD_TRC signals relative to both rising and falling edges of DMD_DCLK DMD	50% reference points		1.5	ns
$t_{p\_d1\_skew}$	Data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB & DMD_TRC signals relative to each other	50% reference points		0.20	ns
$t_{p\_clk\_skew}$	Clock skew – DMD_DCLK & DMD_SAC_CLK relative to each other DAD/ SAC	50% reference points		0.20	ns
$t_{p\_d2\_skew}$	Data Skew - DMD_SAC_BUS, DMD_DAD_OEZ, DMD_DAD_BUS & DMD_DAD_STRB signals relative to DMD_SAC_CLK	50% reference points		0.20	ns

(1) This range include the 200 ppm of the external oscillator

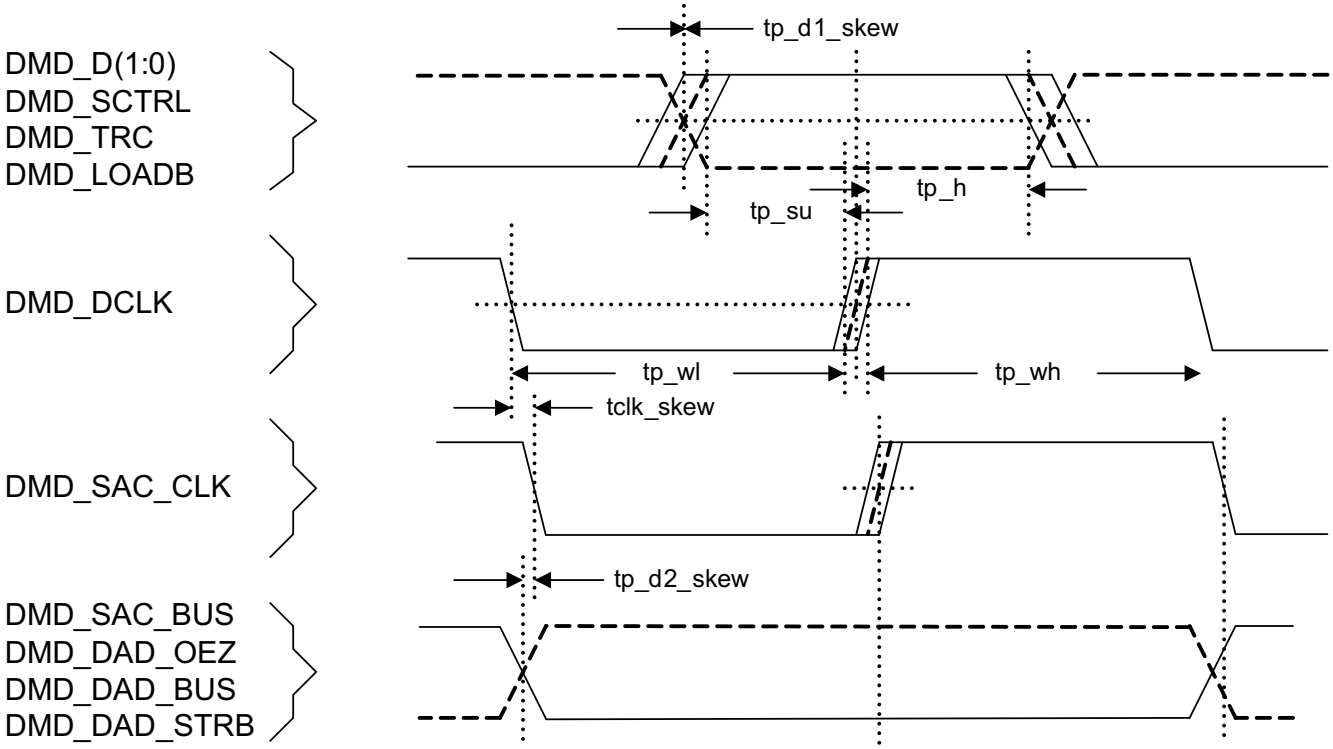


Figure 10. DMD I/F Timing

Mobile SDR Memory Interface

The DLPC100 Controller Mobile SDR Memory interface consists of a 16-bit wide, mobile SDR interface (i.e. LVCMOS signaling) operated at 100.0 MHz (nominal).

MOBILE SDR MEMORY INTERFACE TIMING REQUIREMENTS

PARAMETER		MIN	MAX	UNIT
t_{CYCLE}	Cycle time reference	10		ns
t_{CH}	CK high pulse width(1)	3		ns
t_{CL}	CK low pulse width(1)	3		ns
t_{CMS}	Command setup	1.5		ns
t_{CMH}	Command hold	1		ns
t_{AS}	Address setup	1.5		ns
t_{AH}	Address hold	1		ns
t_{DS}	Write data setup	2.5		ns
t_{DH}	Write data hold	1		ns
t_{AC}	Read data access time		8	ns
t_{OH}	Read data hold time	2.5		ns
t_{LZ}	Read data low impedance time	1		ns
t_{HZ}	Read data high impedance time		8	ns

(1) CK and DQS pulse width specs for the DLPC100 assume it is interfacing to a 125 MHz m_{DDR} device. Even though these memories are only operated at 100.0 MHz, according to memory vendors, the rated t_{CK} spec (i.e. 8 ns) can be applied to determine minimum CK and DQS pulse width requirements to the memory.

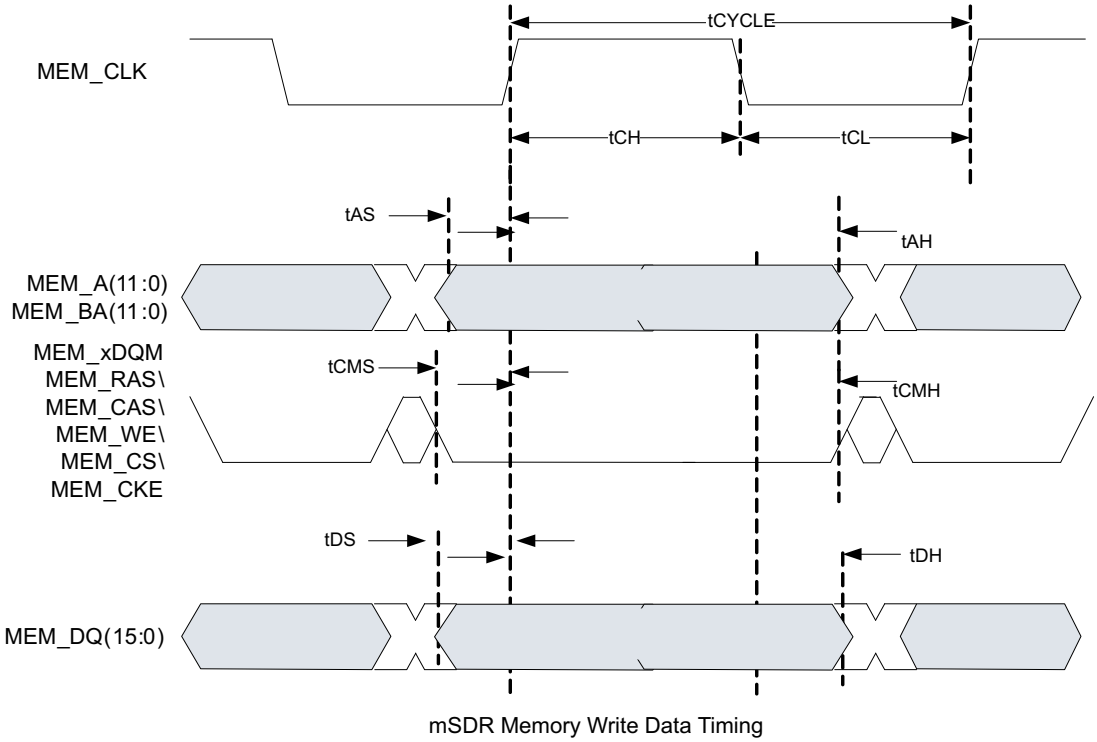
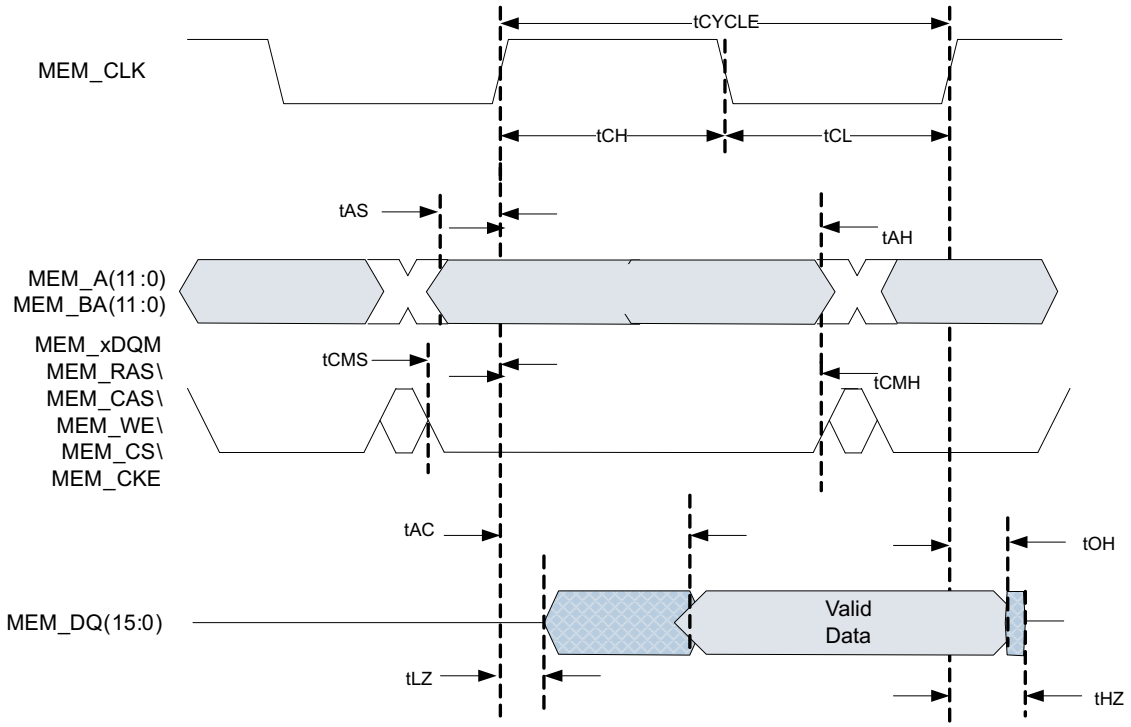


Figure 11. Mobile SDR Memory I/F Write Timing



mSDR Memory Read Data Timing

Figure 12. Mobile SDR Memory I/F Read Timing

SDRAM Memory

The DLPC100 requires an external Mobile SDR SDRAM. The DLPC100 can support either a 128 Mbit or a 64 Mbit SDRAM. The basic requirements for the SDRAM are:

- SDRAM type: mobile SDR
- Speed: 125 MHz minimum
- 16-bit interface size: 64 Mbit or 128 Mbit
- Supply voltage: 1.8 V

Supported SDRAM Devices shows the SDRAM parts that have been tested by TI. All have been found to work properly and are therefore recommended for production use with the DLPC100.

Table 1. Supported SDRAM Devices

PART NUMBER	MANUFACTURER	SIZE
K4M64163PK-BG750JR	Samsung	64 Mbit
K4M28163PH-BG750JR	Samsung	128 Mbit
MT48H4M16LFB4-8	Micron	64 Mbit
MT48H8M16LFB4-8	Micron	128 Mbit

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	VALUE	UNIT
V_{CC12}	Supply voltage range (2)		–0.5 V to 1.80	V
V_{CCIO18}			–0.5 V to 3.90	
V_{CCA25_DPLL}			–0.5 V to 3.75	
INTFPWR			–0.5 V to 3.90	
V_{CCD_PLL1-4}			-0.5 V to 1.80	
V_I	Input voltage range(3)	1.8 V, 2.5V, 3.3V	–0.5 V to 3.95	V
	Continuous total power dissipation: typical		0.300	W
T_J	Operating junction temperature range		–40°C to 125	°C
T_{stg}	Storage temperature range		–60°C to 150	°C
HBM	Electrostatic discharge voltage using the Human Body Model		+/- 2000	V
CD	Electrostatic discharge voltage using the Charged Device Model		+/- 500	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, and at the device not at the power supply.
(3) Applies to external input and bidirectional buffers.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

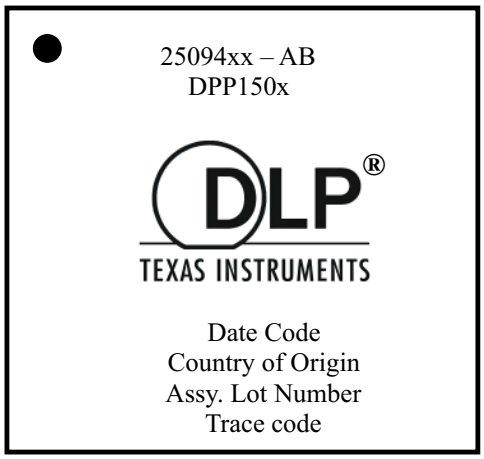
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC12}	1.2-V Supply voltage, core logic		1.15	1.2	1.25	V
V_{CC18}	1.5-V supply voltage, HSTL output buffers		1.71	1.8	1.89	V
V_{CCA25_DPLL}	2.5-V analog voltage for PLL regulator		2.375	2.5	2.625	V
INTFPWR	At 1.8-V IO rail		1.71	1.8	1.89	V
INTFPWR	At 2.5-V IO rail		2.375	2.5	2.625	V
INTFPWR	At 3.3-V IO rail		3.15	3.3	3.45	V
V_{CCD_PLL1-4}	1.2-V supply voltage, for PLL		1.15	1.2	1.25	V
V_{IH}	High-level input voltage	1.8V LVCMOS	$0.65*V_{CCIO}$			V
		2.5V LVCMOS	1.7			
		3.3VLVCMOS	1.7			
V_{IL}	Low-level input voltage	1.8V LVCMOS			$0.35*V_{CCIO}$	V
		2.5V LVCMOS			0.8	
		3.3VLVCMOS			0.8	
V_I	Input voltage		-0.5		3.6	V
V_O	Output voltage		0		VCCIO	V
t_{Ramp}	Power supply ramptime		50 us		3 ms	-
T_J	Operating junction temperature		-20		85	°C

Thermal Considerations

The underlying thermal limitation for the DLPC100 is that the maximum operating junction temperature (T_J) not be exceeded (see Recommended Operating Conditions). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC100 and power dissipation of surrounding components. The DLPC100’s package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Device Marking

Device marking should be as shown below.



25094xx = 2509408 or 2509427; DPP150x = DPP1500 or DPP1505

Marking Key:

Line 1 : TI Reference Number

Line 2 : Device Name

Line 3 : DLP® logo

Line 4 : Date Code

Line 5 : Country of Origin

Line 6 : Assembly Lot Number

Line 7 : Trace Code

Table 2. Revision History

REVISION	SECTION(S)	COMMENT
*	All	Initial release
A	I^2C Interface, I^2C Bus Transactions, Flash Memory Interface, DMD Interface, Mobile SDR Memory Interface,	Added description, graphics, and timing requirements, status changed to Production Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC100ZCT	LIFEBUY	NFBGA	ZCT	256		TBD	Call TI	Call TI	-20 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

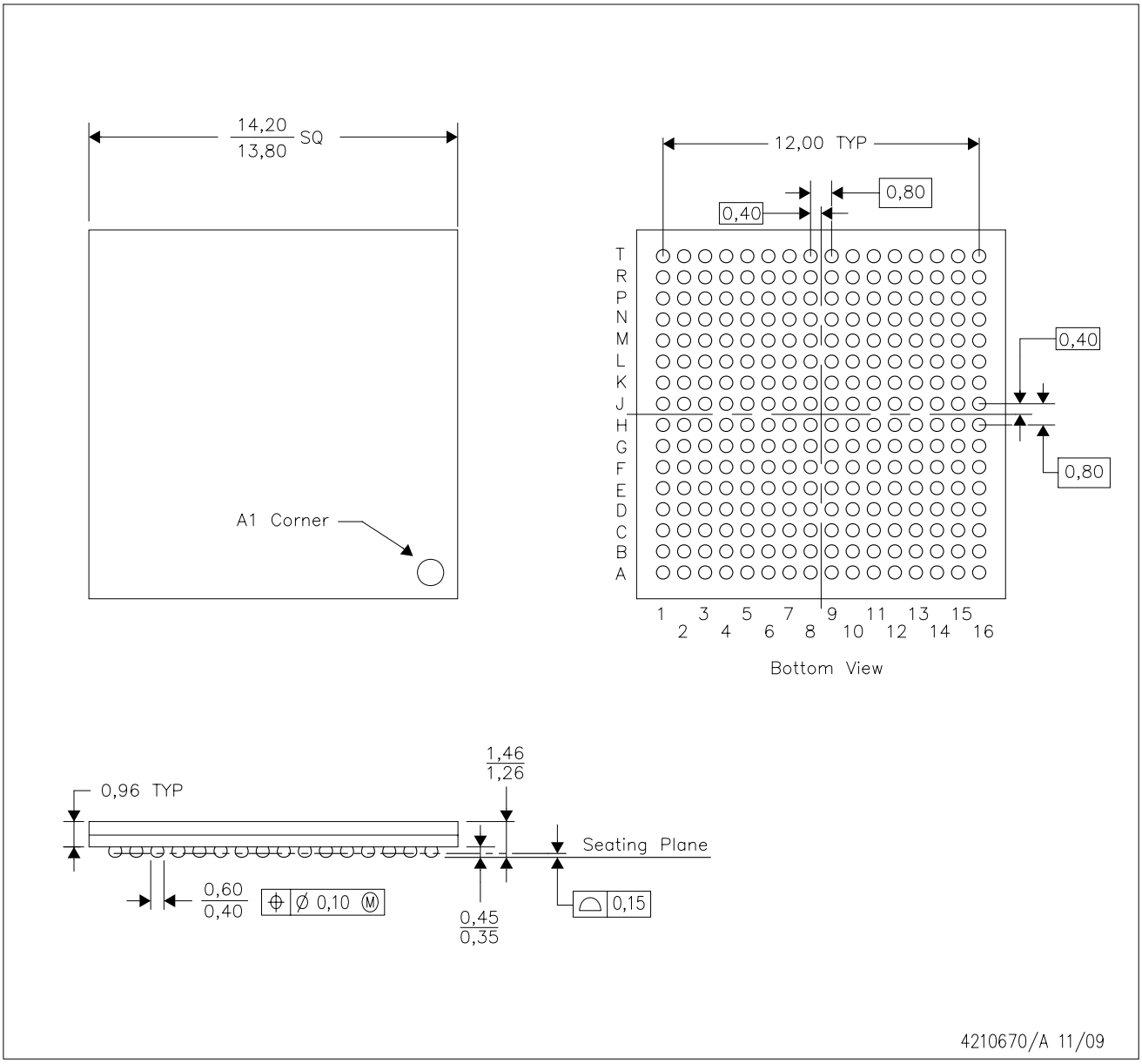
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZCT (S–PBGA–N256) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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