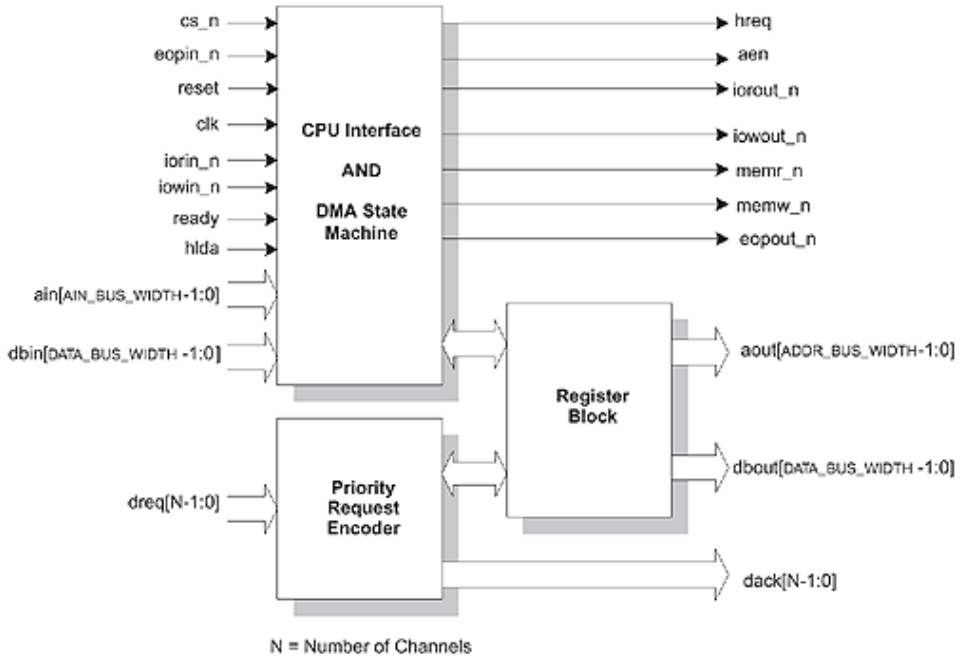
Multi-channel DMA Controller

Overview

The Multi-Channel Direct Memory Access (MCDMA) Controller is designed to improve microprocessor system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also supported.

The MCDMA Controller core supports two modes: 8237 and non-8237. When the 8237 mode is selected, it configures the core to be compatible with the Intel 8237A DMA Controller with a few variations. These variations are listed in the "Compatibility Differences with the 8237 Intel Device" section of the datasheet. The 8237 mode supports four independent channels while the non-8237 mode supports up to 16 independent channels.



Features

- Selectable 8237 Mode
- Configurable up to 16 Independent DMA Channels for Non-8237 Mode
- Configurable Data Width of 8, 16, 32 or 64 Bits for Non-8237 Mode
- Configurable Address Width of 16, 24 or 32 Bits for Non-8237 Mode
- Configurable Word Count Register Width for Non-8237 Mode
- Independent Auto-initialization of All Channels
- Memory-to-Memory Transfers on Single, Block, and Demand Transfer Modes
- Memory Block Initialization
- Software DMA Requests

Evaluation Configurations

Evaluation Configurations Available for Series 4 ORCA FPGAs and FPSCs[1]

Name of Parameter File	dma_mc_o4_2_001.lpc	dma_mc_o4_2_002.lpc

Mode	8237	Non-8237
LUTs	1258	2661
ORCA4 PFUs[2]	200	499
Registers	524	1187
SysMem EBR	N/A	N/A
External Pins	59	125
fMAX (MHz)	58	66
# of Channels	4	4
Data Bus Width	8	32
Address Bus Width	16	32
Word Count Width	16	16

[1] Performance and utilization characteristics are generated using OR4E02-2PBGAM680-DE in Lattice's ispLEVER™ v3.0 SP1 software. Synthesized using Synplicity Synplify v.7.03. When using this IP core in a different density, package, speed, or grade within the ORCA family, performance may vary slightly.

[2] PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.

Please contact your local Lattice sales office to obtain other evaluation configurations.

Evaluation Configurations Available for ispXPGA[1]

Name of Parameter File	dma_mc_xp_2_001.lpc	dma_mc_xp_2_002.lpc
Mode	8237	Non-8237
LUT4[2]	1450	3487
ispXPGA PFUs[2]	432	1072
Registers	562	1181
SysMem EBRs	N/A	N/A
External Pins	58	124
fMAX (MHz)	58	66
# of Channels	4	4
Data Bus Width	8	32
Address Bus Width	16	32
Word Count Width	16	16

[1] Performance and utilization characteristics are generated using LFX1200B-05F900C in Lattice's ispLEVER™ v3.0 software. Synthesized using Synplicity Synplify v.7.03. When using this IP core in a different density, package, speed, or grade within the ispXPGA family, performance may vary slightly.

[2] PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.

Please contact your local Lattice sales office to obtain dma_mc_xp_2_002 and other evaluation configurations.

Evaluation Configurations Available for LatticeECP and LatticeEC[1]

Name of Parameter File	dma_mc_e2_3_001.lpc	dma_mc_e2_3_002.lpc
Mode	8237	Non-8237
SLICEs	710	1633
LUTs	1087	2249
sysMEM EBRs	0	0
Registers	551	1181
I/O	59	125
fMAX (MHz)	72	86
# of Channels	4	4
Data Bus Width	8	32
Address Bus Width	16	32
Word Count Width	16	16

[1] Performance and utilization characteristics are generated using LFEC20E-4F672C in Lattice ispLEVER v.4.1 software. When using this IP core in a different density, package, or speed grade, performance may vary.

Evaluation Configurations Available for LatticeXP[1]

Name of Parameter File	dma_mc_xm_3_001.lpc	dma_mc_xm_3_002.lpc
Mode	8237	Non-8237
SLICEs	746	1794
LUTs	1287	3084
sysMEM EBRs	0	0
Registers	555	1179
I/O	59	125
fMAX (MHz)	71	80
# of Channels	4	4
Data Bus Width	8	32
Address Bus Width	16	32
Word Count Width	16	16

[1] Performance and utilization characteristics are generated using LFXP10E-4F388C in Lattice ispLEVER 5.0 software. When using this IP core in a different density, package, or speed grade, performance may vary.

Evaluation Configurations Available for LatticeSC[1]

Name of Parameter File	dma_mc_sc_3_001.lpc	dma_mc_sc_3_002.lpc
Mode	8237	Non-8237

SLICEs	717	1744
LUTs	1249	2864
sysMEM EBRs	0	0
Registers	534	1179
I/O	59	125
fMAX (MHz)	>100	>100
# of Channels	4	4
Data Bus Width	8	32
Address Bus Width	16	32
Word Count Width	16	16

[1] Performance and utilization characteristics are generated using LFSC3G!25E-5F900Cin Lattice ispLEVER 5.1 SP2 software. When using this IP core in a different density, package, or speed grade, performance may vary.

Ordering Information

Part Numbers:

For ORCA 4: DMA-MC-O4-N2

For ispXPGA: DMA-MC-XP-N2

For LatticeECP/EC: DMA-MC-E2-N3

For LatticeXP: DMA-MC-XM-N3

For LatticeSC: DMA-MC-SC-N3

To find out how to purchase the Multi-channel DMA Controller IP Core, please contact your local Lattice Sales Office.