Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

MPXV4006G

INTEGRATED PRESSURE SENSOR
0 to 6 kPa (0 to 0.87 psi)
0.2 to 4.7 V OUTPUT

The MPXV4006G series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This sensor combines a highly sensitive implanted strain gauge with advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

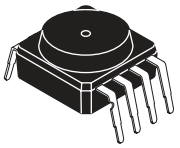
Features

- Temperature Compensated over 10° to 60°C
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Available in Gauge Surface Mount (SMT) or Through-hole (DIP) Configurations
- Durable Thermoplastic (PPS) Package

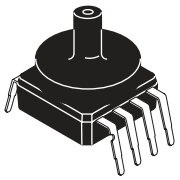
MPXV4006G series pressure sensors are available in the basic element package or with pressure ports. Two packing options are offered for the 482 and 482A case configurations.

ORDERING INFORMATION					
Device Type	**Options**	**Case No.**	**MPX Series Order No.**	**Packing Options**	**Marking**
Basic Element	Element Only	482	MPXV4006G6U	Rails	MPXV4006G
	Element Only	482	MPXV4006G6T1	Tape & Reel	MPXV4006G
	Element Only	482B	MPXV4006G7U	Rails	MPXV4006G
Ported Element	Axial Port	482A	MPXV4006GC6U	Rails	MPXV4006G
	Axial Port	482A	MPXV4006GC6T1	Tape & Reel	MPXV4006G
	Axial Port	482C	MPXV4006GC7U	Rails	MPXV4006G
	Side Port	1369	MPXV4006GP	Trays	MPXV4006G
	Dual Port	1351	MPXV4006DP	Trays	MPXV4006G

SMALL OUTLINE PACKAGE THROUGH-HOLE

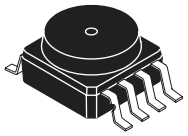


MPXV4006G7U
CASE 482B-03

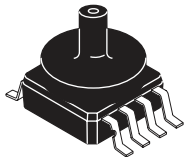


MPXV4006GC7U
CASE 482C-03

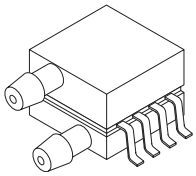
SMALL OUTLINE PACKAGE SURFACE MOUNT



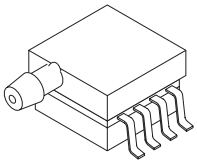
MPXV4006G6U/6T1
CASE 482-01



MPXV4006GC6U/C6T1
CASE 482A-01



MPXV4006DP
CASE 1351-01



MPXV4006GP
CASE 1369-01

PIN NUMBERS[1]			
1	N/C	5	N/C
2	V_S	6	N/C
3	Gnd	7	N/C
4	V_{out}	8	N/C

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch i n the lead.

freescale semiconductor

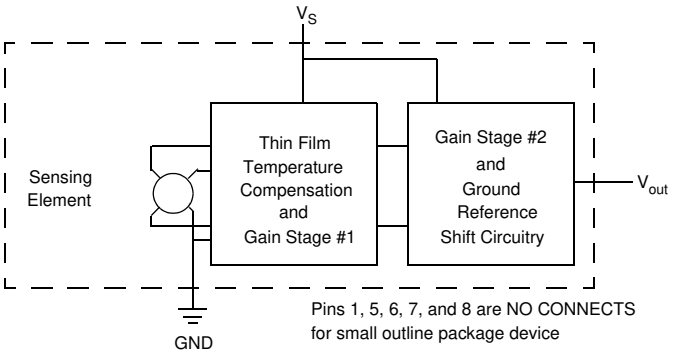


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings(1)

Parametrics	Symbol	Value	Units
Maximum Pressure (P1 >P2)	P_{max}	24	kPa
Storage Temperature	T_{stg}	-30° to +100°	°C
Operating Temperature	T_A	-10° to +60°	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics

Characteristic		Symbol	Min	Typ	Max	Unit
Pressure Range		P_{OP}	0	—	6.0	kPa
Supply Voltage(1)		V_S	4.75	5.0	5.25	Vdc
Supply Current		I_S	—	—	10	mAdc
Full Scale Output(2)	(RF = 51kΩ)	V_{FSS}	—	4.6	—	V
Offset(3)(5)	(RF = 51kΩ)	V_{off}	0.100	0.225	0.430	V
Sensitivity		V/P	—	766	—	mV/kPa
Accuracy(4)(5)	(10 to 60°C)	—	—	—	±5.0	$\%V_{FSS}$

1. Device is ratiometric within this specified excitation range.
2. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
3. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
4. Accuracy (error budget) consists of the following:
   - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
   - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
   - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or maximum rated pressure, at 25°C.
   - Offset Stability: Output deviation, after 1000 temperature cycles, -30 to 100°C, and 1.5 million pressure cycles, with minimum rated pressure applied.
   - TcSpan: Output deviation over the temperature range of 10° to 60°C, relative to 25°C.
   - TcOffset: Output deviation with minimum pressure applied, over the temperature range of 10° to 60°C, relative to 25°C.
5. Auto Zero at Factory Installation: Due to the sensitivity of the MPXV4006G, external mechanical stresses and mounting position can affect the zero pressure output reading. To obtain the 5% FSS accuracy, the device output must be “autozeroed" after installation. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION, AND SIGNAL CONDITIONING

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPXV4006G series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and qualification test for dry air, and other media, are available from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

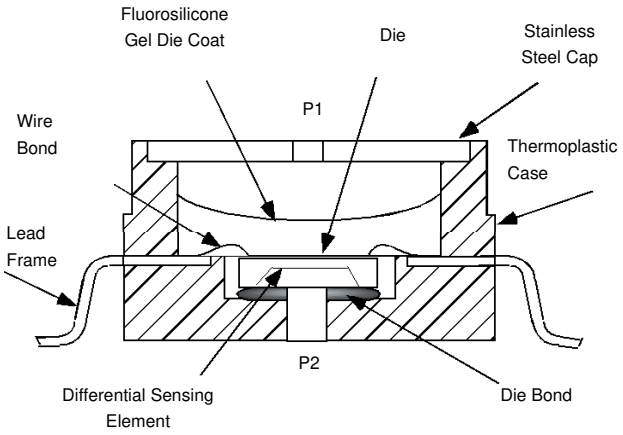


Figure 2. Cross Sectional Diagram SOP (Not to Scale)

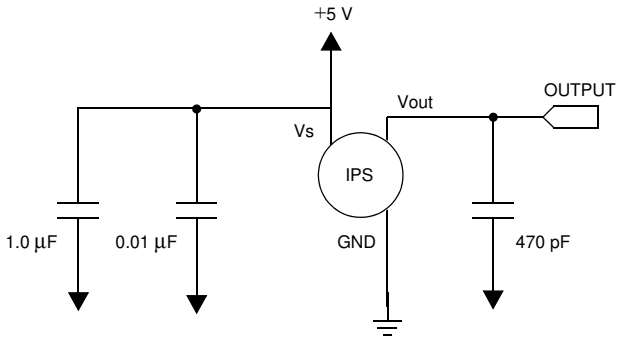


Figure 3. Recommended Power Supply Decoupling and Output Filtering Recommendations
(For additional output filtering, please refer to Application Note AN1646.)

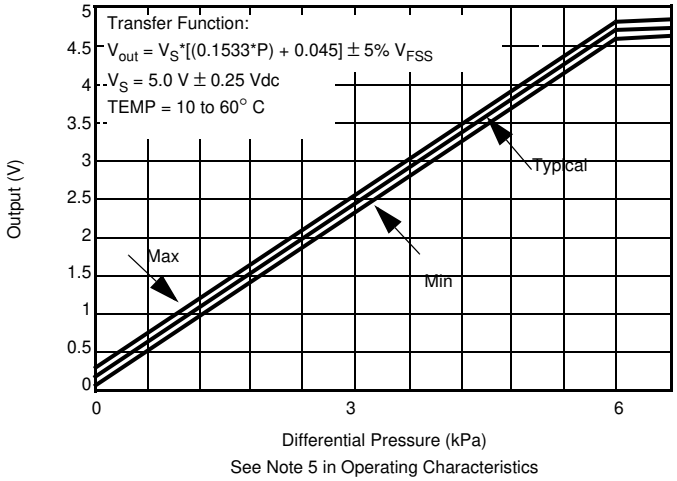


Figure 4. Output versus Pressure Differential

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing silicone gel which isolates the die from the environment. The pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below:

Table 3. Pressure (P1)/Vacuum (P2) Side Identification Table

Part Number	Case Type	Pressure (P1) Side Identifier
MPXV4006G6U/T1	482	Stainless Steel Cap
MPXV4006GC6U/T1	482A	Side with Port Attached
MPXV4006G7U	482B	Stainless Steel Cap
MPXV4006GC7U	482C	Side with Port Attached
MPXV4006GP	1369	Side with Port Attached
MPXV4006DP	1351	Side with Part Marking

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

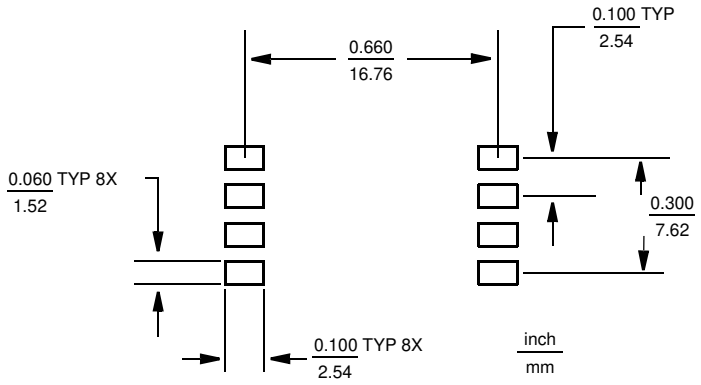
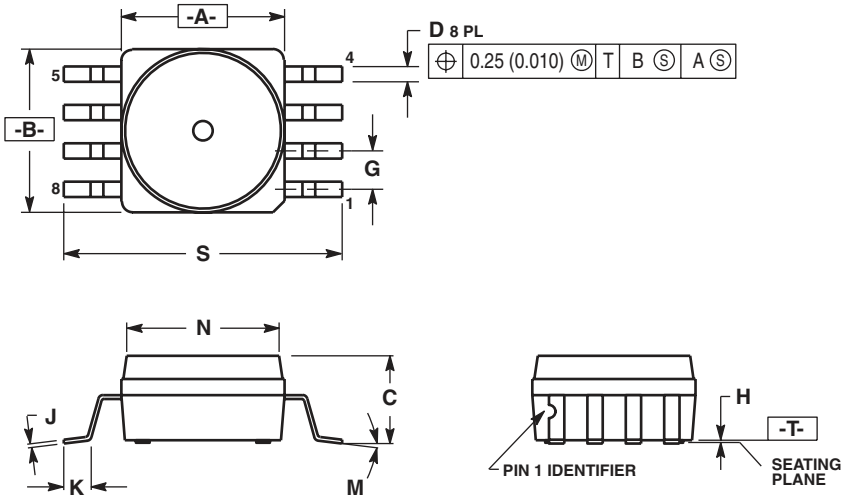


Figure 5. SOP Footprint (Case 482)

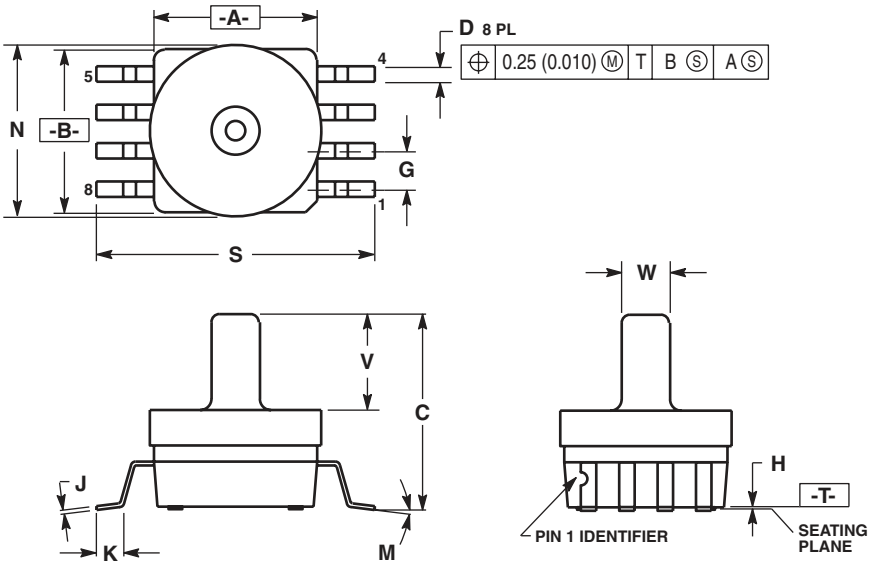
PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41

CASE 482-01
ISSUE O
SMALL OUTLINE PACKAGE
SURFACE MOUNT

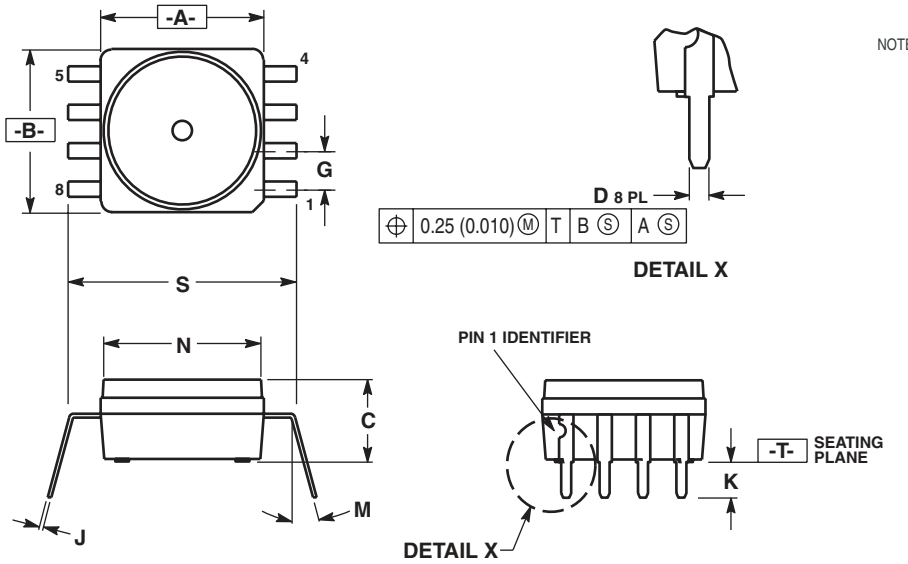


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01
ISSUE A
SMALL OUTLINE PACKAGE
SURFACE MOUNT

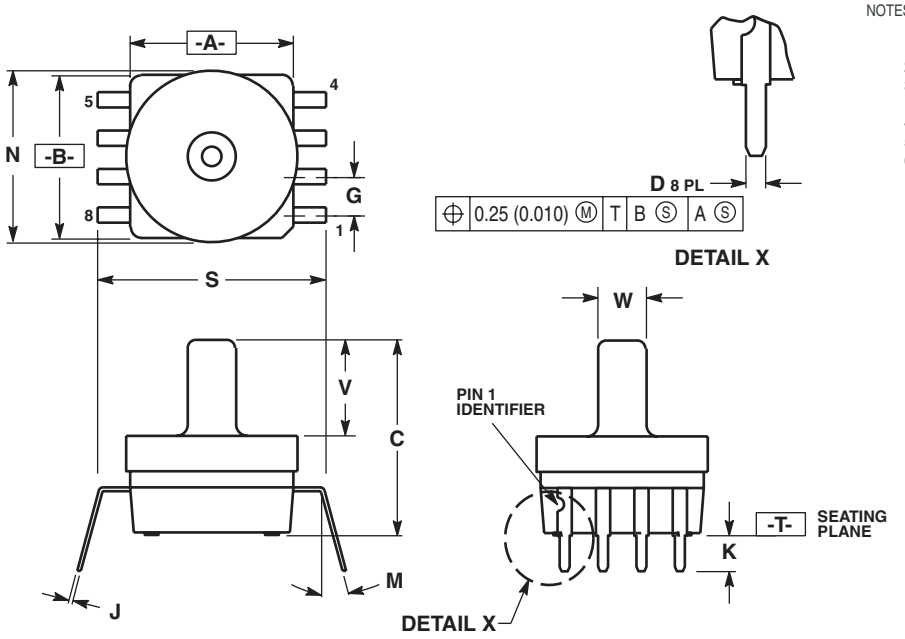
PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.210	0.220	5.33	5.59
D	0.026	0.034	0.66	0.864
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.405	0.415	10.29	10.54
S	0.540	0.560	13.72	14.22

CASE 482B-03
ISSUE B
SMALL OUTLINE PACKAGE
THROUGH-HOLE

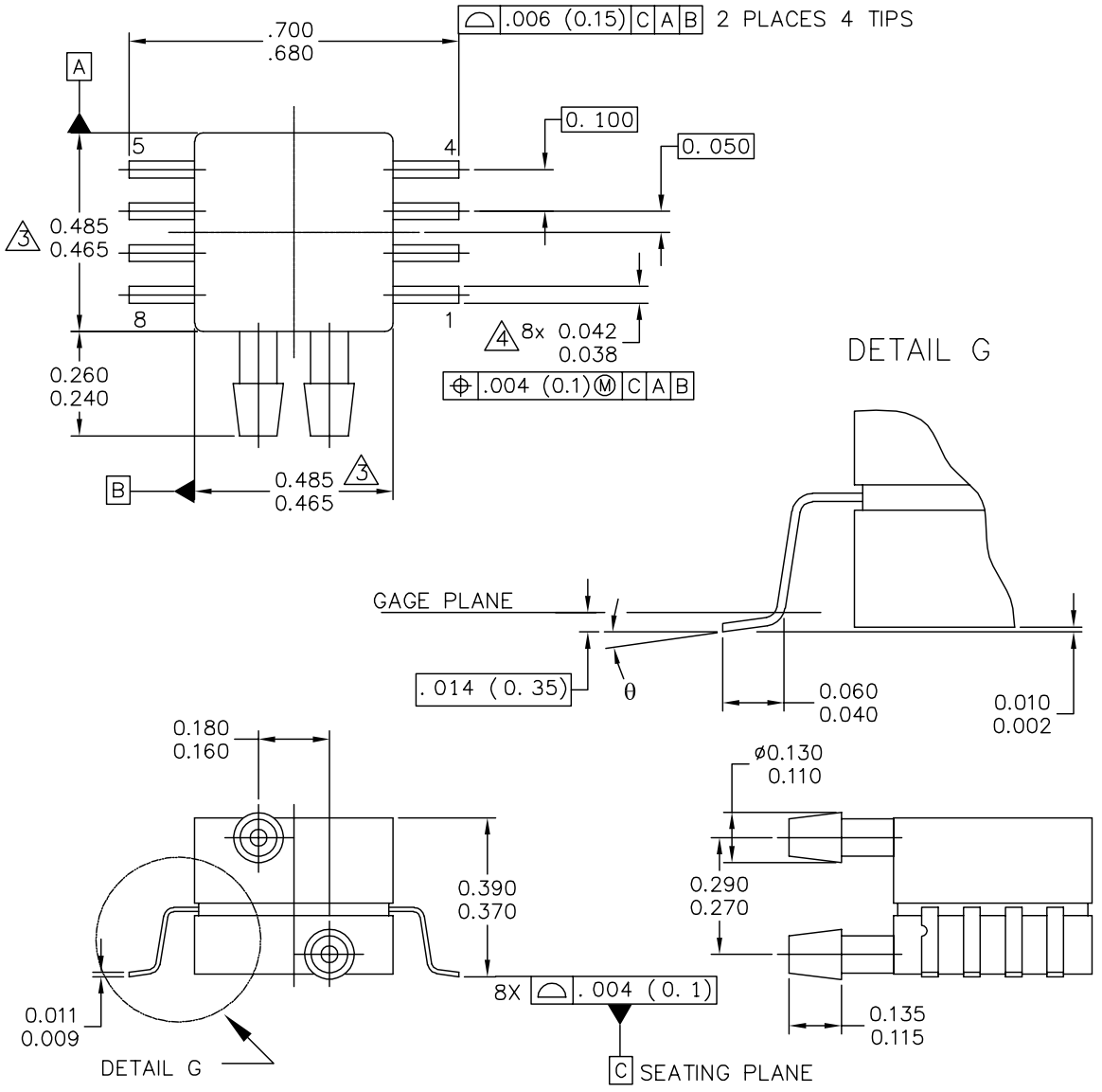


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.026	0.034	0.66	0.864
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.444	0.448	11.28	11.38
S	0.540	0.560	13.72	14.22
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482C-03
ISSUE B
SMALL OUTLINE PACKAGE
THROUGH-HOLE

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: A
	CASE NUMBER: 1351–01	27 JUL 2005
	STANDARD: NON–JEDEC	

CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE
SURFACE MOUNT

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 MAXIMUM.

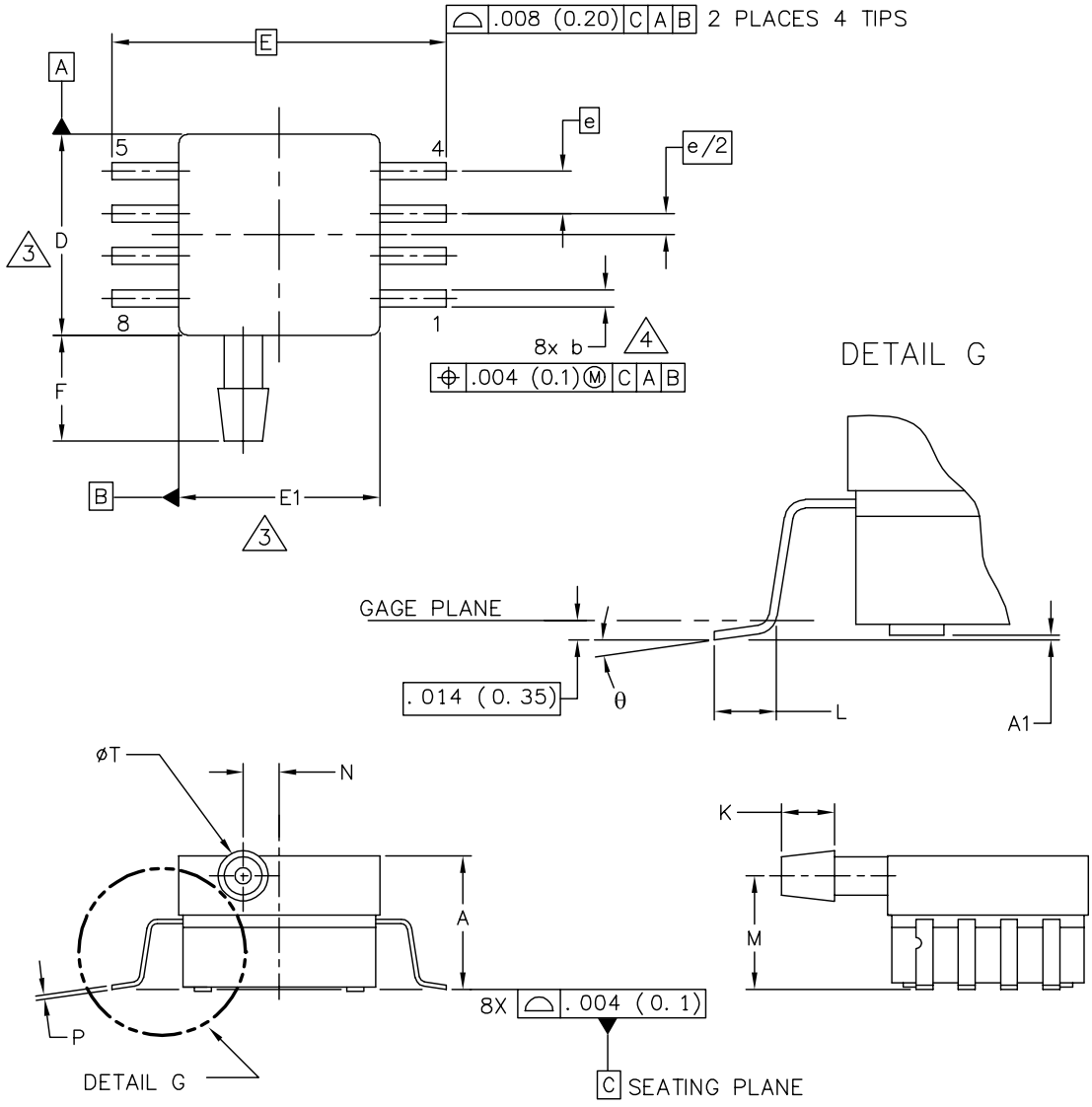
STYLE 1:	STYLE 2:
PIN 1: GND	PIN 1: N/C
PIN 2: +Vout	PIN 2: Vs
PIN 3: Vs	PIN 3: GND
PIN 4: –Vout	PIN 4: Vout
PIN 5: N/C	PIN 5: N/C
PIN 6: N/C	PIN 6: N/C
PIN 7: N/C	PIN 7: N/C
PIN 8: N/C	PIN 8: N/C

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA99255D	REV: A
8 LD SNSR, DUAL PORT	CASE NUMBER: 1351–01	27 JUL 2005
	STANDARD: NON–JEDEC	

CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE
SURFACE MOUNT

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SOP, SIDE PORT	DOCUMENT NO: 98ASA99303D	REV: B
	CASE NUMBER: 1369–01	24 MAY 2005
	STANDARD: NON–JEDEC	

CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE
SURFACE MOUNT

PACKAGE DIMENSIONS

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.300	.330	7.11	7.62	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	–	---	---	---	---
b	.038	.042	0.96	1.07	–	---	---	---	---
D	.465	.485	11.81	12.32	–	---	---	---	---
E	.717 BSC		18.21 BSC		–	---	---	---	---
E1	.465	.485	11.81	12.32	–	---	---	---	---
e	.100 BSC		2.54 BSC		–	---	---	---	---
F	.245	.255	6.22	6.47	–	---	---	---	---
K	.120	.130	3.05	3.30	–	---	---	---	---
L	.061	.071	1.55	1.80	–	---	---	---	---
M	.270	.290	6.86	7.36	–	---	---	---	---
N	.080	.090	2.03	2.28	–	---	---	---	---
P	.009	.011	0.23	0.28	–	---	---	---	---
T	.115	.125	2.92	3.17	–	---	---	---	---

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA99303D	REV: B
8 LD SOP, SIDE PORT	CASE NUMBER: 1369–01	24 MAY 2005
	STANDARD: NON–JEDEC	

CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE
SURFACE MOUNT

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MPXV4006G
Rev. 6
01/2007