FEATURES

- TI AM1808 ARM9 Application Processor
  - **456 MHz ARM926EJ-S MPU**
    - 16 KB L1 Program Cache
    - 16 KB L1 Data Cache
    - 8 KB Internal RAM
    - 64 KB boot ROM
    - JTAG Emulation/Debug
- On-Board Xilinx Spartan-6 FPGA
  - Up To XC6SLX45
    - Up To 2,088 KBits Block RAM
    - Up To 6,822 Slices (6 Input LUTs)
  - 1050 Mbps data rate
  - JTAG Interface/Debug
- Up To 256 MB mDDR2 CPU RAM
- Up To 512 MB Parallel NAND FLASH
- 8 MB SPI based NOR FLASH
- Integrated Power Management
- Standard SO-DIMM-200 Interface
  - 96 FPGA User I/O Pins
  - 10/100 EMAC MII / MDIO
  - 2 UARTS
  - 2 McBSPs
  - 2 USB Ports
  - Video Output
  - Camera/Video Input
  - MMC/SD
  - SATA
  - Single 3.3V Power Supply

APPLICATIONS

- Embedded Instrumentation
- Industrial Automation
- Industrial Instrumentation
- Medical Instrumentation
- Embedded Control Processing
- Network Enabled Data Acquisition
- Test and Measurement
- Software Defined Radio
- Bar Code Scanners
- Power Protection Systems
- Portable Data Terminals

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Linux
  - QNX 6.4
  - Windows Embedded CE Ready
  - ThreadX Real Time OS

DESCRIPTION

The MitySOM-1808F is a highly configurable, very small form-factor processor card that features a Texas Instruments AM1808 456 MHz ARM Applications Processor tightly integrated with the Xilinx Spartan-6 Field Programmable Gate Array (FPGA), FLASH (NAND, and NOR) and mDDR2 RAM memory subsystems. The design of the MitySOM-1808F allows end users the capability to develop programs/logic images for both the ARM processor and the FGPA. The MitySOM-1808F provides a complete and flexible digital processing infrastructure necessary for the most demanding embedded applications development.

The AM1808 includes an ARM926EJ-S micro-processor unit (MPU) capable of running the rich software applications programmer interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, QNX and Windows XP embedded.

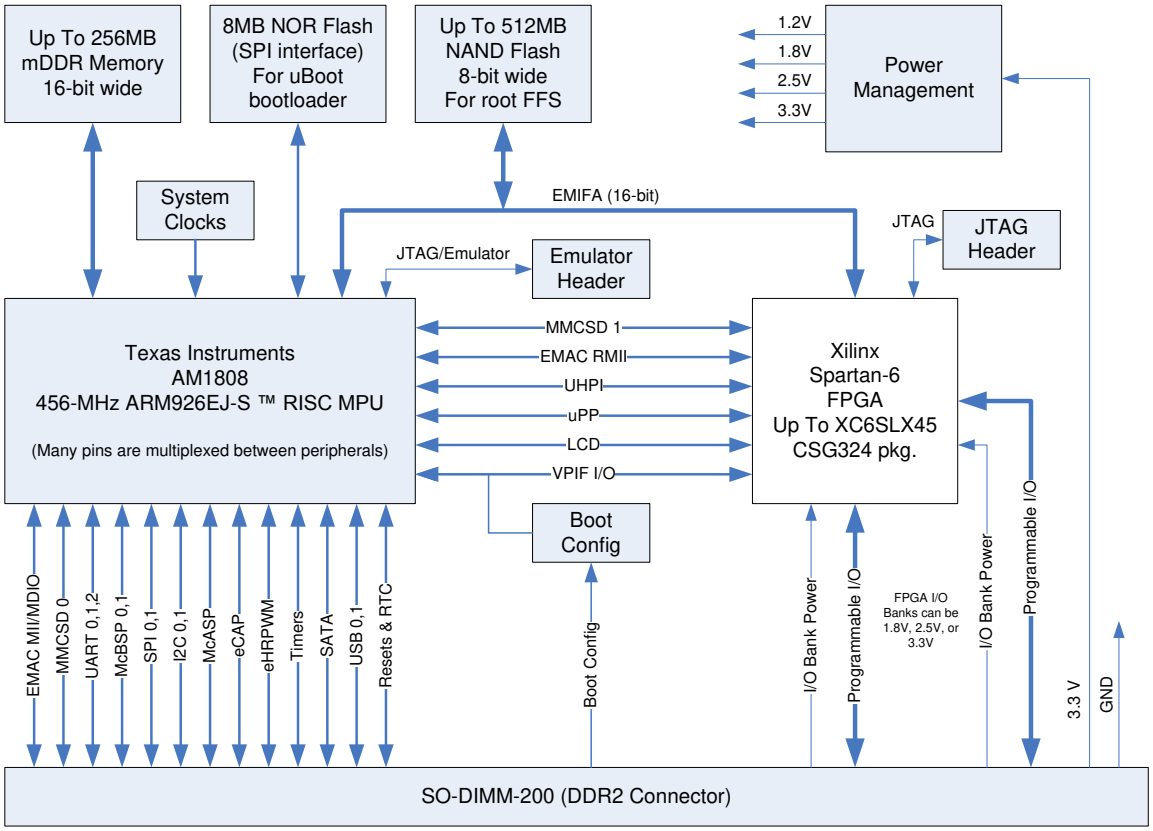

Figure 1 MitySOM-1808F Block Diagram

Figure 1 provides a top level block diagram of the MitySOM-1808F processor card. As shown in the figure, the primary interface to the MitySOM-1808F is through a standard SO-DIMM-200 card edge interface. The interface provides power, synchronous serial connectivity, and up to 96 pins of configurable FPGA I/O for application defined interfacing. Details of the SO-DIMM-200 connector interface are included in the SO-DIMM-200 Interface Description, below.

FPGA Bank I/O

The MitySOM-1808F provides 96 lines of FPGA I/O directly to the SO-DIMM-200 card edge interface. The 96 lines of FPGA I/O are distributed across 2 banks of the FPGA. These I/O lines and their associated logic are completely configurable within the FPGA at the end user's discretion.

With the Xilinx Spartan-6 series FPGA, up to the XC6SLX45, each of the user controlled banks may be configured to operate on a different electrical interface standard based on

input voltage provided at the card edge connector. The banks support 3.3V, 2.5V, and 1.8V standard CMOS switching level technology. In addition, the I/O lines from the FPGA have been routed as differential pairs and support higher speed LVDS standards as well as SSTL 2.5 switching standards. Various forms of termination (pull-up/pull-down, digitally controlled impedance matching) are available within the FPGA switch fabric. Refer to the Xilinx Spartan 6 user's guide for more information.

AM1808 mDDR2 Memory Interface

The AM1808 includes a dedicated DDR2 SDRAM memory interface. The MitySOM-1808F includes up to 256 MB of mDDR2 RAM integrated with the AM1808 processor. The bus interface is capable of burst transfer rates of 600 MB / second.

AM1808 SPI NOR FLASH Interface

The MitySOM-1808F includes 8 MB of SPI NOR FLASH. This FLASH memory is intended to store a factory provided bootloader, and typically a compressed image of a linux kernel for the ARM core processor.

EMIFA - FPGA / NAND FLASH Interface

The AM1808 and the Spartan-6 FPGA are connected using the DSP Asynchronous External Memory Interface (EMIFA). The EMIFA interface includes 3 chip select spaces. The EMIF interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, and 16 bit data word sizes may be used. Two of the three chip select lines (CE2, CE3) are reserved for the FPGA interface. The MitySOM-1808F also includes 4 lines between the FPGA and the OMAP for the purposes of generating interrupt signals.

In addition to the FPGA, up to 512 MB of on-board NAND FLASH memory is connected to the AM1808 using the EMIFA bus. The FLASH memory is 8 bits wide and is connected to third chip select line of the EMIFA (CE1). The FLASH memory is typically used to store the following types of data:

- ARM Linux / Windows Embedded CE / QNX embedded root file-system
- FPGA application images
- runtime ARM software
- runtime application data (non-volatile storage)

AM1808 Camera and Video Interfaces

The AM1808 includes an optional video port I/O interface commonly used to drive LCD screens as well as a camera input interface. These interfaces have been routed to the FPGA, which may be routed to the FPGA output pins on the SO-DIMM-200 connector. By routing the video data through the FPGA, additional user customization and/or processing (e.g., overlays of video output, preprocessing or filtering of camera input) may be offloaded from the AM1808 to the FPGA for compute intensive applications.

Debug Interface

Both the JTAG interface signals for the FPGA and the JTAG signals for the AM1808 processor have been brought out to a Hirose header that is intended for use with an available Critical Link breakout adapter. This header can be removed for production units; please contact your Critical Link representative for details.

This adapter is not included with individual modules but is included with each Critical Link Development Kit that is ordered. If an adapter, Critical Link (CL) part number 80-000286, is needed please contact your Critical Link representative.

Software and Application Development Support

Users of the MitySOM-1808F are encouraged to develop applications and FPGA firmware using the MitySOM-1808F hardware and software development kit provided by Critical Link LLC. The development kit includes an implementation of an OpenEmbedded board support package providing an Angstrom based Linux distribution and compatible gcc compiler tool-chain with debugger.

To support rapid FPGA and applications development, netlist components - compatible with the Xilinx ISE FPGA synthesis tool – for commonly used FPGA designs and a corresponding set of Linux loadable kernel modules are included. The libraries provide the necessary functions needed to configure the MitySOM-1808F, program standalone embedded applications, and interface with the various hardware components both on the processor board as well as a custom application carrier card. The libraries include several interface "cores" – FPGA and ARM software modules designed to interface with various high performance data converter modules (ADCs, DACs, LCD and touchscreen interfaces, etc) – as well as bootloading and FLASH programming utilities.

Growth Options

The MitySOM-1808F has been designed to support several upgrade options. These options include various speed grades, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.5 V
Storage Temperature Range	-65°C to 80°C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range Commercial	0°C to 70°C
Ambient Temperature Range Industrial	-40°C to 85°C
Humidity	0 to 95% Non-condensing
MIL-STD-810F	Contact Critical Link for Details

SO-DIMM-200 Interface Description

The primary interface connector for the MitySOM-1808F is the SO-DIMM card edge interface.

Table 1 SO-DIMM Pin-Out

Pin	I/O	Signal	Pin	I/O	Signal
1	-	+3.3 V in	2	-	+3.3 V in
3	-	+3.3 V in	4	-	+3.3 V in
5	-	+3.3 V in	6	-	+3.3 V in
7	-	GND	8	-	GND
9	-	GND	10	-	GND
11	I	RESET_IN#	12		EXT_BOOT#
13	O	SATA_TX_P	14	I/O	GP0_7
15	O	SATA_TX_N	16	I/O	GP0_10
17	I	SATA_RX_P	18	I/O	GP0_11
19	I	SATA_RX_N	20	I/O	GP0_15
21	I	USB0_ID	22	I/O	GP0_6
23	I/O	USB1_D_N	24	I/O	GP0_14
25	I/O	USB1_D_P	26	I/O	GP0_12
27	O	USB0_VBUS	28	I/O	GP0_5
29	I/O	USB0_D_N	30	I/O	GP0_13
31	I/O	USB0_D_P	32	I/O	GP0_1
33	O	USB0_DRVVBUS	34	I/O	GP0_4
35	-	3V RTC Battery	36	I/O	GP0_3
37	-	+3.3 V in	38	-	+3.3 V in
39	-	+3.3 V in	40	-	+3.3 V in
41	-	GND	42	-	GND
43	I/O	SPI1_MISO	44	I/O	GP0_2
45	I/O	SPI1_MOSI	46	I/O	GP0_0
47	I/O	SPI1_ENA	48	I/O	GP0_8
49	I/O	SPI1_CLK	50	I/O	GP0_9
51	I/O	SPI1_SCS1	52	I/O	MMCSD0_DAT7
53	I/O	Reserved	54	I/O	MMCSD0_DAT6
55	I/O	I2C0_SCL	56	I/O	MMCSD0_DAT5
57	I/O	I2C0_SDA	58	I/O	MMCSD0_DAT4

Pin	I/O	Signal	Pin	I/O	Signal
59	I/O	UART2_TXD / I2C1_SDA	60	I/O	MMCSD0_DAT3
61	I/O	UART2_RXD / I2C1_SCL	62	I/O	MMCSD0_DAT2
63	I/O	GND	64	I/O	GND
65	I/O	UART1_TXD	66	I/O	MMCSD0_DAT1
67	I/O	UART1_RXD	68	I/O	MMCSD0_DAT0
69	I/O	MDIO_CLK	70	I/O	MMCSD0_CMD
71	I/O	MDIO_DAT	72	I/O	MMCSD0_CLK
73	I/O	MII_RXCLK	74	I/O	MII_TXCLK
75	I/O	MII_RXDV	76	I/O	MII_TXD3
77	I/O	MII_RXD0	78	I/O	MII_TXD2
79	I/O	MII_RXD1	80	I/O	MII_TXD1
81	I/O	MII_RXD2	82	I/O	MII_TXD0
83	I/O	MII_RXD3	84	I/O	MII_TXEN
85	-	GND	86	-	GND
87	I/O	MII_CRS	88	I/O	MII_COL
89	I/O	MII_RXER	90	I/O	FPGA_SUSPEND
91	I/O	B1 _47_P.U17	92	I/O	B1 _48_P.M14
93	I/O	B1_ 47_N.U18	94	I/O	B1_ 48_N.N14
95	I/O	B1 _45_P.T17	96	I/O	B1 _46_P.N15
97	I/O	B1_ 45_N.T18	98	I/O	B1_ 46_N.N16
99	I/O	B1_43_P.P17	100	I/O	B1 _44_P.L12
101	I/O	B1_43_N.P18	102	I/O	B1_ 44_N.L13
103	I/O	B1_41_P.N17	104	I/O	B1 _42_P.K12
105	I/O	B1_41_N.N18	106	I/O	B1_ 42_N.K13
107	-	GND	108	-	GND
109	I/O	B1_39_P.M16	110	I/O	B1 _40_P.L15
111	I/O	B1_39_N.M18	112	I/O	B1_ 40_N.L16
113	I/O	B1_37_P.L17	114	I/O	B1 _38_P.K15
115	I/O	B1_37_N.L18	116	I/O	B1_ 38_N.K16
117	I/O	B1_35_P.K17	118	I/O	B1 _36_P.J13
119	I/O	B1_35_N.K18	120	I/O	B1_ 36_N.K14
121	I/O	B1_33_P.J16	122	I/O	B1 _34_P.H15
123	I/O	B1_33_N.J18	124	I/O	B1_ 34_N.H16
125	I/O	B1_31_P.H17	126	I/O	B1 _32_P.H13
127	I/O	B1_31_N.H18	128	I/O	B1_ 32_N.H14
129	-	GND	130	-	GND
131	I/O	B1_29_P.G16	132	I/O	B1 _30_P.F15
133	I/O	B1_29_N.G18	134	I/O	B1_ 30_N.F16
135	I/O	B1_27_P.F17	136	I/O	B1 _28_P.H12
137	I/O	B1_27_N.F18	138	I/O	B1_ 28_N.G13
139	I/O	B1_25_P.E16	140	I/O	B1 _26_P.F14
141	I/O	B1_25_N.E18	142	I/O	B1_ 26_N.G14
143	I/O	B1_23_P.D17	144	I/O	B0 _24_P.F13
145	I/O	B1_23_N.D18	146	I/O	B0_ 24_N.E13
147	I/O	B1_21_P.C17	148	I/O	B0 _22_P.D14
149	I/O	B1_21_N.C18	150	I/O	B0_ 22_N.C14
151	-	GND	152	-	GND
153	I/O	B0_19_P.B16	154	I/O*	B0 _20_P.F12*
155	I/O	B0_19_N.A16	156	I/O*	B0_ 20_N.E12*
157	I/O	B0_17_P.C15	158	I/O*	B0 _18_P.D12*

Pin	I/O	Signal	Pin	I/O	Signal
159	I/O	B0_17_N.A15	160	I/O*	B0_ 18_N.C12*
161	I/O	B0_15_P.B14	162	I/O*	B0 _16_P.F11*
163	I/O	B0_15_N.A14	164	I/O*	B0_ 16_N.E11*
165	I/O	B0_13_P.C13	166	I/O	B0 _14_P.D11
167	I/O	B0_13_N.A13	168	I/O	B0_ 14_N.C11
169	I/O	B0_11_P.B12	170	I/O*	B0 _12_P.E7*
171	I/O	B0_11_N.A12	172	I/O*	B0_ 12_N.E8*
173	-	GND	174	-	GND
175	I/O	B0_9_P.B11	176	I/O	B0 _10_P.D9
177	I/O	B0_9_N.A11	178	I/O	B0_ 10_N.C9
179	I/O	B0_7_P.C10	180	I/O	B0 _8_P.D8
181	I/O	B0_7_N.A10	182	I/O	B0_ 8_N.C8
183	I/O	B0_5_P.B9	184	I/O	B0 _6_P.D6
185	I/O	B0_5_N.A9	186	I/O	B0_ 6_N.C6
187	I/O	B0_3_P.B8	188	I/O	B0 _4_P.B6
189	I/O	B0_3_N.A8	190	I/O	B0_ 4_N.A6
191	I/O	B0_1_P.C7	192	I/O	B0 _2_P.C5
193	I/O	B0_1_N.A7	194	I/O	B0_ 2_N.A5
195	-	GND	196	-	GND
197	-	VCCO_1	198	-	VCCO_0
199	-	VCCO_1	200	-	VCCO_0

* The Xilinx 6SLX45 FPGA does not bond I/O Buffers to balls E7, E8, F11, E11, D12, C12, E12, and F12 of the package used for this module. For MitySOM-1808F configurations using this FPGA option, these edge connector signals should be treated as no-connects and will not function as FPGA I/O lines.

The signal group description for the above pins is included in Table 2

Table 2 Signal Group Description

Signal / Group	I/O	Description
3.3 V in	N/A	3.3 volt input power referenced to GND.
EXT_BOOT#	I	Bootstrap configuration pin. Pull low to configure booting from external UART1.
RESET_IN#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the DSP processor.
SPI_XXXX	I/O	The pins with an SPI_ prefix are direct connections to the AM1808 pins supporting the SPI1 interface. The SPI1_CLK, SPI1_ENA, SPI1_MISO, SPI1_MOSI pins must remain configured for the SPI function in order to support interfacing to the on-board SPI boot ROM. For details please refer to the AM1808 processor specifications.
MII_XXXX	I/O	The pins with an MII_ prefix are direct connections to the AM1808 pins supporting the

Signal / Group	I/O	Description
		media independent interface (MII) function. The MII pins provide multiplex capability and may alternately be used as UART, GPIO, and SPI control pins. For details please refer to the OMAP-L137 processor specification.
MDIO_XX	I/O	The MDIO_CLK and MDIO_DAT signals are direct connects to the corresponding MDIO signals on the AM1808 processor. These pins may be configured for GPIO.
GP0_X	IO	General Purpose / multiplexed pins. These pins are direct connects to the corresponding GP0[X] pins on the AM1808 processor. The include support for the McASP, general purpose I/O, UART flow control, and McBSP 1. For details please refer to the AM1808 processor specifications.
SATA_TX_P/N	O	These pins are direct connects to the AM1808 SATA_TX differential Serial ATA controller pins.
SATA_RX P/N	I	These pins are direct connects to the AM1808 SATA_RX differential Serial ATA controller pins.
GND	N/A	System Digital Ground.
BX_Y_P.ZZ, BX_Y_N.ZZ	IO	FPGA I/O pins. These pins are routed directly to FPGA pins ZZ. The "X" indicates which FPGA bank the pin is allocated. The bank is either 0 or 1. The FPGA fabric supports routing pins in differential pairs, the Y_P and Y_N portion of the name indicates the pair number and polarity. The pins have been routed in pairs with phase matched line lengths.
VCCO_X	I	FPGA Bank interface power input. These pins must be tied to the desired voltage used for the FPGA Bank 0 or 1 interface pins. Please refer to the VCCO input pin specifications for the Xilinx Spartan 6 family of devices for further information. Typical values are 3.3V and 2.5 volts.
USB0_XXXX, USB1_XXXX	I/O	The USBN_ prefixed pins are direct connects to the corresponding pins on the AM1808 processor. For details please refer to the AM1808 processor specifications.

DEBUG INTERFACE

Below is the pin-out for the Hirose 31 pin header (DF9-31P-1V(32)) that interfaces with an available adapter board, CL part number 80-000286, to debug the AM1808 and FPGA.

Debug Interface Connector Description (J2)

Table 3 OMAP-L138 Hirose Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	O	OMAP EMU1
3	-	GND	4	O	OMAP EMU0
5	-	GND	6	I	OMAP TCK
7	-	GND	8	O	OMAP RTCK
9	-	GND	10	O	OMAP TDO
11	-	GND	12	-	OMAP VCC / 3.3V
13	-	GND	14	I	OMAP TDI
15	-	GND	16	I	OMAP TRST
17	-	GND	18	I	OMAP TMS
19	-	GND	20	-	GND
21	-	GND	22	O	FPGA VREF / VCCAUX
23	-	GND	24	I	FPGA TMS
25	-	GND	26	I	FPGA TCK
27	-	GND	28	O	FPGA TDO
29	-	GND	30	I	FPGA TDI
31	-	GND			

ELECTRICAL CHARACTERISTICS

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V33	Voltage supply, 3.3 volt input.		3.2	3.3	3.4	Volts
I33	Quiescent Current draw, 3.3 volt input			TBS	TBS	mA
I33-max	Max current draw, positive 3.3 volt input.			TBS	TBS	mA
FCPU	CPU internal clock Frequency (PLL output)		25	375	456	MHz
FEMIF	EMIF bus frequency	Must be ½ CPU	-	100	-	MHz
	1. Power utilization of the MitySOM-1808F is heavily dependant on end-user application. Major factors include: ARM CPU PLL configuration, DSP Utilization FPGA utilization, and external DDR2 RAM utilization.					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 5: Standard Model Numbers

Model	ARM Speed	FPGA	NOR Flash	NAND Flash	RAM	Operating Temp
1808-FG-225-RC	456 MHz	6SLX16	8MB	256MB	128MB	0°C to 70° C
1808-DG-225-RI	375 MHz	6SLX16	8MB	256MB	128MB	-40°C to 85° C
1808-FI-236-RC	456 MHz	6SLX45	8MB	512MB	256MB	0°C to 70° C

MECHANICAL INTERFACE

A mechanical outline of the MitySOM-1808F is illustrated in Figure 2, below.

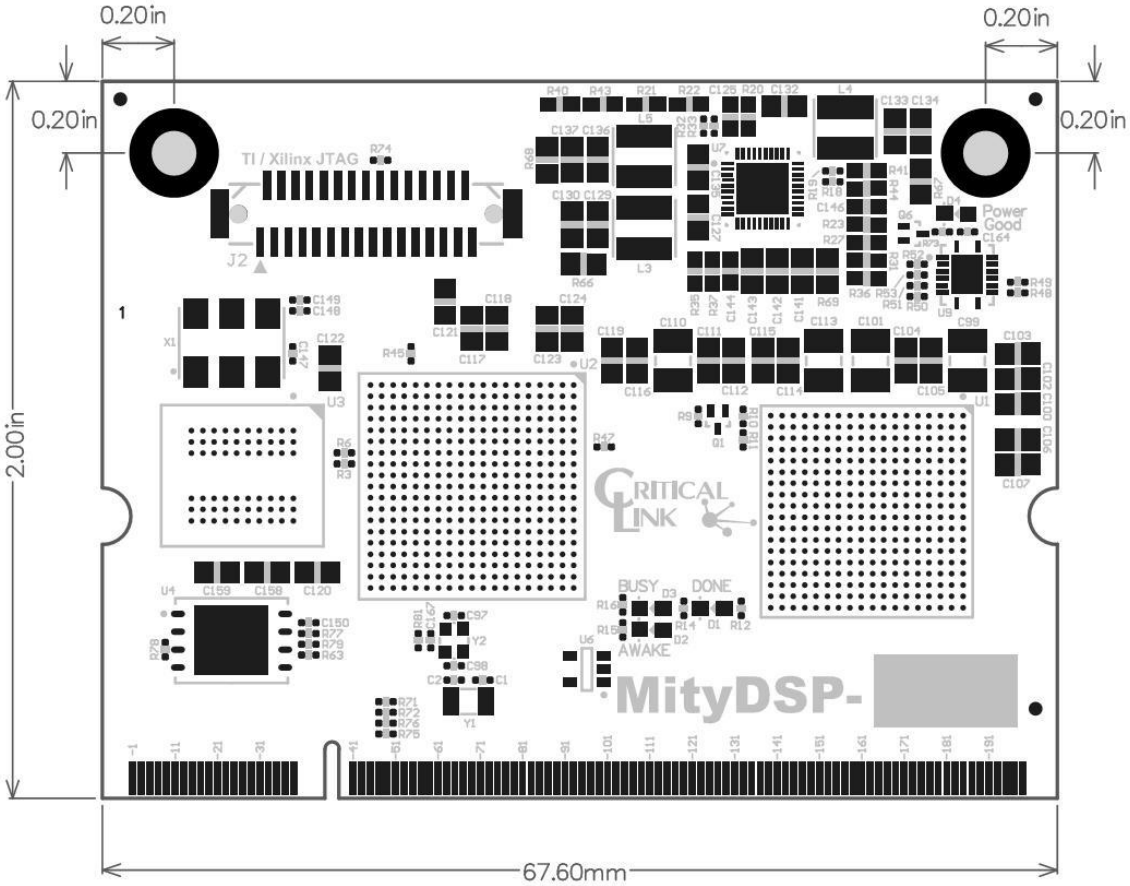

Figure 2 MitySOM-1808F Mechanical Outline

REVISION HISTORY

Date	Change Description
7-NOV-2009	Preliminary Draft, product overview
10-NOV-2009	Updates after initial review.
15-JAN-2010	Updates to features, applications and benefits
16-MAR-2010	Finalize connector pin-outs. Update mechanical outlines.
6-APR-2010	Update product photo and speed grade.
21-APR-2010	Update specifications and options.
26-JUL-2010	Update ordering information, images and mechanical drawing.
11-FEB-2011	Correct edge connector Table 1. Update DDR bandwidth to support 150 MHz clocking.
02-JUN-2011	Update edge connector Table 1 to indicate unavailable FPGA pins for 6SLX45 options.
12-JUL-2011	Update NAND to indicate 8 bit data width. Update block diagram accordingly.
17-FEB-2012	Updated ordering information.
13-AUG-2012	Fix typo in signal name for pin 84.
11-DEC-2012	Update Debug Header information, added MIL-STD-810F and Up To notation for RAM and NAND
5-MAR-2014	Update MitySOM product name.