



**MOTOROLA**

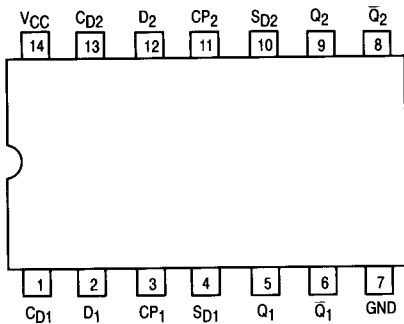
# Dual D-Type Flip-Flop With Clear and Preset

**ELECTRICALLY TESTED PER:  
MIL-M-38510/30102**

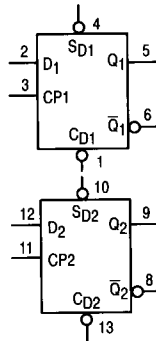
The 54LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high-speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

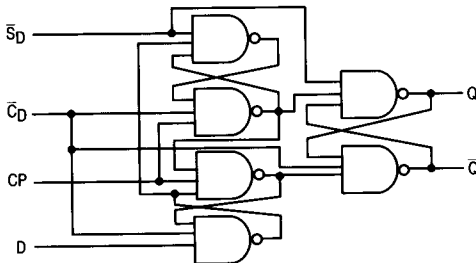
**CONNECTION DIAGRAM**



**LOGIC SYMBOL**



**LOGIC DIAGRAM**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

\* Both outputs will be High while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go High simultaneously. If the levels at the set and clear near  $V_{IL}$  maximum then we cannot guarantee to meet the minimum level for  $V_{OH}$ .

## Military 54LS74A



**AVAILABLE AS:**

- 1) JAN: JM38510/30102BXA
- 2) SMD: N/A
- 3) 883: 54LS74A/BXAJC

**X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2**

**THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.**

**PIN ASSIGNMENTS**

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
CD1	1	1	2	GND
D1	2	2	3	VCC
CP1	3	3	4	VCC
SD1	4	4	6	GND
Q1	5	5	8	VCC
Q1-bar	6	6	9	VCC
GND	7	7	10	GND
Q2	9	9	13	VCC
SD2	10	10	14	GND
CP2	11	11	16	VCC
D2	12	12	18	VCC
CD2	13	13	19	GND
VCC	14	14	20	VCC

**BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX**

**MODE SELECT - TRUTH TABLE**

Operating Mode	Inputs			Outputs	
	$\bar{S}_D$	$\bar{C}_D$	D	Q	Q-bar
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

H, h = HIGH Voltage Level

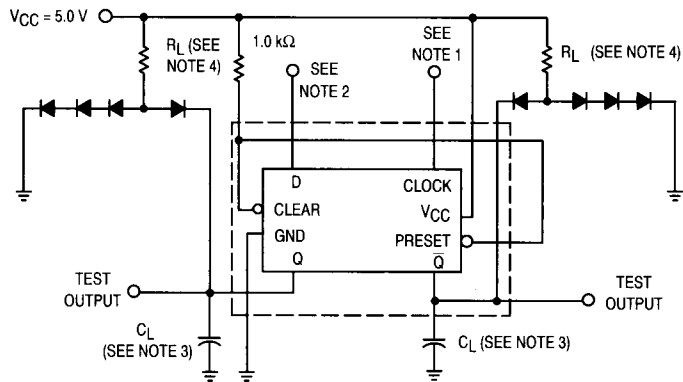
L, l = LOW Voltage Level

X = Don't Care

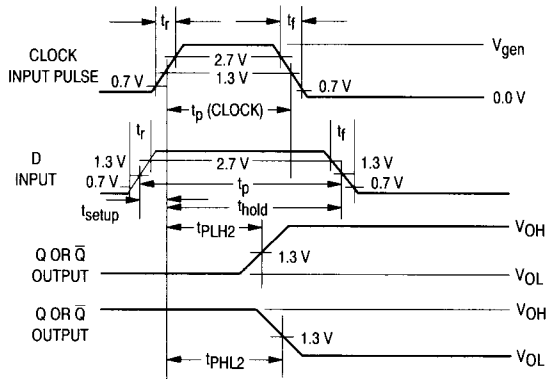
l, h, (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

# 54LS74A

## SYNCHRONOUS SWITCHING TEST CIRCUIT



## WAVEFORMS

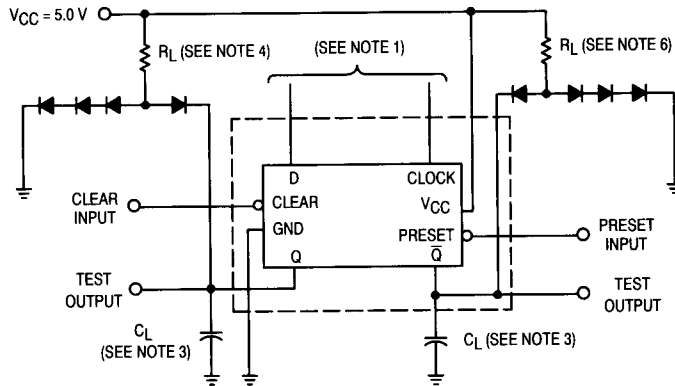


### NOTES:

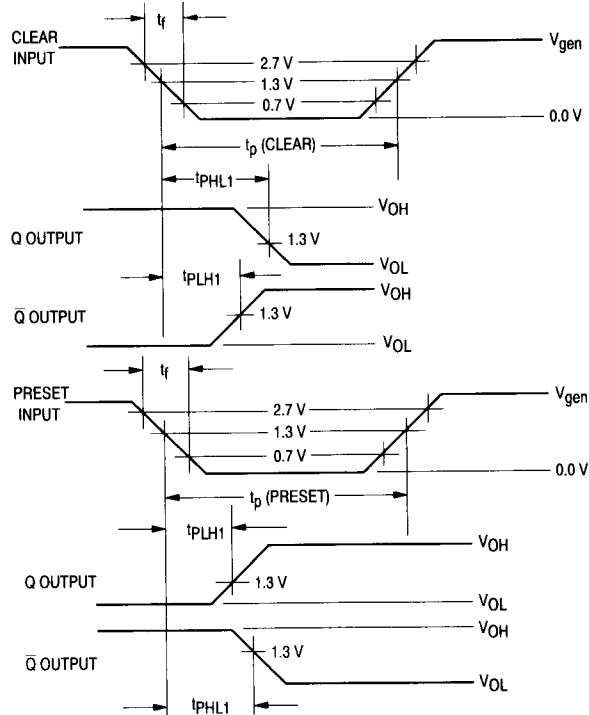
1. Clock input pulse has the following characteristics:  
 $V_{gen} = 3.0 \text{ V}$ ,  $t_r \leq 15 \text{ ns}$ ,  $t_f \leq 6.0 \text{ ns}$ ,  $t_p(\text{clock}) = 30 \text{ ns}$  and  $\text{PRR} \leq 1.0 \text{ MHz}$ . When testing  $f_{MAX}$  see table,  $t_p(\text{clock}) \leq 30 \text{ ns}$ ,  $t_r = t_f \leq 6.0 \text{ ns}$ .
2. D input has the following characteristics:  
 $V_{gen} = 3.0 \text{ V}$ ,  $t_r \leq 15 \text{ ns}$ ,  $t_f \leq 6.0 \text{ ns}$ ,  $t_{setup} = 20 \text{ ns}$ ,  $t_{hold} = 5.0 \text{ ns}$ ,  $t_p = 25 \text{ ns}$  and  $\text{PRR}$  is 50% of the clock  $\text{PRR}$ . When testing  $f_{MAX}$ ,  $t_r = t_f \leq 6.0 \text{ ns}$ .
3.  $C_L = 50 \text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$ .
5. All diodes are 1N3064, or equivalent.

# 54LS74A

## CLEAR & PRESET SWITCHING TEST CIRCUIT



### WAVEFORMS





#### NOTES:

1. Clear or preset inputs dominate regardless of the state of the clock or D inputs.
2. Clear or preset input pulse characteristics:  $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 6.0\text{ ns}$ ,  $PRR \leq 1.0\text{ MHz}$ ,  $t_p(\text{clear}) = t_p(\text{preset}) = 35\text{ ns}$ .
3.  $C_L = 50\text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table).

## 54LS74A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IN</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V, CP = GND and (See Note 1).
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V, CP = (See Note 1) and GND.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH1</sub>	Logical "1" Input Current (D inputs)		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = 4.5 V, CD = GND.
I <sub>IHH1</sub>	Logical "1" Input Current (D inputs)		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, CD = GND, other inputs = 4.5 V.
I <sub>IH2</sub>	Logical "1" Input Current (CP & SD)		40		40		40	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = 4.5 V, CD = GND.
I <sub>IHH2</sub>	Logical "1" Input Current (CP & SD)		200		200		200	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs = 4.5 V, CP = (See Note 2).
I <sub>IH3</sub>	Logical "1" Input Current (CD inputs)		60		60		60	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, CP = (See Note 2), SD = 4.5 V, D = GND.
I <sub>IHH3</sub>	Logical "1" Input Current (CD inputs)		300		300		300	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, CP = (See Note 2), SD = 4.5 V, D = GND.
I <sub>IL1</sub>	Logical "0" Input Current (D inputs)	-135	-370	-135	-370	-135	-370	μA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, SD = GND, other inputs = 4.5 V.
I <sub>IL2</sub>	Logical "0" Input Current (CP inputs)	-120	-360	-120	-360	-120	-360	μA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, CD = 4.5 V, other inputs = GND.
I <sub>IL3</sub>	Logical "0" Input Current (SD inputs)	-280	-760	-280	-760	-280	-760	μA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other inputs = GND.
I <sub>IL4</sub>	Logical "0" Input Current (CD inputs)	-280	-760	-280	-760	-280	-760	μA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, SD = GND, other inputs = 4.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V <sub>CC</sub> = 5.5 V, CD = GND, V <sub>OUT</sub> = GND, other inputs are open.
I <sub>CC</sub>	Power Supply Current		8.0		8.0		8.0	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V, other inputs are open.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

## NOTES:

-  2.5 V min/5.5 V max  
0.0 V
-  2.5 V min/5.5 V max  
0.0 V

54LS74A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL1</sub>	Propagation Delay SD <sub>n</sub> or CD <sub>n</sub> to Q <sub>n</sub> to Q <sub>n</sub>	5.0 —	46 40	5.0 —	59 54	5.0 —	59 54	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PLH1</sub> t <sub>PLH1</sub>	Propagation Delay SD <sub>n</sub> or CD <sub>n</sub> to Q <sub>n</sub> to Q <sub>n</sub>	5.0 —	30 25	5.0 —	39 34	5.0 —	39 34	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PHL2</sub>	Propagation Delay /Data-Output CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	46	5.0	59	5.0	59	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PLH2</sub>	Propagation Delay /Data-Output CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	5.0	30	5.0	39	5.0	39	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	20		20		20		MHz	V <sub>CC</sub> = 5.0 V, V <sub>IN</sub> = 2.7 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	25						MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.

NOTES:

1. f<sub>MAX</sub>, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.