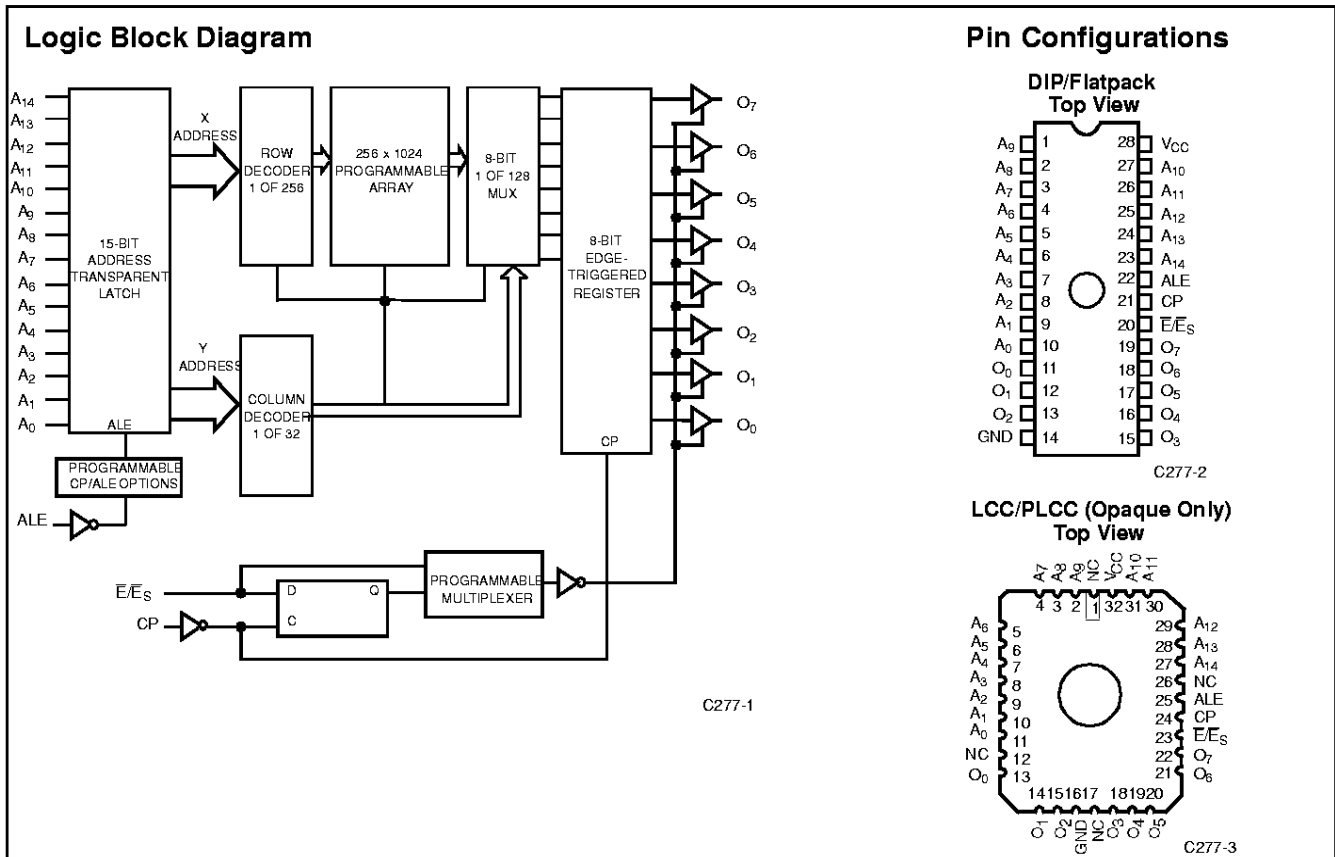




32K x 8 Reprogrammable Registered PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
 - 30-ns address set-up
 - 15-ns clock to output
- Low power
 - 660 mW (commercial)
 - 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered output registers
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge



Selection Guide

| | 7C277-30 | 7C277-40 | 7C277-50 |
|----------------------------------|----------|----------|----------|
| Minimum Address Set-Up Time (ns) | 30 | 40 | 50 |
| Maximum Clock to Output (ns) | 15 | 20 | 25 |
| Maximum Operating Current (mA) | Com'l | 120 | 120 |
| | Mil | | 130 |

Functional Description

The CY7C277 is a high-performance 32K word by 8-bit CMOS PROMs. It is packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C277 offers the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge triggered output register. The \bar{E}/E_S input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the \bar{E}/E_S pin operates as an asynchronous output enable. If the synchronous mode is selected, the \bar{E}/E_S pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted.

The user may define the polarity of the ALE signal, with the default being active HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied..... | -55°C to +125°C |
| Supply Voltage to Ground Potential | -0.5V to +7.0V (Pin 24 to Pin 12) |
| DC Voltage Applied to Outputs in High Z State | -0.5V to +7.0V |
| DC Input Voltage | -3.0V to +7.0V |
| DC Program Voltage (Pins 7, 18, 20) | 13.0V |
| UV Erasure..... | 7258 Wsec/cm ² |
| Static Discharge Voltage | >2001V (per MIL-STD-883, Method 3015) |
| Latch-Up Current..... | >200 mA |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|---------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ±10% |
| Industrial ^[1] | -40°C to +85°C | 5V ±10% |
| Military ^[2] | -55°C to +125°C | 5V ±10% |

Electrical Characteristics Over the Operating Range^[3, 4]

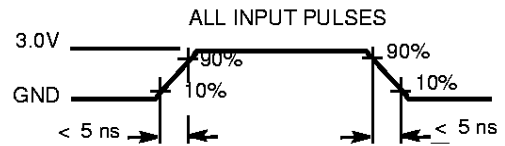
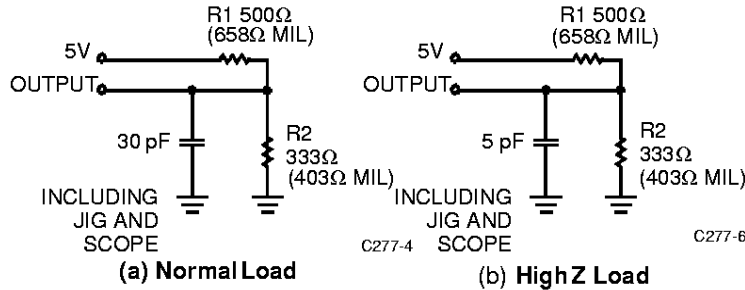
| Parameter | Description | Test Conditions | 7C277-30 | | 7C277-40, 50 | | Unit | |
|------------------|--------------------------------|--|------------|-----------------|--------------|-----------------|------|----|
| | | | Min. | Max. | Min. | Max. | | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -2.0 mA | 2.4 | | 2.4 | | V | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | V | |
| V _{IH} | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs | 2.0 | V _{CC} | 2.0 | V _{CC} | V | |
| V _{IL} | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs | | 0.8 | | 0.8 | V | |
| I _{IX} | Input Leakage Current | GND ≤ V _{IN} ≤ V _{CC} | -10 | +10 | -10 | +10 | μA | |
| V _{CD} | Input Clamp Diode Voltage | | Note 4 | | | | | |
| I _{OZ} | Output Leakage Current | 0 ≤ V _{OUT} ≤ V _{CC} , Output Disabled ^[5] | -40 | +40 | -40 | +40 | μA | |
| I _{OS} | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = 0.0V ^[6] | -20 | -90 | -20 | -90 | mA | |
| I _{CC} | Power Supply Current | V _{CC} = Max., $\overline{CS} \geq V_{IH}$ I _{OUT} = 0 mA | Commercial | | 120 | | 120 | mA |
| | | | Military | | 130 | | | |
| V _{PP} | Programming Supply Voltage | | 12 | 13 | 12 | 13 | V | |
| I _{PP} | Programming Supply Current | | | 50 | | 50 | mA | |
| V _{IHP} | Input HIGH Programming Voltage | | 3.0 | | 3.0 | | V | |
| V _{ILP} | Input LOW Programming Voltage | | | 0.4 | | 0.4 | V | |

Notes:

- Contact a Cypress representative for industrial temperature range specifications.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See "Introduction to CMOS PROMs" in this Book for general information on testing.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

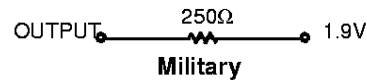
Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|--------------------|---|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$ | 10 | pF |
| C_{OUT} | Output Capacitance | | 10 | pF |

AC Test Loads and Waveforms^[4]


C277-5

Equivalent to: THÉVENIN EQUIVALENT



C277-7

CY7C277 Switching Characteristics Over the Operating Range^[3, 4]

| Parameter | Description | 7C277-30 | | 7C277-40 | | 7C277-50 | | Unit |
|-----------------|--|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{AL} | Address Set-Up to ALE Inactive | 5 | | 10 | | 10 | | ns |
| t_{LA} | Address Hold from ALE Inactive | 10 | | 10 | | 15 | | ns |
| t_{LL} | ALE Pulse Width | 10 | | 10 | | 15 | | ns |
| t_{SA} | Address Set-Up to Clock HIGH | 30 | | 40 | | 50 | | ns |
| t_{HA} | Address Hold from Clock HIGH | 0 | | 0 | | 0 | | ns |
| t_{SES} | \overline{E}_S Set-Up to Clock HIGH | 12 | | 15 | | 15 | | ns |
| t_{HES} | \overline{E}_S Hold from Clock HIGH | 5 | | 10 | | 10 | | ns |
| t_{CO} | Clock HIGH to Output Valid | | 15 | | 20 | | 25 | ns |
| t_{PWC} | Clock Pulse Width | 15 | | 20 | | 20 | | ns |
| $t_{LZC}^{[7]}$ | Output Valid from Clock HIGH | | 15 | | 20 | | 30 | ns |
| t_{HZC} | Output High Z from Clock HIGH | | 15 | | 20 | | 30 | ns |
| $t_{LZE}^{[8]}$ | Output Valid from \overline{E} LOW | | 15 | | 20 | | 30 | ns |
| $t_{HZE}^{[8]}$ | Output High Z from \overline{E} HIGH | | 15 | | 20 | | 30 | ns |

Notes:

7. Applies only when the synchronous (\overline{E}_S) function is used.
8. Applies only when the asynchronous (\overline{E}) function is used.

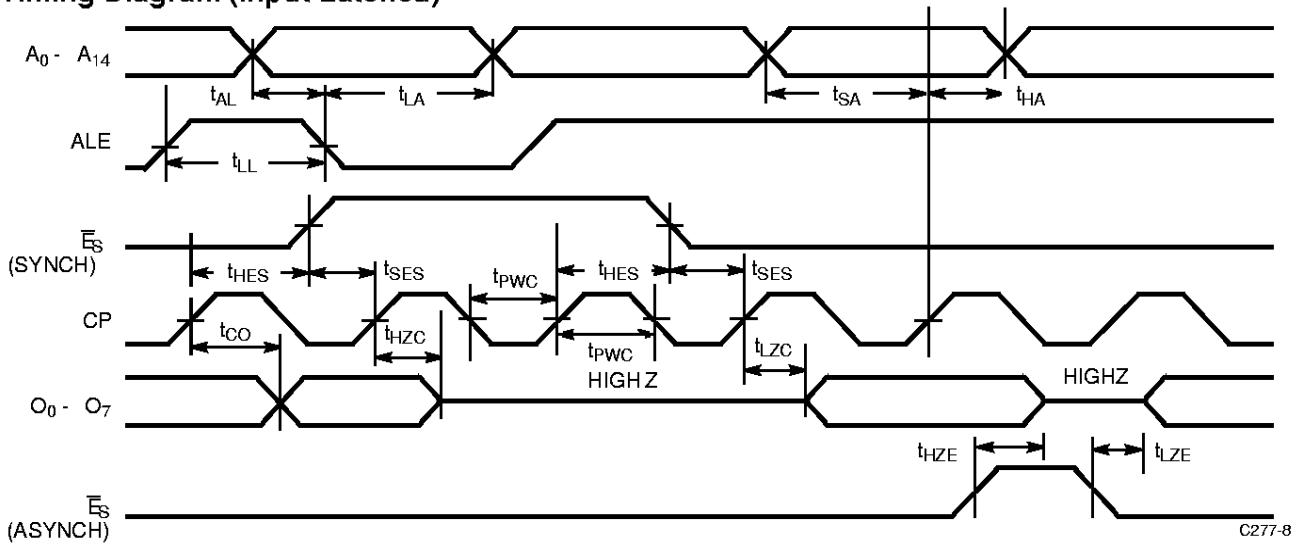
Architecture Configuration Bits

| Architecture Bit | Architecture Verify D ₇ - D ₀ | | Function |
|------------------|---|-------------|---|
| ALE | D ₁ | 0 = DEFAULT | Input Transparent |
| | | 1 = PGMED | Input Latched |
| ALEP | D ₂ | 0 = DEFAULT | ALE = Active HIGH |
| | | 1 = PGMED | ALE = Active LOW |
| E/E _S | D ₀ | 0 = DEFAULT | Asynchronous Output Enable (E) |
| | | 1 = PGMED | Synchronous Output Enable (E _S) |

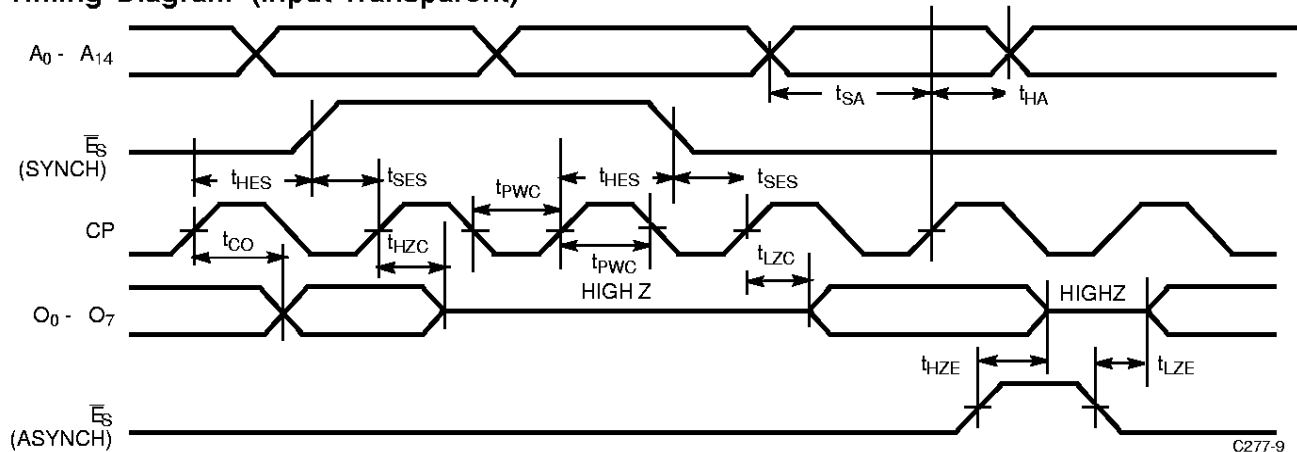
Bit Map

| Programmer Address (Hex.) | RAM Data |
|---------------------------|--------------|
| 0000 | Data |
| . | . |
| . | . |
| 7FFF | Data |
| 8000 | Control Byte |

Architecture Byte (8000)
 D7 D0
 C7 C6 C5 C4 C3 C2 C1 C0

Timing Diagram (Input Latched)⁹


C277-8

Timing Diagram (Input Transparent)


C277-9

Notes:

- ALE is shown with positive polarity.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed

programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

| Mode | Pin Function ^[10] | | | | | |
|-----------------|------------------------------|----------------------------------|-------------------|------------------------------------|-----------------|---------------------------------|
| | Read or Output Disable | A ₁₄ - A ₀ | E, E _S | CP | ALE | O ₇ - O ₀ |
| | Other | A ₁₄ - A ₀ | VFY | PGM | V _{PP} | D ₇ - D ₀ |
| Read | | A ₁₄ - A ₀ | V _{IL} | V _{IH} | V _{IL} | O ₇ - O ₀ |
| Output Disable | | A ₁₄ - A ₀ | V _{IH} | X | X | High Z |
| Program | | A ₁₄ - A ₀ | V _{IHP} | V _{ILP} | V _{PP} | D ₇ - D ₀ |
| Program Verify | | A ₁₄ - A ₀ | V _{ILP} | V _{IHP} /V _{ILP} | V _{PP} | O ₇ - O ₀ |
| Program Inhibit | | A ₁₄ - A ₀ | V _{IHP} | V _{IHP} | V _{PP} | High Z |
| Blank Check | | A ₁₄ - A ₀ | V _{ILP} | V _{IHP} /V _{ILP} | V _{PP} | O ₇ - O ₀ |

Notes:

10. X = "don't care" but not to exceed V_{CC} ±5%.

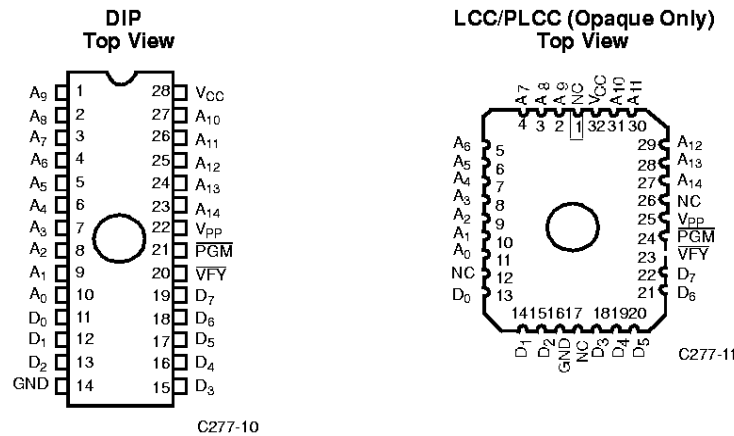
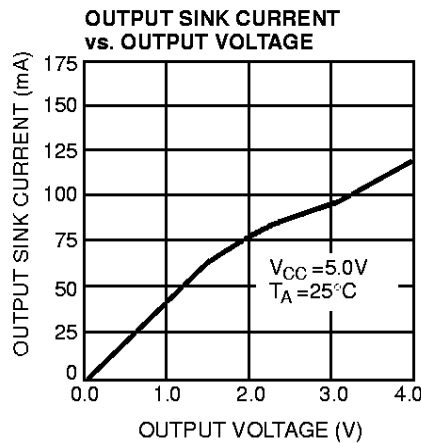
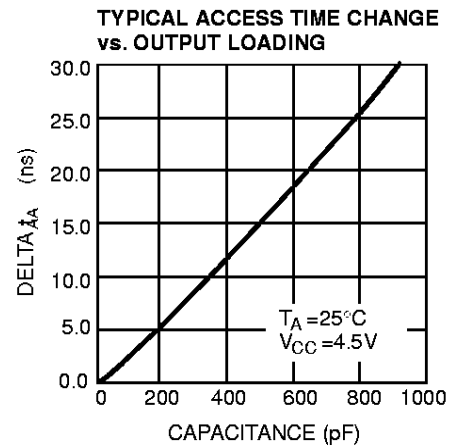
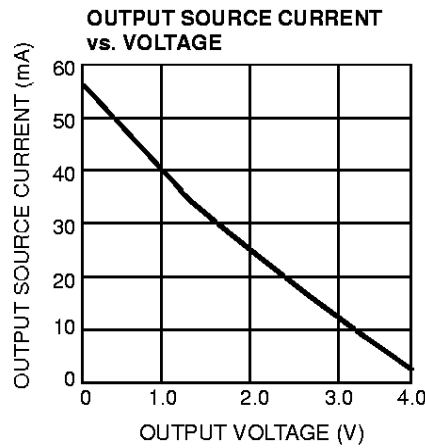
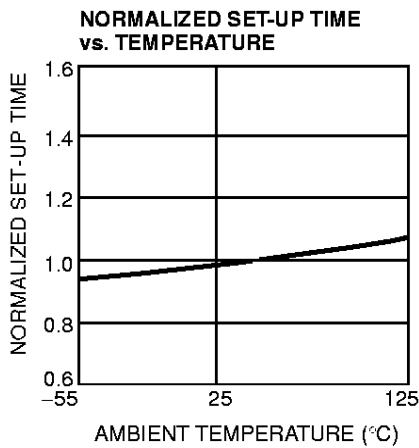
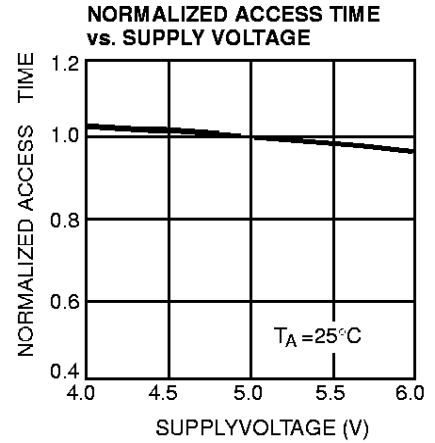
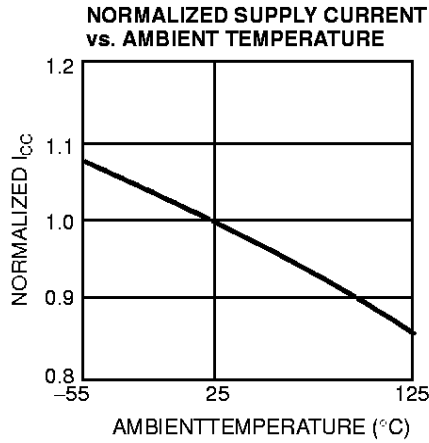
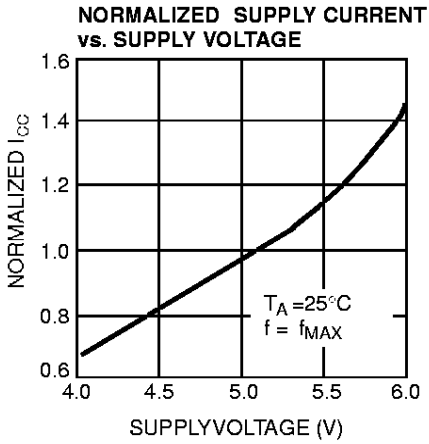


Figure 1. Programming Pinouts

Typical DC and AC Characteristics


Ordering Information^[11]

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---------------|---------------|-----------------------------------|---|-----------------|
| 30 | CY7C277-30JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C277-30PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C277-30WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 40 | CY7C277-40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C277-40PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C277-40WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| | CY7C277-40DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C277-40KMB | K74 | 28-Lead Rectangular Cerpack | |
| | CY7C277-40LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| | CY7C277-40QMB | Q55 | 32-Pin Windowed Rectangular Leadless Chip Carrier | |
| | CY7C277-40TMB | T74 | 28-Lead Windowed Cerpack | |
| | CY7C277-40WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| 50 | CY7C277-50JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C277-50PC | P21 | 28-Lead (300-Mil) Molded DIP | |
| | CY7C277-50WC | W22 | 28-Lead (300-Mil) Windowed CerDIP | |
| | CY7C277-50DMB | D22 | 28-Lead (300-Mil) CerDIP | Military |
| | CY7C277-50KMB | K74 | 28-Lead Rectangular Cerpack | |
| | CY7C277-50LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| | CY7C277-50QMB | Q55 | 32-Pin Windowed Rectangular Leadless Chip Carrier | |
| | CY7C277-50TMB | T74 | 28-Lead Windowed Cerpack | |
| CY7C277-50WMB | W22 | 28-Lead (300-Mil) Windowed CerDIP | | |

Notes:

11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

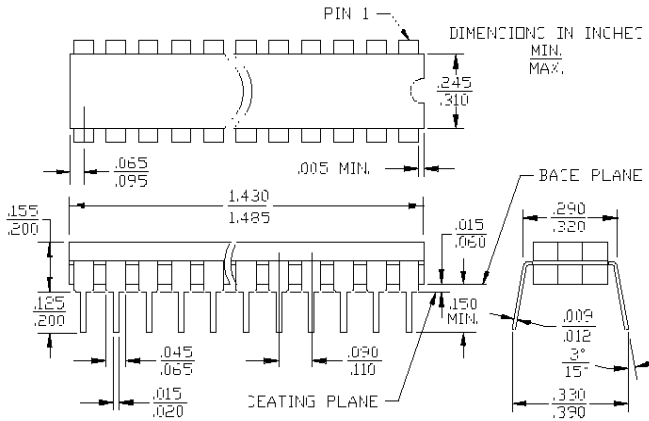
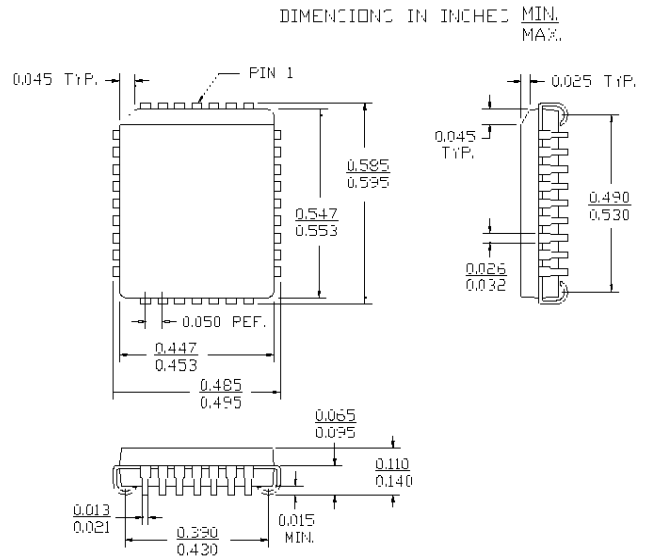
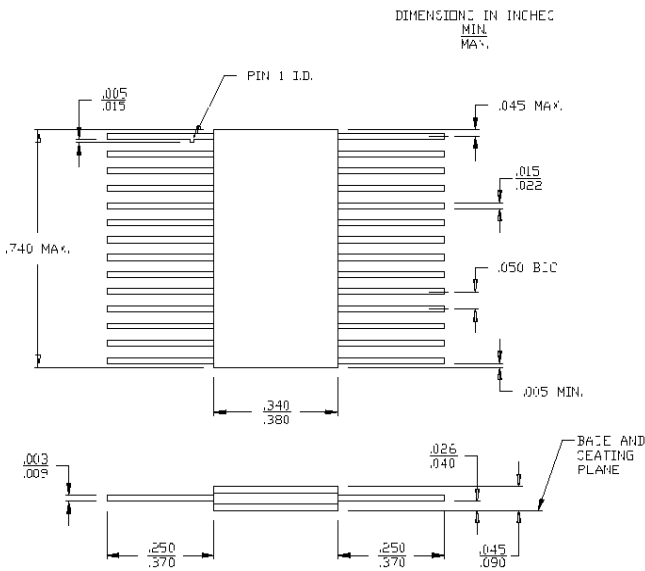
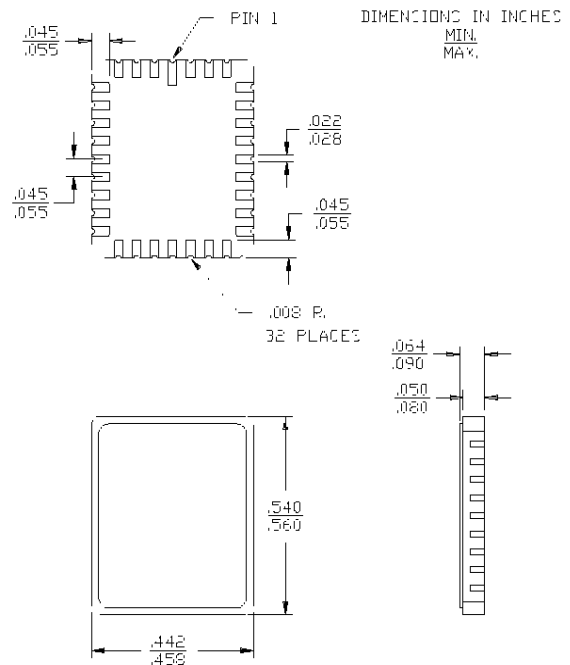
**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

| Parameter | Subgroups |
|-----------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OZ} | 1, 2, 3 |
| I_{CC} | 1, 2, 3 |

Switching Characteristics

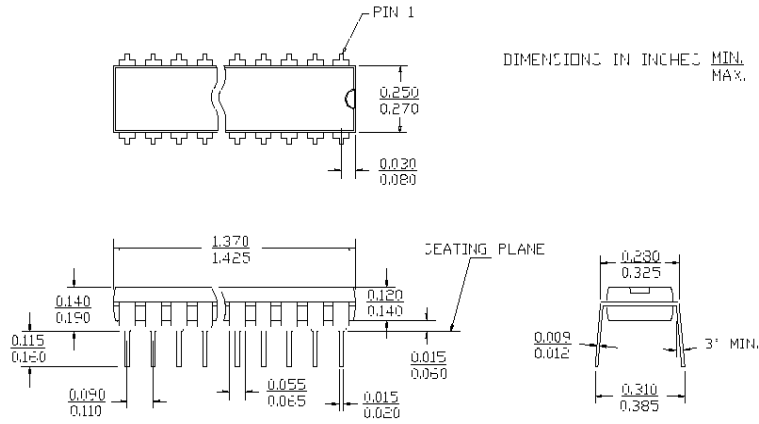
| Parameter | Subgroups |
|-----------|-----------------|
| t_{SA} | 7, 8, 9, 10, 11 |
| t_{HA} | 7, 8, 9, 10, 11 |
| t_{CO} | 7, 8, 9, 10, 11 |

Document #: 38-00085-E

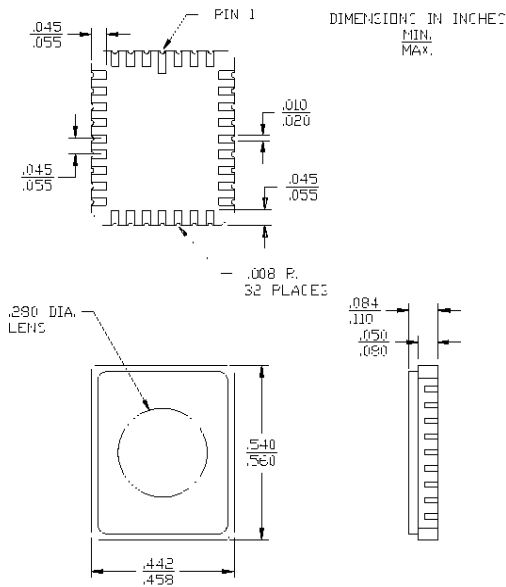
Package Diagrams
28-Lead (300-Mil) CerDIP D22
 MIL-STD-1835 D-15 Config.A

32-Lead Plastic Leaded Chip Carrier J65

28-Lead Rectangular Cerpack K74
 MIL-STD-1835 F-11 Config.A

32-Pin Rectangular Leadless Chip Carrier L55
 MIL-STD-1835 C-12


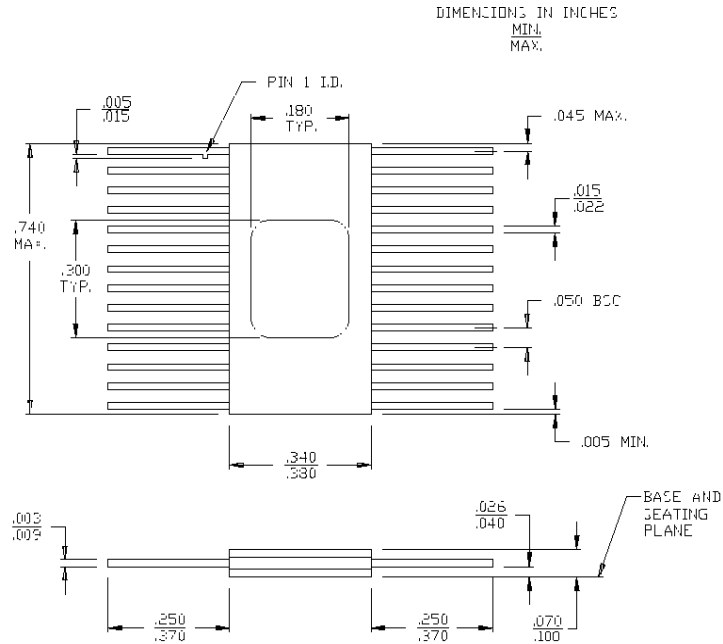
Package Diagrams (Continued)

28-Lead (300-Mil) Molded DIP P21



32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL-STD-1835 C-12



Package Diagrams (Continued)
28-Lead Windowed Cerpack T74

28-Lead (300-Mil) Windowed CerDIP W22
 MIL-STD-1835 D-15 Config.A
