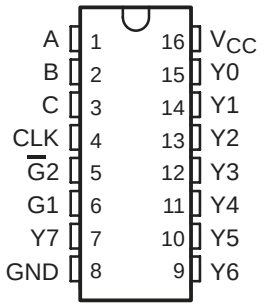
- **Combines Decoder and 3-Bit Address Register**
- **Incorporates Two Enable Inputs to Simplify Cascading**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74AS131A is a 3-line to 8-line decoder/demultiplexer with registers on the three address inputs. When the clock (CLK) input goes from low to high, the device acts as a decoder/demultiplexer and the address present at the select (A, B, and C) inputs is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output-enable (G1, $\overline{G}2$) inputs control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G}2$ is low. This device is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN74AS131A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLK | ENABLE | | SELECT | | | | | | | | | | |
| | G1 | $\overline{G}2$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| ↑ | H | L | L | L | L | L | H | H | H | H | H | H | H |
| ↑ | H | L | L | L | H | H | L | H | H | H | H | H | H |
| ↑ | H | L | L | H | L | H | H | L | H | H | H | H | H |
| ↑ | H | L | L | H | H | H | H | H | L | H | H | H | H |
| ↑ | H | L | H | L | L | H | H | H | H | L | H | H | H |
| ↑ | H | L | H | L | H | H | H | H | H | H | L | H | H |
| ↑ | H | L | H | H | L | H | H | H | H | H | H | L | H |
| ↑ | H | L | H | H | H | H | H | H | H | H | H | H | L |
| L or H | H | L | X | X | X | Outputs corresponding to stored address = L; all others = H. | | | | | | | |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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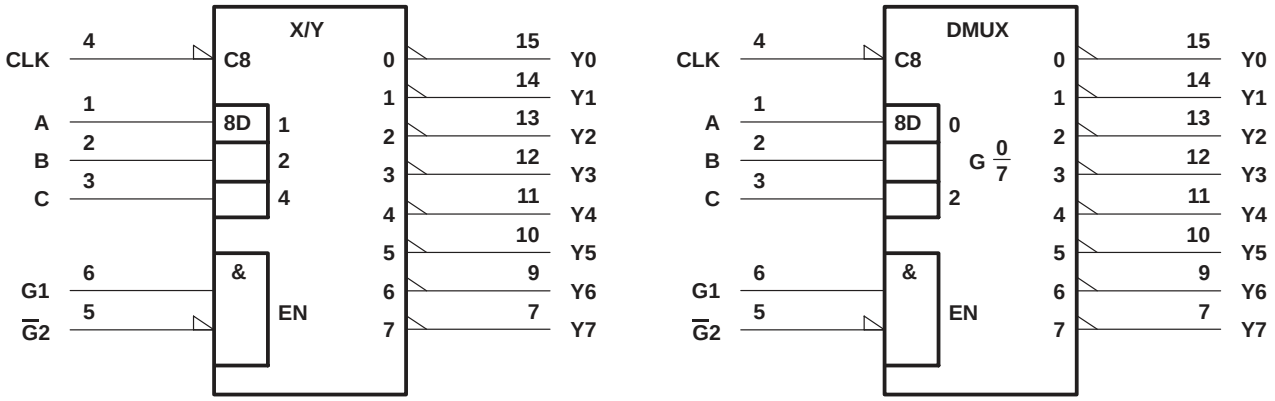
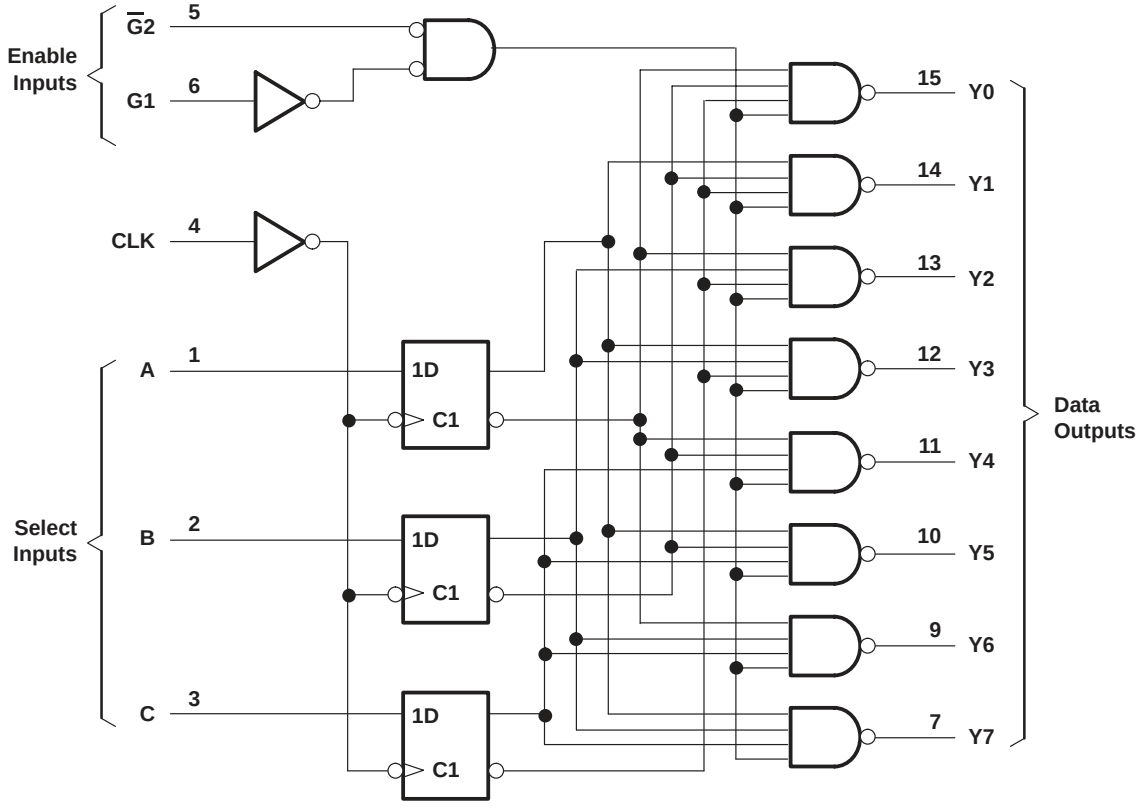
## logic symbols (alternatives)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)






TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −2 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 100 | MHz |
| $t_w$ | Pulse duration | CLK high | 5 | | | ns |
| | | CLK low | 5 | | | |
| $t_{su}$ | Setup time, A, B, and C before CLK↑ | | 3.5 | | | ns |
| $t_h$ | Hold time, A, B, and C after CLK↑ | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.35 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | mA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V | | | 15 | 29 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V | | | 16 | 30 | mA |

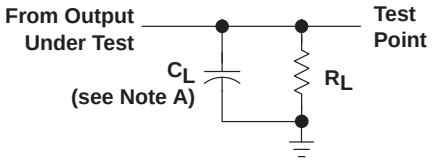
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

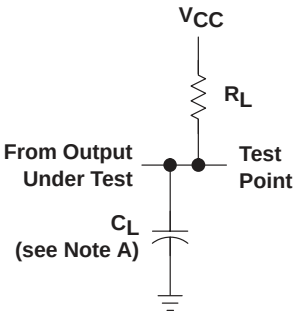
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | | | 100 | | MHz |
| $t_{PLH}$ | CLK | Y | 2 | 14.5 | ns |
| $t_{PHL}$ | | | 2 | 9.5 | |
| $t_{PLH}$ | G1 | Y | 2 | 10 | ns |
| $t_{PHL}$ | | | 2 | 9 | |
| $t_{PLH}$ | $\overline{G}2$ | Y | 2 | 7 | ns |
| $t_{PHL}$ | | | 2 | 8.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

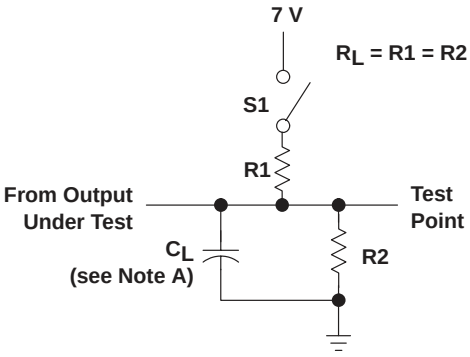
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



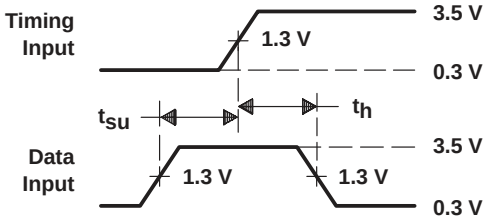

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



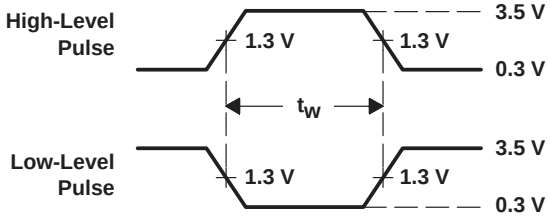

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



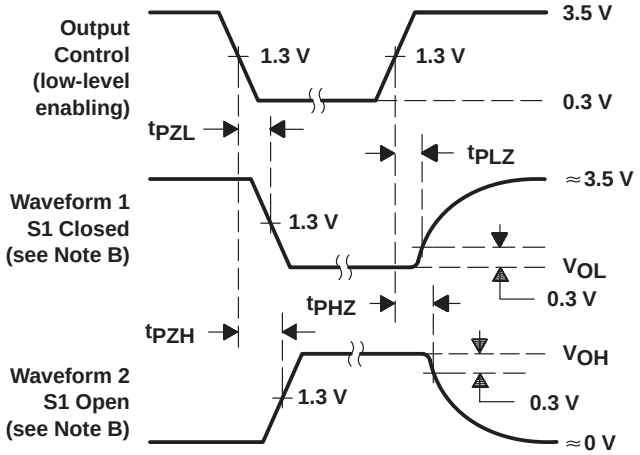

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



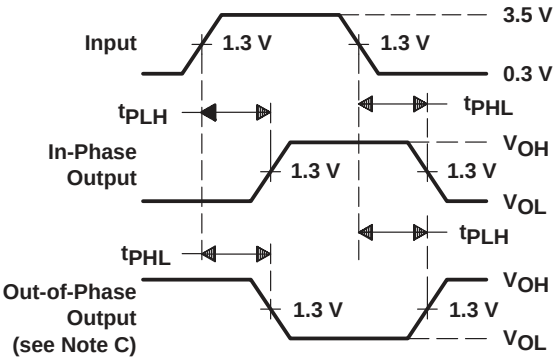

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74AS131AD | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74AS131ADR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74AS131AN | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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