MIC24053

12V, 9A High-Efficiency Buck Regulator with Hyper Speed Control

Features

- Hyper Speed Control® Architecture Enables:
  - High Delta V Operation (V_{IN} = 19V and V_{OUT} = 0.8V)
  - Small Output Capacitance
- 4.5V to 19V Voltage Input
- 9A Output Current Capability, Up to 95% Efficiency
- Adjustable Output from 0.8V to 5.5V
- ±1% Feedback Accuracy
- Any Capacitor Stable-Zero-to-High ESR
- 600 kHz Switching Frequency
- No External Compensation
- Power Good (PG) Output
- Foldback Current-Limit and "Hiccup Mode" Short-Circuit Protection
- Supports Safe Startup into a Pre-Biased Load
- –40°C to +125°C Junction Temperature Range
- Available in 28-pin 5 mm x 6 mm QFN Package

Applications

- Servers, Workstations
- Routers, Switches, and Telecom Equipment
- Base Stations

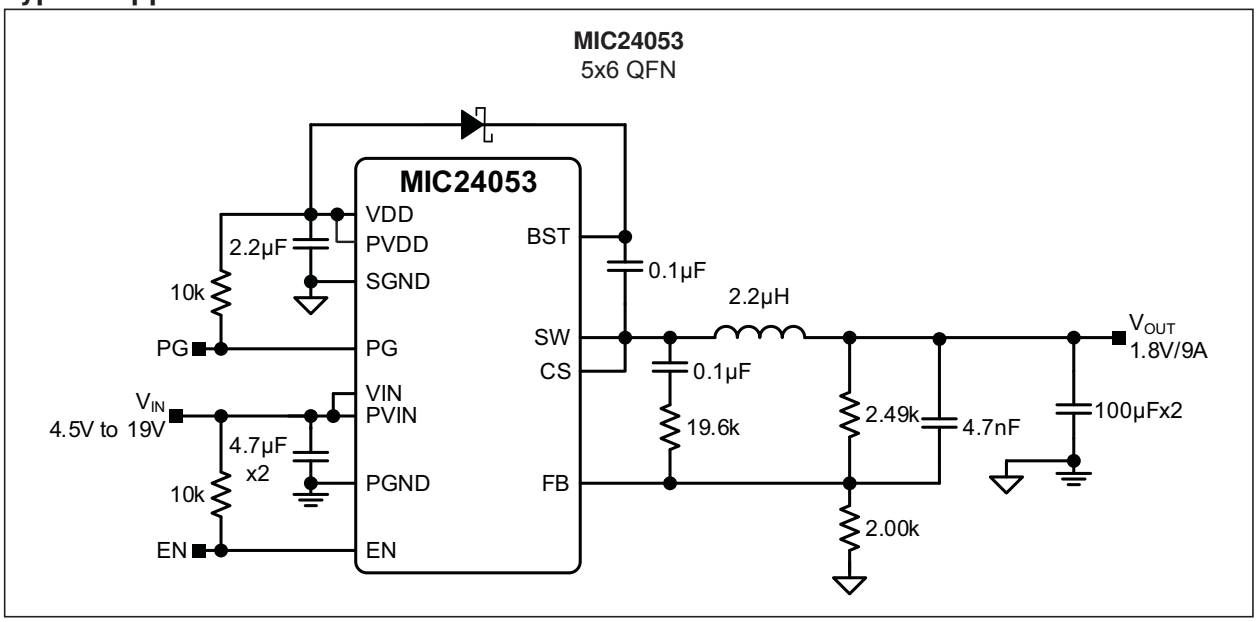
General Description

The MIC24053 is a constant-frequency, synchronous buck regulator featuring a unique adaptive on-time control architecture. The MIC24053 operates over an input supply range of 4.5V to 19V and provides a regulated output of up to 9A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%, and the device operates at a switching frequency of 600 kHz.

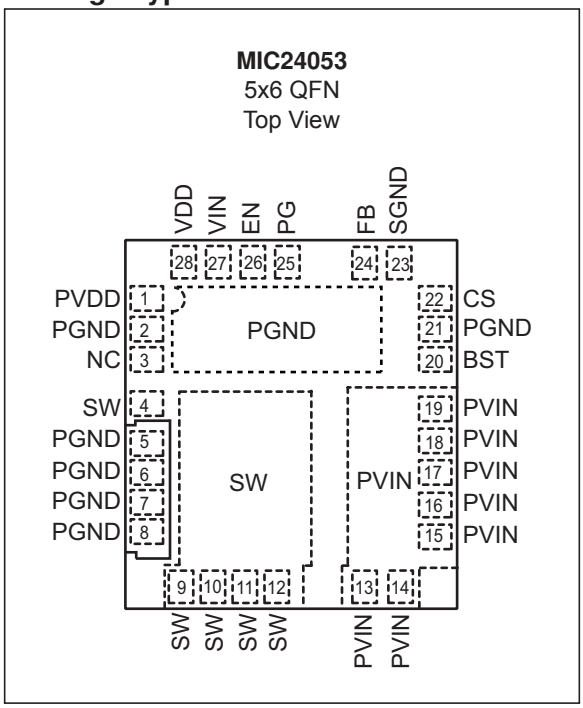
The Hyper Speed Control® architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High V_{IN})/(Low V_{OUT}) operation possible. This adaptive t_{ON} ripple control architecture combines the advantages of fixed-frequency operation and fast transient response in a single device.

The MIC24053 offers a full suite of features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, foldback current limit, "hiccup mode" short-circuit protection, and thermal shutdown. An open-drain Power Good (PG) pin is provided. pin is provided.

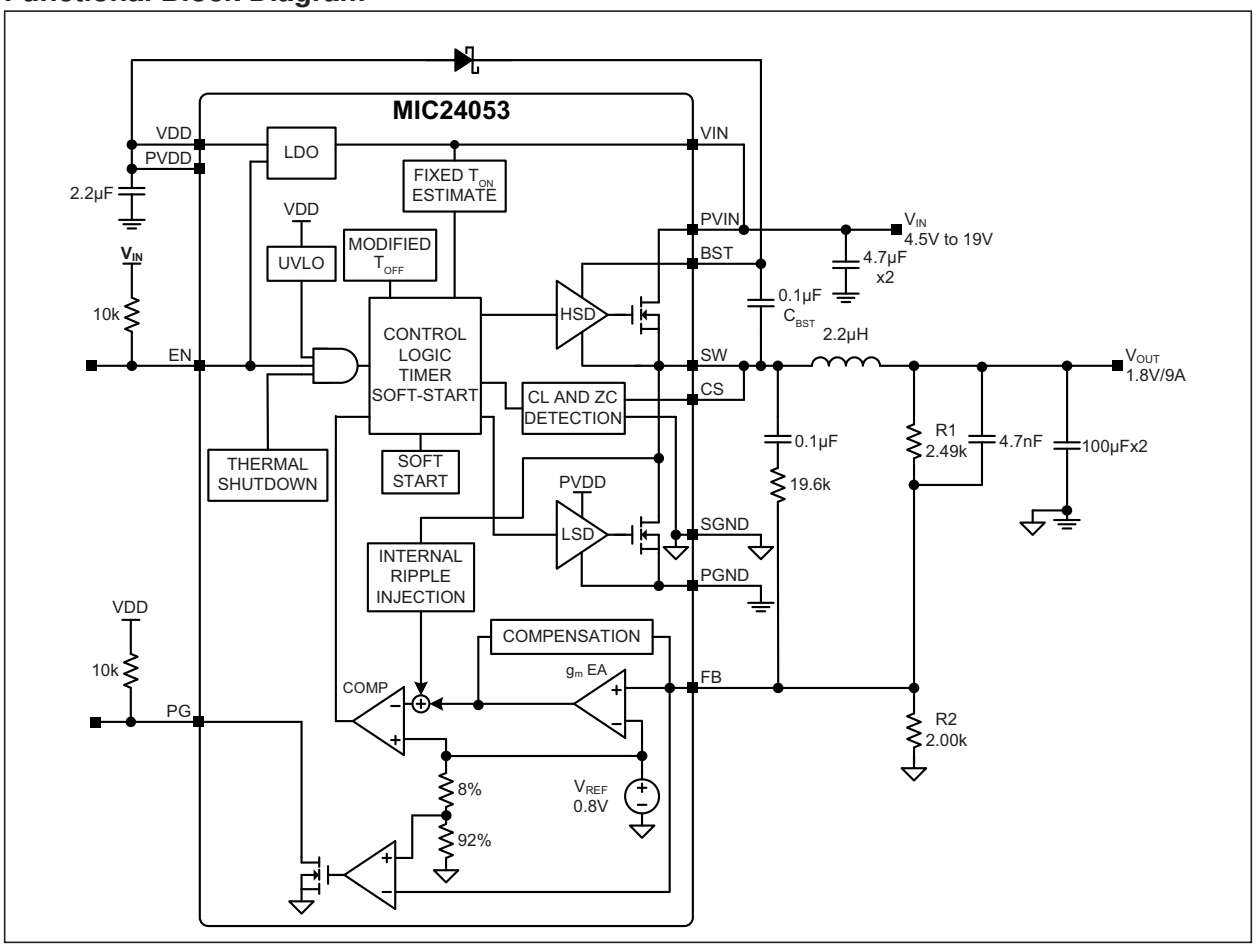
Typical Application Circuit



Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PV_{IN} to PGND ..... –0.3V to +29V
V_{IN} to PGND ..... –0.3V to PV_{IN}
PV_{DD}, V_{DD} to PGND ..... –0.3V to +6V
V_{SW}, V_{CS} to PGND ..... –0.3V to (PV_{IN} +0.3V)
V_{BST} to V_{SW} ..... –0.3V to 6V
V_{BST} to PGND ..... –0.3V to 35V
V_{FB}, V_{PG} to PGND ..... –0.3V to (V_{DD} + 0.3V)
V_{EN} to PGND ..... –0.3V to (V_{IN} +0.3V)
PGND to SGND ..... –0.3V to +0.3V
ESD Rating (Note 1). ..... ESD Sensitive

Operating Ratings ††

Supply Voltage (PV_{IN}, V_{IN}) ..... 4.5V to 19V
PV_{DD}, V_{DD} Supply Voltage (PV_{DD}, V_{DD}) ..... 4.5V to 5.5V
Enable Input (V_{EN}) ..... 0V to V_{IN}
Maximum Power Dissipation ..... Note 2

† Notice: Exceeding the absolute maximum rating can damage the device.

†† Notice: The device is not guaranteed to function outside its operating range.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

2: $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\Theta_{JA}$, where Θ_{JA} depends on the printed circuit layout. A 5 in^2, 4-layer, 0.62”, FR-4 PCB with 2 oz finish copper weight per layer is used for the Θ_{JA}.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $PV_{IN} = V_{IN} = V_{EN}$ = 12V, $V_{BST} – V_{SW}$ = 5V; T_A = 25°C. Bold values indicate –40°C ≤ T_J ≤ +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range (V_{IN}, PV_{IN})		**4.5**	—	**19**	V	—
Quiescent Supply Current		—	730	**1500**	µA	V_{FB} = 1.5V (non-switching)
Shutdown Supply Current		—	5	**10**	µA	V_{EN} = 0V
V_{DD} Supply Voltage						
V_{DD} Output Voltage		**4.8**	5	**5.4**	V	V_{IN} = 7V to 19V, I_{DD} = 40 mA
V_{DD} UVLO Threshold		**3.7**	4.2	**4.5**	V	V_{DD} Rising
V_{DD} UVLO Hysteresis		—	400	—	mV	—
Dropout Voltage ($V_{IN} – V_{DD}$)		—	380	**600**	mV	I_{DD} = 25 mA
DC - DC Controller						
Output-Voltage Adjust Range (V_{OUT})		0.8	—	**5.5**	V	—

Note 1: Specification for packaged product only.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time (t_{OFF}) of typically 300 ns.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $PV_{IN} = V_{IN} = V_{EN}$ = 12V, $V_{BST} – V_{SW}$ = 5V; T_A = 25°C. Bold values indicate –40°C ≤ T_J ≤ +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Reference						
Feedback Reference Voltage		**0.792**	0.8	**0.808**	V	0°C ≤ T_J ≤ 85°C (±1.0%)
		0.788	0.8	**0.812**		–40°C ≤ T_J ≤ 125°C (±1.5%)
Load Regulation		—	0.25	—	%	I_{OUT} = 0A to 9A (Continuous Mode)
Line Regulation		—	0.25	—	%	V_{IN} = 4.5V to 19V
FB Bias Current		—	50	—	nA	V_{FB} = 0.8V
Enable Control						
EN Logic Level High		**1.8**	—	—	V	—
EN Logic Level Low		—	—	**0.6**	V	—
EN Bias Current		—	6	**30**	µA	V_{EN} = 12V
Oscillator						
Switching Frequency (Note 2)		**450**	600	**750**	kHz	V_{OUT} = 2.5V
Maximum Duty Cycle (Note 3)		—	82	—	%	V_{FB} = 0V
Minimum Duty Cycle		—	0	—	%	V_{FB} = 1.0V
Minimum Off-Time		—	300	—	ns	—
Soft-Start						
Soft-Start Time		—	3	—	ms	—
Short-Circuit Protection						
Peak Inductor Current-Limit Threshold		12.5	14	20	A	V_{FB} = 0.8V, T_J = 25°C
		11.25	14	20	A	V_{FB} = 0.8V, T_J = 125°C
Short-Circuit Current		—	8	—	A	V_{FB} = 0V
Internal FETs						
Top-MOSFET $R_{DS(ON)}$		—	27	—	mΩ	I_{SW} = 3A
Bottom-MOSFET $R_{DS(ON)}$		—	10.5	—	mΩ	I_{SW} = 3A
SW Leakage Current		—	—	**60**	µA	V_{EN} = 0V
V_{IN} Leakage Current		—	—	**25**	µA	V_{EN} = 0V
Power Good (PG)						
PG Threshold Voltage		85	92	95	%V_{OUT}	Sweep V_{FB} from Low to High
PG Hysteresis		—	5.5	—	%V_{OUT}	Sweep V_{FB} from High to Low
PG Delay Time		—	100	—	µs	Sweep V_{FB} from Low to High
PG Low Voltage		—	70	200	mV	Sweep $V_{FB} < 0.9 \times V_{NOM}$, I_{PG} = 1 mA

Note 1: Specification for packaged product only.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time (t_{OFF}) of typically 300 ns.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $PV_{IN} = V_{IN} = V_{EN} = 12V$, $V_{BST} – V_{SW} = 5V$; $T_A = 25°C$. Bold values indicate $–40°C \le T_J \le +125°C$

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Thermal Protection						
Overtemperature Shutdown		—	160	—	°C	T_J Rising
Overtemperature Shutdown Hysteresis		—	15	—	°C	—

Note 1: Specification for packaged product only.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time (t_{OFF}) of typically 300 ns.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	—	—	—	+150	°C	—
Junction Operating Temperature	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	260	—	°C	Soldering, 10s
Package Thermal Resistances (Note 1)						
Thermal Resistance, 5 x 6 QFN-28Ld	θ_{JA}	—	28	—	°C/W	—

Note 1: $P_{D(MAX)} = (T_{J(MAX)} – TA)/\Theta J_A$, where ΘJ_A depends on the printed circuit layout. A $5in^2$, 4-layer, 0.62”, FR-4 PCB with 2 oz finish copper weight per layer is used for the Θ_{JA}.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

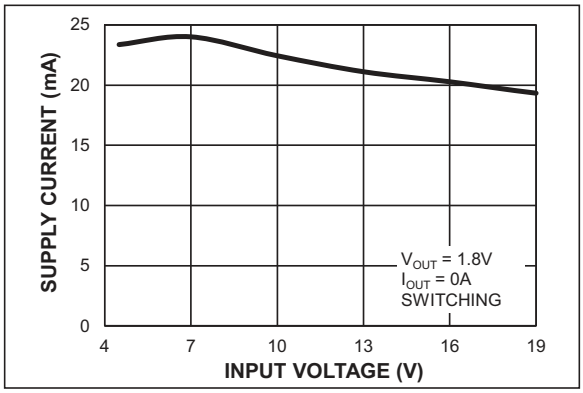


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage.*

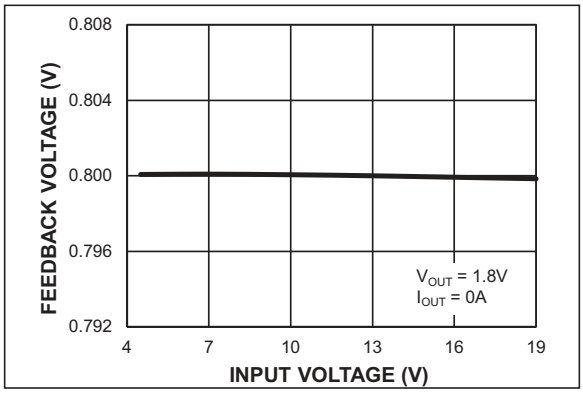


FIGURE 2-4: *Feedback Voltage vs. Input Voltage.*

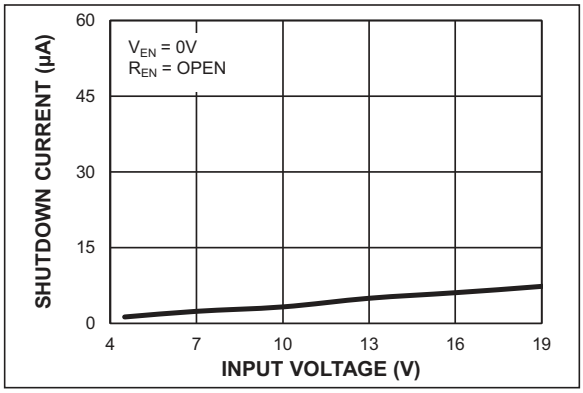


FIGURE 2-2: *V_{IN} Shutdown Current vs. Input Voltage.*

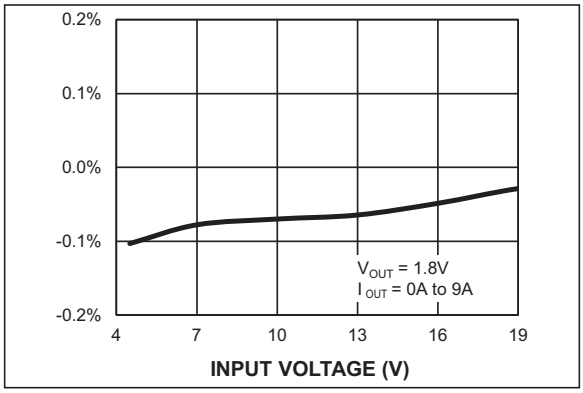


FIGURE 2-5: *Total Regulation vs. Input Voltage.*

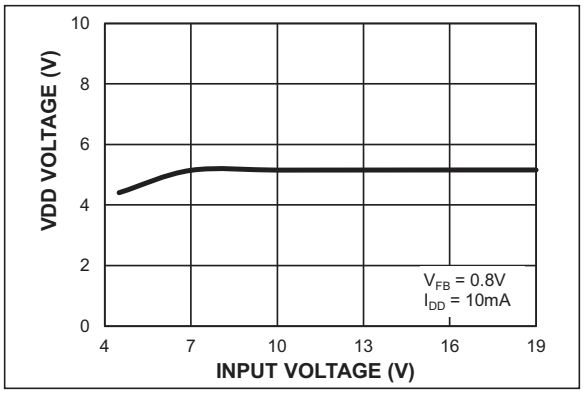


FIGURE 2-3: *V_{DD} Output Voltage vs. Input Voltage.*

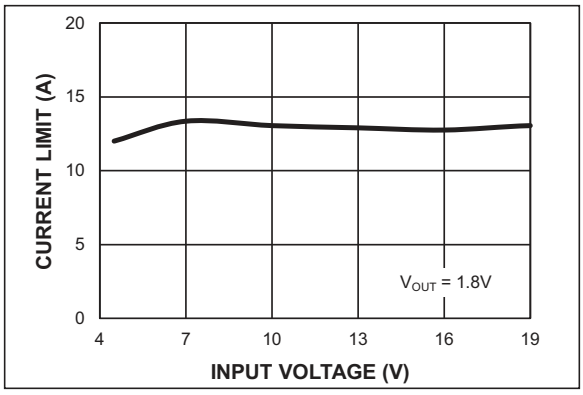


FIGURE 2-6: *Output Current Limit vs. Input Voltage.*

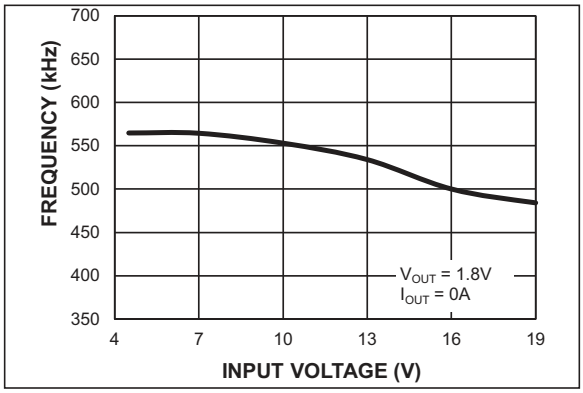


FIGURE 2-7: *Switch Frequency vs. Input Voltage.*

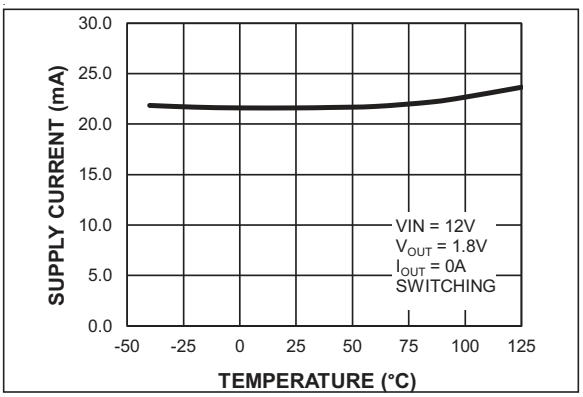


FIGURE 2-10: *V_{IN} Operating Supply Current vs. Temperature.*

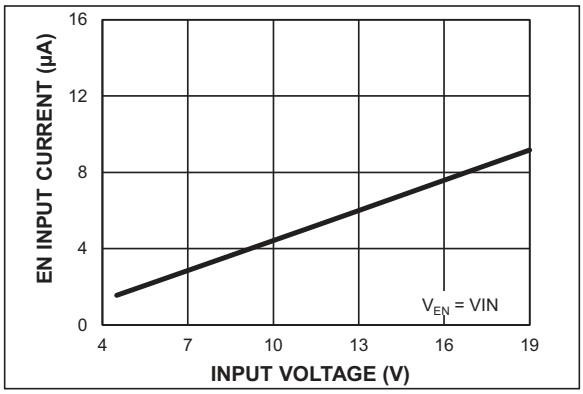


FIGURE 2-8: *Enable Input Current vs. Input Voltage.*

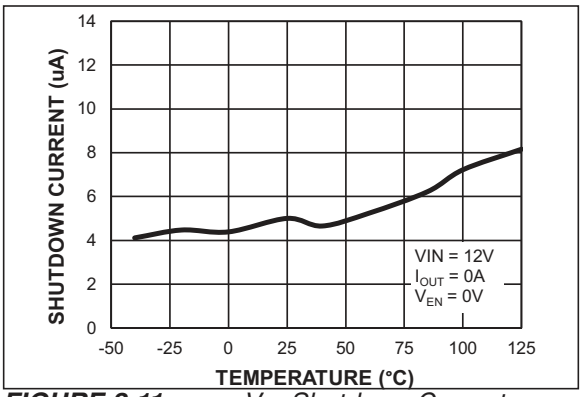


FIGURE 2-11: *V_{IN} Shutdown Current vs. Temperature.*

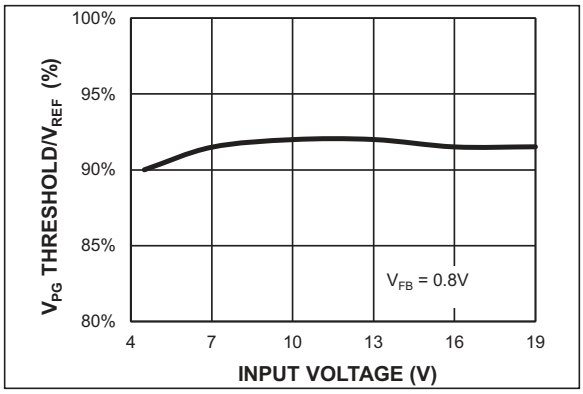


FIGURE 2-9: *PG/V_{REF} Ratio vs. Input Voltage.*

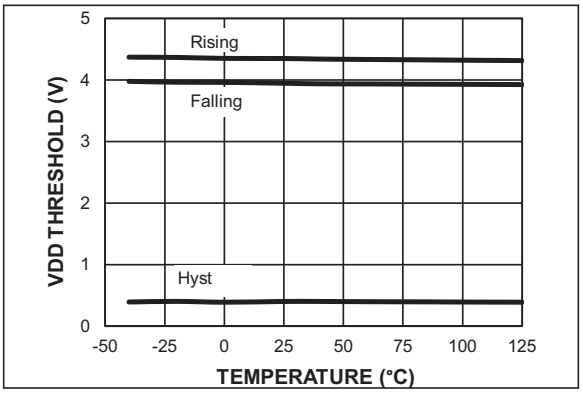


FIGURE 2-12: *V_{DD} UVLO Threshold vs. Temperature.*

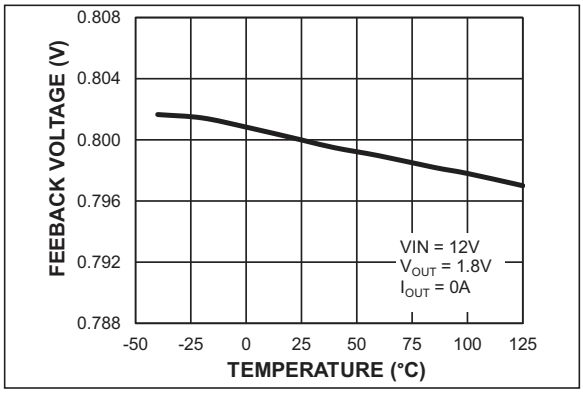


FIGURE 2-13: *Feedback Voltage vs. Temperature.*

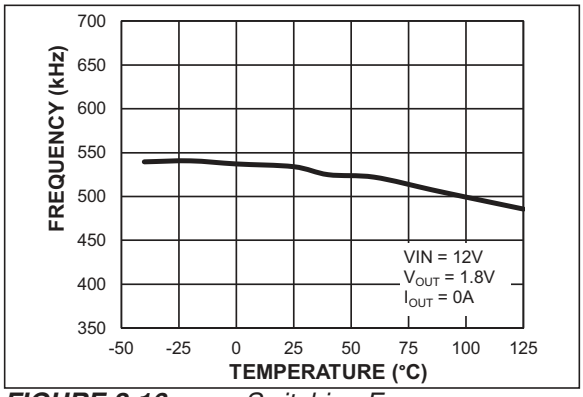


FIGURE 2-16: *Switching Frequency vs. Temperature.*

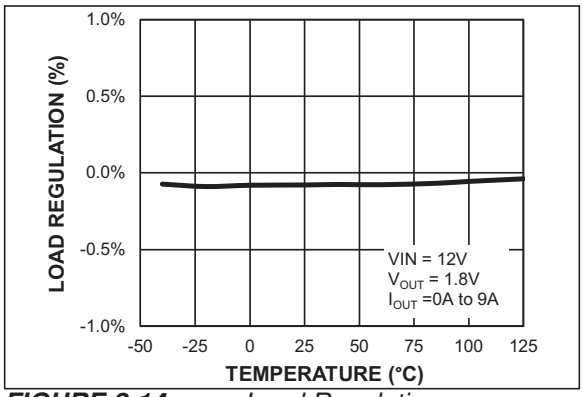


FIGURE 2-14: *Load Regulation vs. Temperature.*

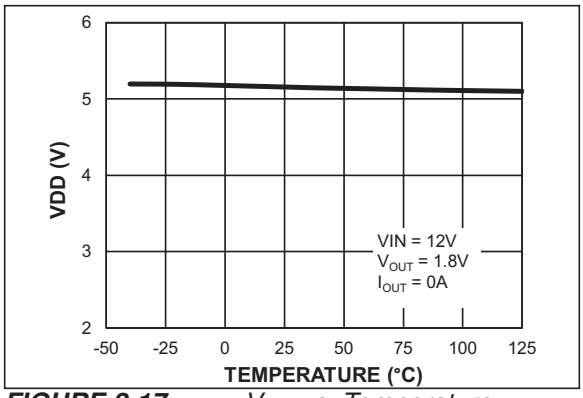


FIGURE 2-17: *V_{DD} vs. Temperature.*

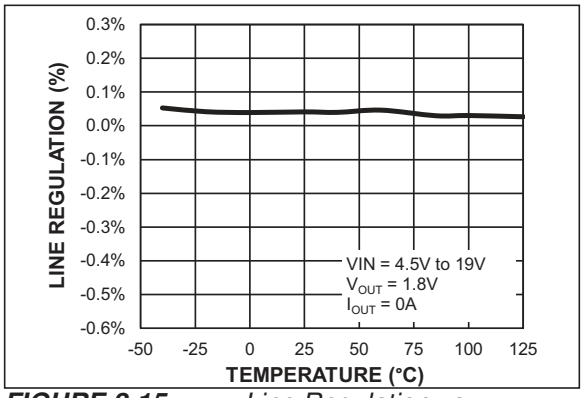


FIGURE 2-15: *Line Regulation vs. Temperature.*

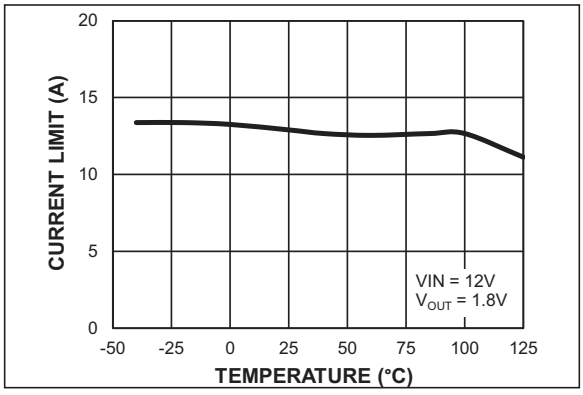


FIGURE 2-18: *Output Current Limit vs. Temperature.*

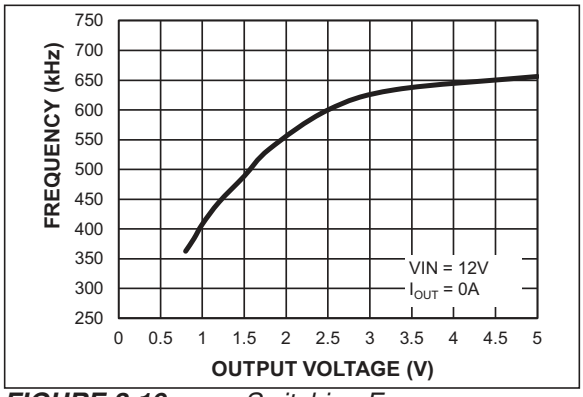


FIGURE 2-19: *Switching Frequency vs. Output Voltage.*

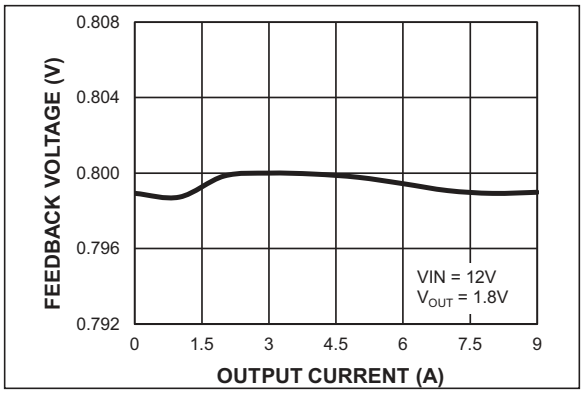


FIGURE 2-20: *Feedback Voltage vs. Output Current.*

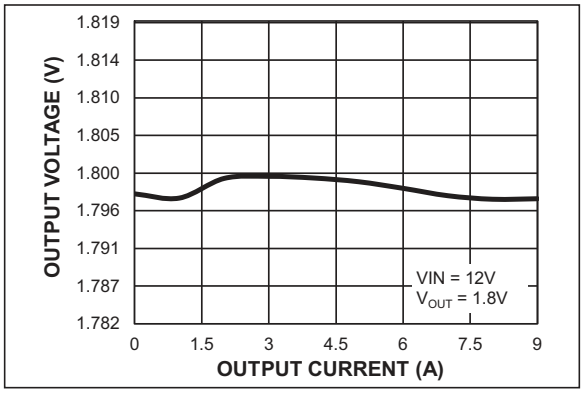


FIGURE 2-21: *Output Voltage vs. Output Current.*

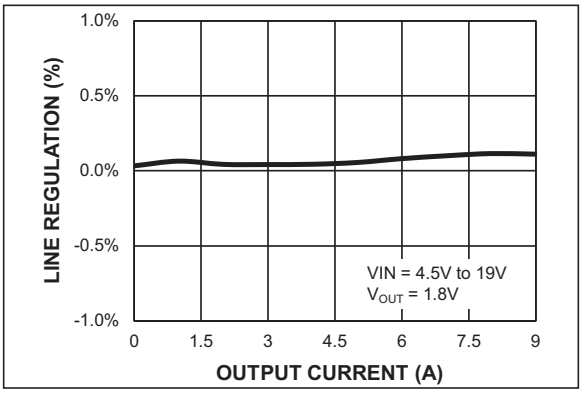


FIGURE 2-22: *Line Regulation vs. Output Current.*

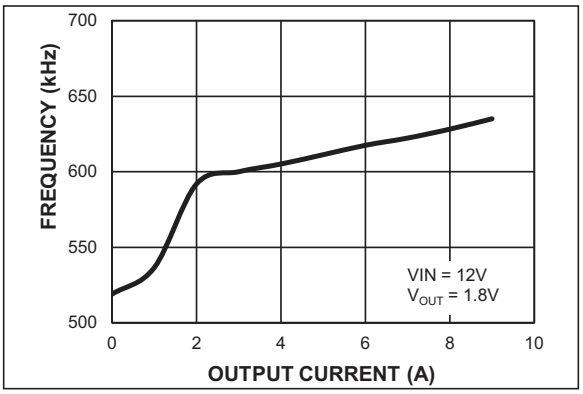


FIGURE 2-23: *Switching Frequency vs. Output Current.*

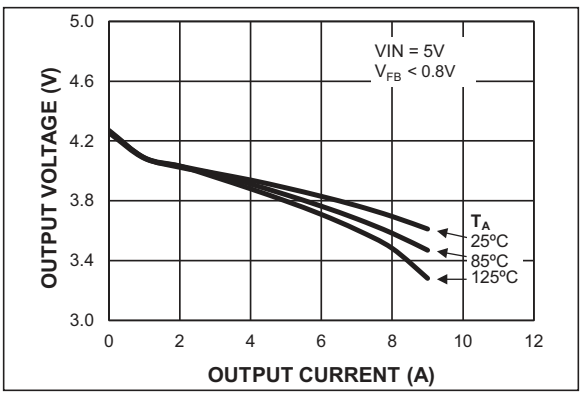


FIGURE 2-24: *Output Voltage (V_{IN} = 5V) vs. Output Current.*

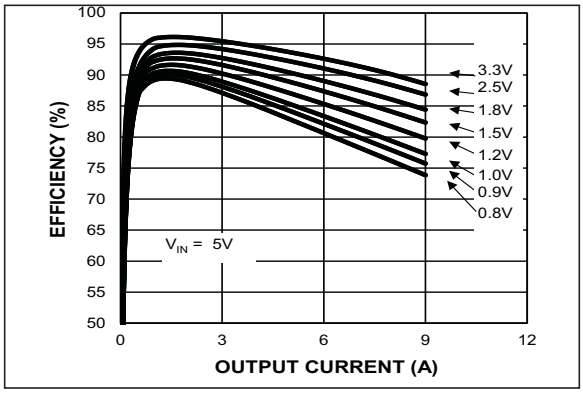


FIGURE 2-25: *Efficiency (V_{IN} = 5V) vs. Output Current.*

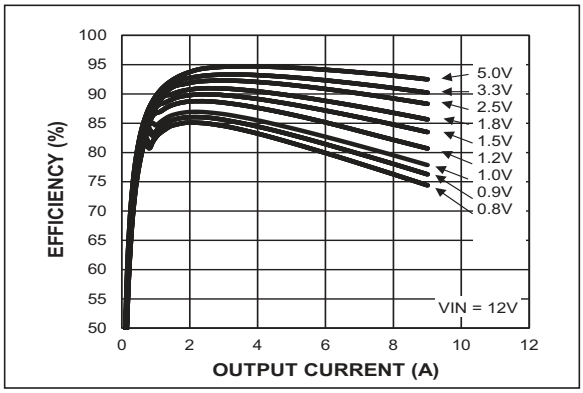


FIGURE 2-28: *Efficiency (V_{IN} = 12V) vs. Output Current.*

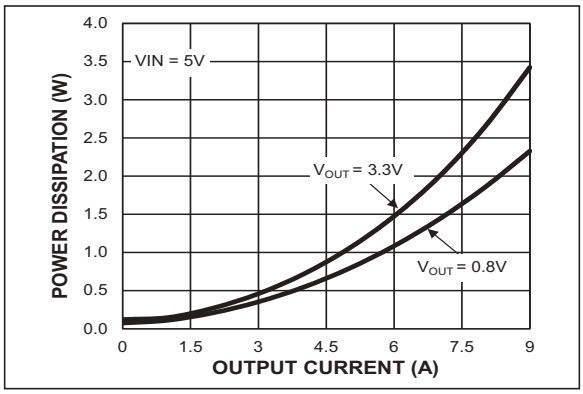


FIGURE 2-26: *IC Power Dissipation (V_{IN} = 5V) vs. Output Current.*

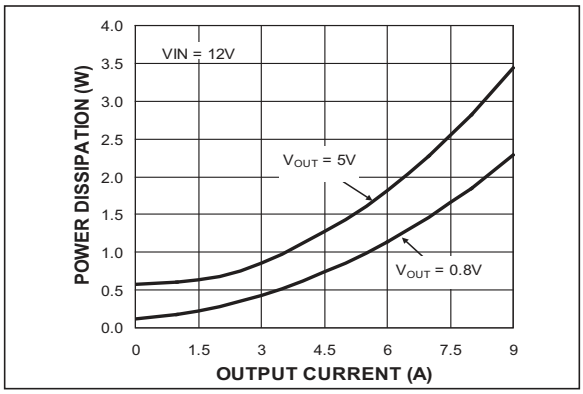


FIGURE 2-29: *IC Power Dissipation (V_{IN} = 12V) vs. Output Current.*

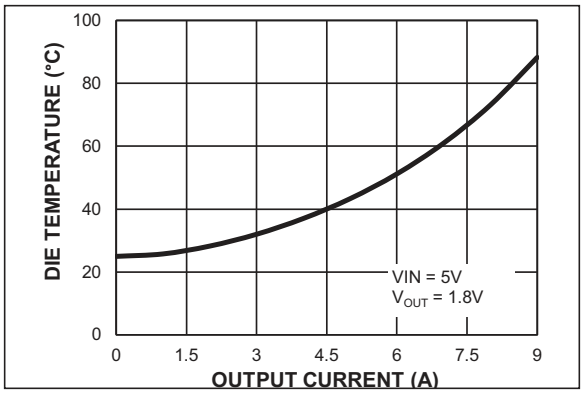


FIGURE 2-27: *Die Temperature (V_{IN} = 5V) vs. Output Current (Note 1).*

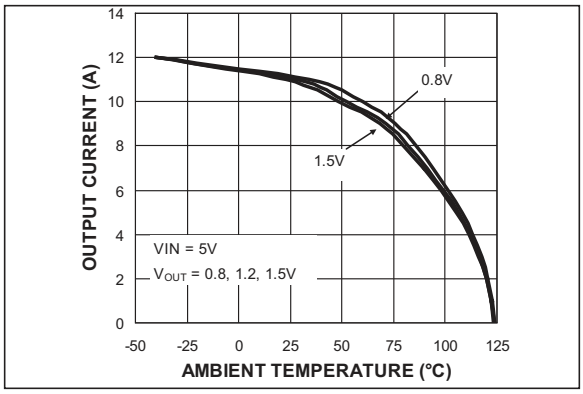


FIGURE 2-30: *Thermal Derating vs. Ambient Temperature (Note 1).*

Note 1: Die Temperature: The temperature measurement was taken at the hottest point on the MIC24053 case mounted on a 5in^2, 4 layer, 0.62”, FR-4 PCB with 2oz finish copper weight per layer; see the Thermal Measurements section. Actual results depend on the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

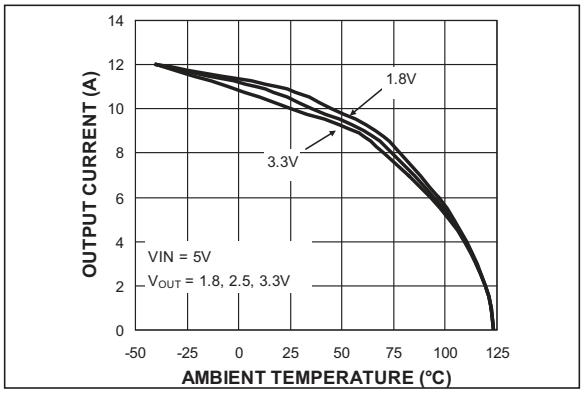


FIGURE 2-31: *Thermal Derating vs. Ambient Temperature (Note 1).*

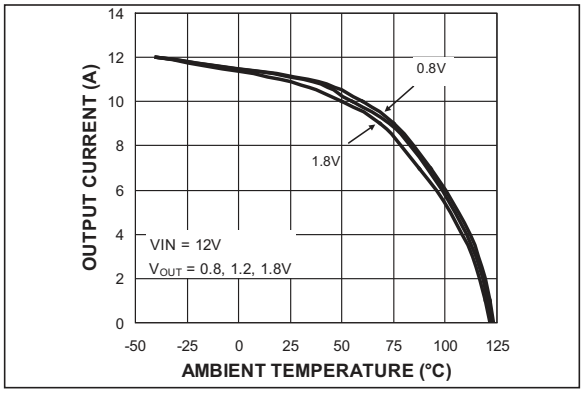


FIGURE 2-32: *Thermal Derating vs. Ambient Temperature (Note 1).*

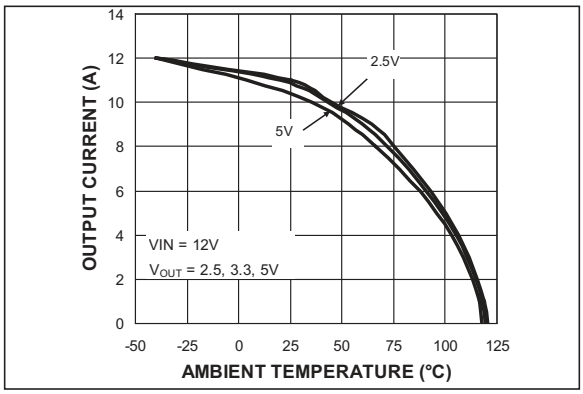


FIGURE 2-33: *Thermal Derating vs. Ambient Temperature (Note 1).*

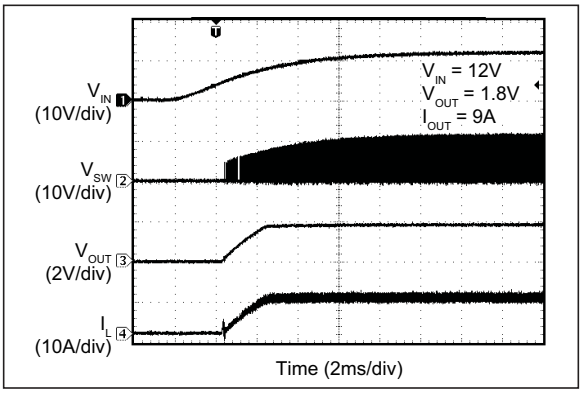


FIGURE 2-34: *V_{IN} Soft Turn-On.*

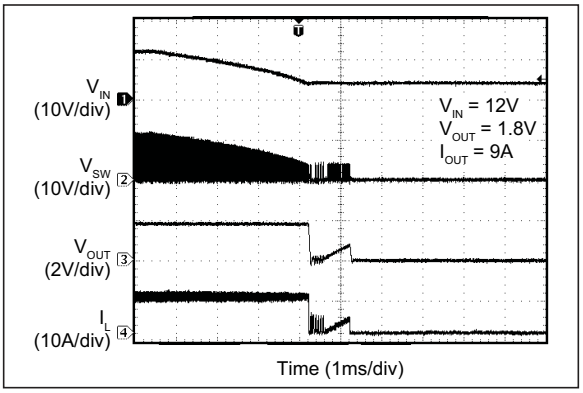


FIGURE 2-35: *V_{IN} Soft Turn-Off.*

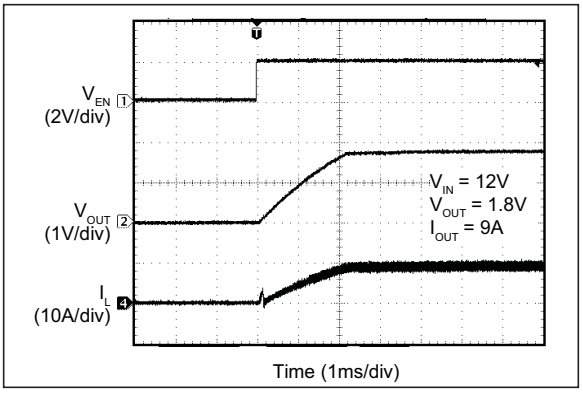


FIGURE 2-36: *Enable Turn-On Delay and Rise Time.*

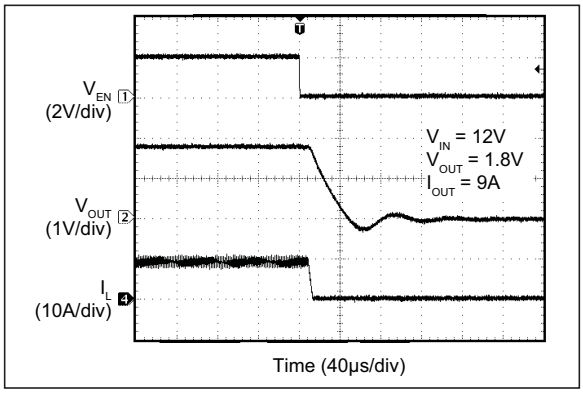


FIGURE 2-37: *Enable Turn-Off Delay and Fall Time.*

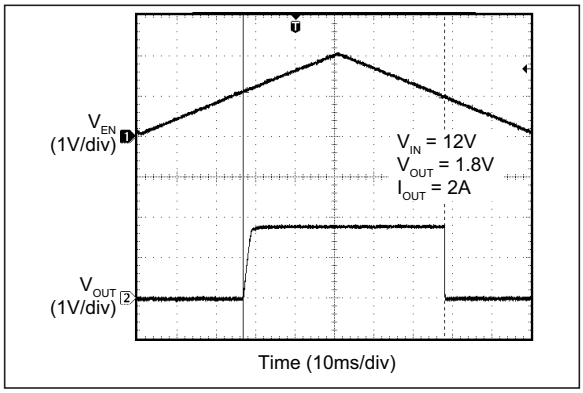


FIGURE 2-40: *Enable Thresholds.*

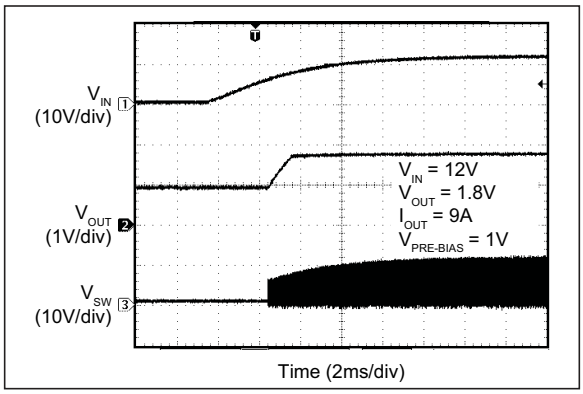


FIGURE 2-38: *V_{IN} Start-Up with Pre-Biased Output.*

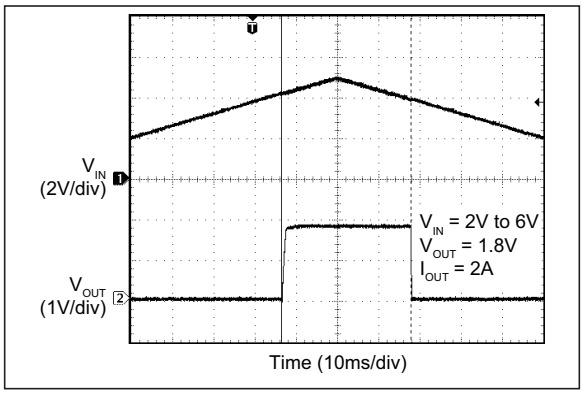


FIGURE 2-41: *V_{IN} UVLO Thresholds.*

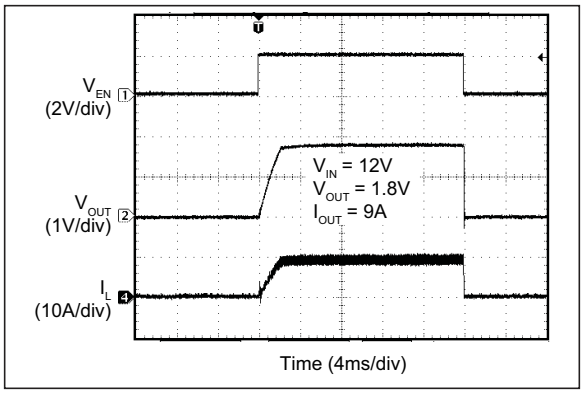


FIGURE 2-39: *Enable Turn-On/Turn-Off.*

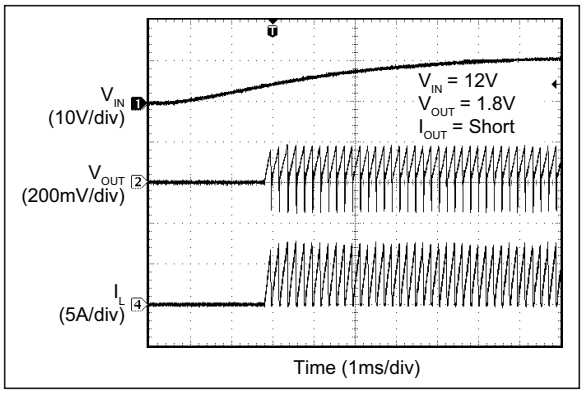


FIGURE 2-42: *Power Up into Short Circuit.*

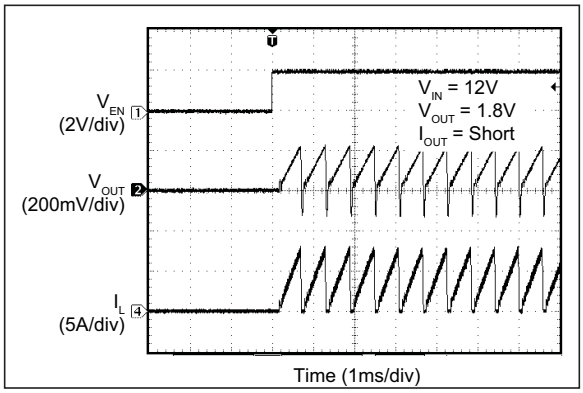


FIGURE 2-43: *Enabled into Short.*

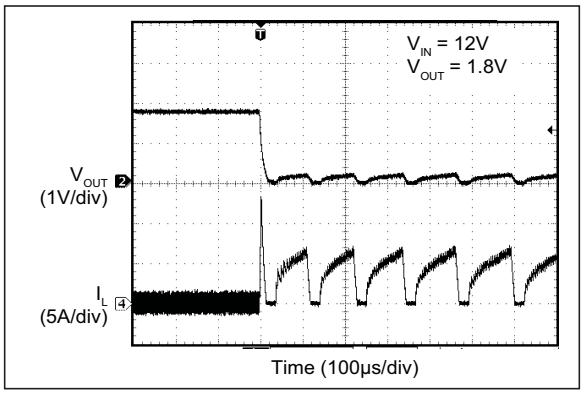


FIGURE 2-44: *Short Circuit.*

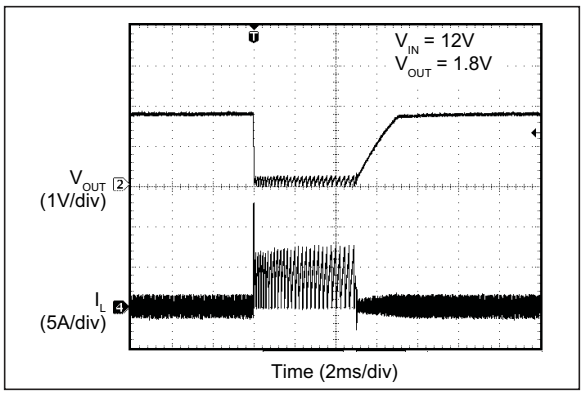


FIGURE 2-45: *Output Recovery from Short Circuit.*

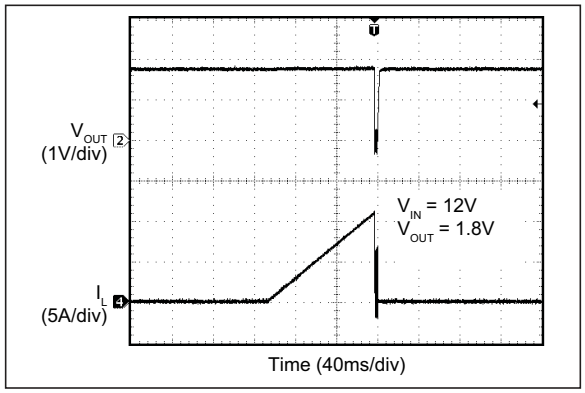


FIGURE 2-46: *Output Current Limit Threshold.*

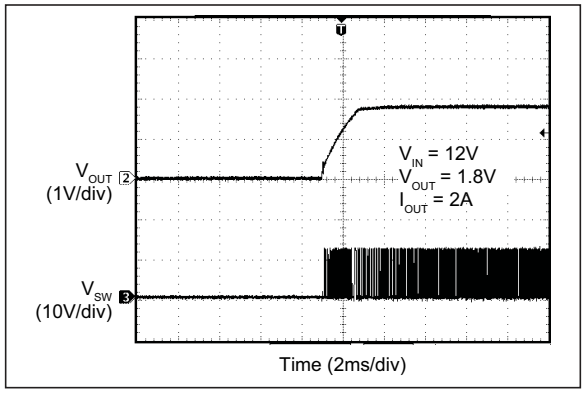


FIGURE 2-47: *Output Recovery from Thermal Shutdown.*

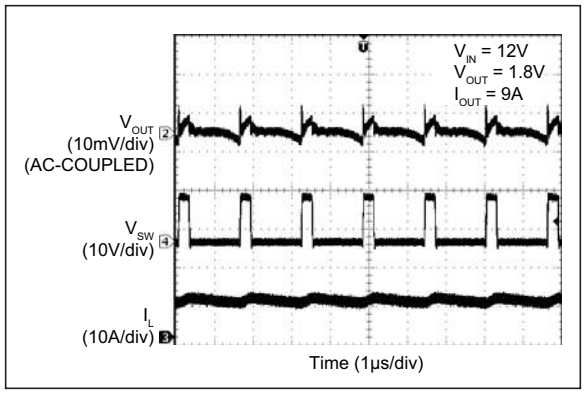


FIGURE 2-48: *Switching Waveforms, I_{OUT} = 9A.*

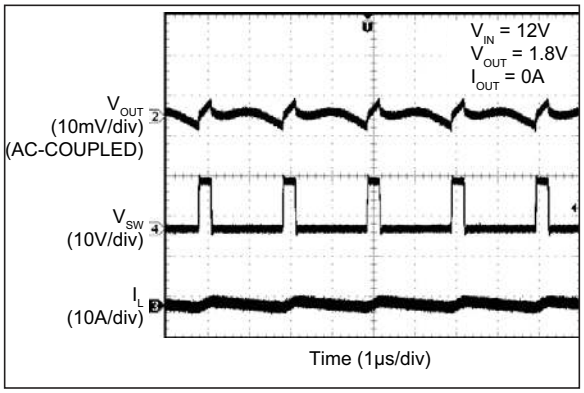


FIGURE 2-49: *Switching Waveforms, I_{OUT} = 0A.*

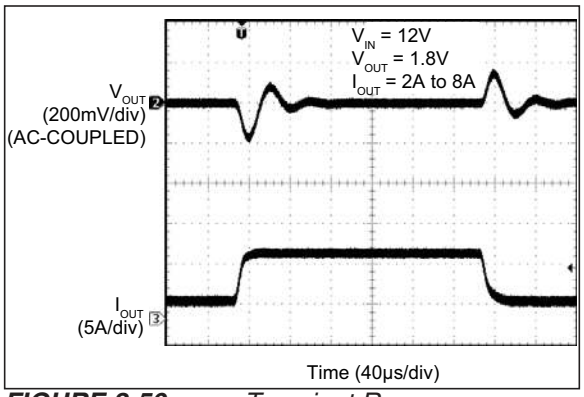


FIGURE 2-50: *Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	PV_{DD}	5V Internal Linear Regulator output. PV_{DD} supply is the power MOSFET gate drive supply voltage created by internal LDO from V_{IN}. When $V_{IN} < 5.5V$, PV_{DD} should be tied to PV_{IN} pins. A 2.2 µF ceramic capacitor from the PV_{DD} pin to PGND (pin 2) must be placed next to the IC.
2, 5, 6, 7, 8, 21	PGND	Power Ground. PGND is the ground path for the MIC24053 buck converter power stage. The PGND pins connect to the low-side N-Channel internal MOSFET gate drive supply ground, the sources of the MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (SGND) loop.
3	NC	No Connect.
4, 9, 10, 11, 12	SW	Switch Node output. Internal connection for the high-side MOSFET source and low-side MOSFET drain. Because of the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes.
13, 14, 15, 16, 17, 18, 19	PVIN	High-Side N-internal MOSFET Drain Connection input. The PV_{IN} operating voltage range is from 4.5V to 19V. Input capacitors between the PV_{IN} pins and the power ground (PGND) are required; keep the connection short.
20	BST	Boost output. Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PV_{DD} pin and the BST pin. A boost capacitor of 0.1 µF is connected between the BST pin and the SW pin. Adding a small resistor at the BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.
22	CS	Current Sense input. The CS pin senses current by monitoring the voltage across the low-side MOSFET during the OFF-time. Current sensing is necessary for short circuit protection. To sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection. The CS pin is also the high-side MOSFET's output driver return.
23	SGND	Signal ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
24	FB	Feedback input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
25	PG	Power Good output. Open-drain output. The PG pin is externally tied with a resistor to V_{DD}. A high output is asserted when $V_{OUT} > 92\%$ of nominal.
26	EN	Enable input. A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, the device's supply current is greatly reduced (typically 5 µA). Do not leave the EN pin floating.
27	VIN	Power Supply Voltage input. Requires bypass capacitor to SGND.
28	V_{DD}	5V Internal Linear Regulator output. V_{DD} supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. V_{DD} is created by internal LDO from V_{IN}. When $V_{IN} < +5.5V$, tie V_{DD} to PV_{IN} pins. A 1 µF ceramic capacitor from the V_{DD} pin to SGND pins must be placed next to the IC.

4.0 FUNCTIONAL DESCRIPTION

The MIC24053 is an adaptive ON-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a Power Good (PG) output. It is designed to operate over a wide input-voltage range, from 4.5V to 19V, and provides a regulated output voltage at up to 9A of output current. It uses an adaptive ON-time control scheme to get a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented without using an external sense resistor. The device includes an internal soft-start function, which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.1 Theory of Operation

The MIC24053 operates in a continuous mode, as shown in the Package Type.

4.2 Continuous Mode

In continuous mode, the MIC24053 feedback pin (FB) senses the output voltage through the voltage divider (R1 and R2), and compares it to a 0.8V reference voltage (V_{REF}) at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the gm amplifier is below 0.8V, the error comparator triggers the control logic and generates an ON-time period. The ON-time period length is predetermined by the “FIXED t_{ON} ESTIMATION” circuitry:

EQUATION 4-1:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times 600kHz}$$

Where:

V_{OUT} = Output voltage

V_{IN} = Power stage input voltage

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. In most cases, the OFF-time period length depends on the feedback voltage. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time ($t_{OFF(min)}$), which is about 300 ns, the MIC24053 control logic applies the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300 ns $t_{OFF(min)}$:

EQUATION 4-2:

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{300ns}{t_S}$$

Where:

t_s = 1/600 kHz = 1.66 µs

It is not recommended to use using the MIC24053 with an OFF-time close to $t_{OFF(min)}$ during steady-state operation. Also, as V_{OUT} increases, the internal ripple injection increases and reduces the line regulation performance. Therefore, the maximum output voltage of the MIC24053 should be limited to 5.5V and the maximum external ripple injection should be limited to 200mV. Please refer to the Setting Output Voltage subsection in the Application Information section for more details.

The actual ON-time and resulting switching frequency vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 18V to 1.0V. The minimum t_{ON} measured on the MIC24053 evaluation board is about 100 ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, analysis of both the steady-state and load transient scenarios is needed.

Figure 4-1 shows the MIC24053 control-loop timing during steady-state operation. During steady-state, the gm amplifier senses the feedback voltage ripple to trigger the ON-time period. The feedback voltage ripple is proportional to the output voltage ripple and the inductor current ripple. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

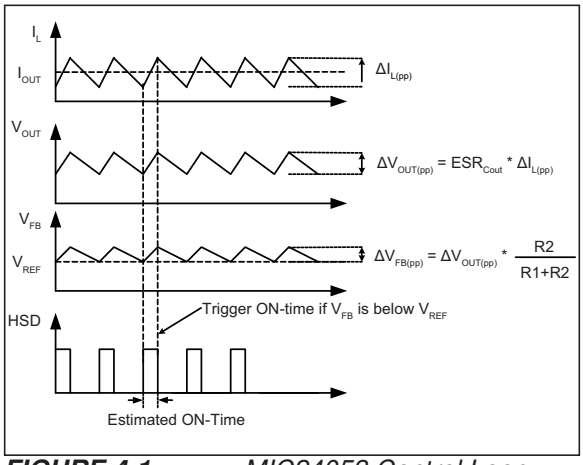


FIGURE 4-1: *MIC24053 Control Loop Timing.*

Figure 4-2 shows the operation of the MIC24053 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This causes the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time ($t_{OFF(min)}$) is generated to charge C_{BST} because the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered because of the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency after the output has stabilized at the new load current level. Because of the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC24053 converter.

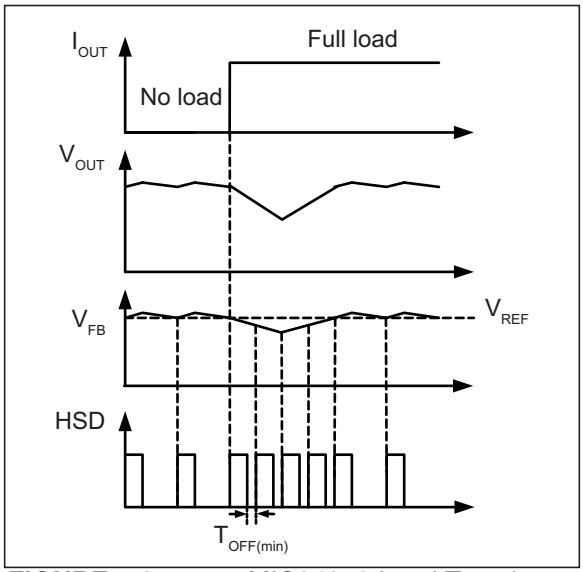


FIGURE 4-2: *MIC24053 Load Transient Response.*

Unlike true current-mode control, the MIC24053 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC24053 control loop has the advantage of eliminating the need for slope compensation.

To meet the stability requirements, the MIC24053 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection subsection in Application Information for more details about the ripple injection technique.

4.3 V_{DD} Regulator

The MIC24053 provides a 5V regulated output for input voltage V_{IN} ranging from 5.5V to 19V. When VIN < 5.5V, tie V_{DD} to the PV_{IN} pins to bypass the internal linear regulator.

4.4 Soft-Start

Soft-start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time draws a lower input surge current.

The MIC24053 implements an internal digital soft-start by making the 0.8V reference voltage (V_{REF}) ramp from 0 to 100% in about 3 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase V_{FB} ramp. After the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

4.5 Current Limit

The MIC24053 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense overcurrent conditions. This method reduces cost, board space, and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC24053 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the peak inductor current is greater than 14A, the MIC24053 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode.” Its purpose is to protect the downstream load in

case of a hard short. The load current-limit threshold has a foldback characteristic related to the feedback voltage as shown in Figure 4-3.

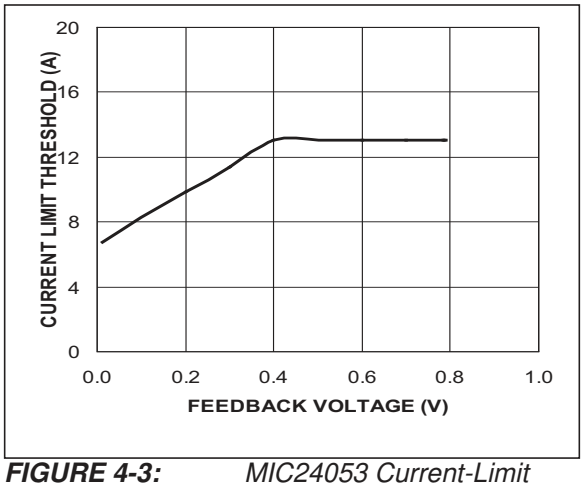


FIGURE 4-3: *MIC24053 Current-Limit Foldback Characteristic.*

4.6 Power Good (PG)

The Power Good (PG) pin is an open-drain output that indicates logic high when the output is nominally 92% of its steady-state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to V_{DD}.

4.7 MOSFET Gate Drive

The Package Type shows a bootstrap circuit consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA, so a 0.1 µF to 1 µF capacitor is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle; that is, Δ_{BST} = 10 mA x 1.67 µs/0.1 µF = 167 mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor (R_G), which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} - V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

5.0 APPLICATION INFORMATION

5.1 Inductor Selection

Selecting the output inductor requires values for inductance, peak, and RMS currents. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 5-1:

EQUATION 5-1:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times 20\% \times I_{OUT(max)}}$$

Where:

- f_{SW} = Switching Frequency, 600 kHz
- 20% = Ratio of AC ripple current to DC output current
- $V_{IN(max)}$ = Maximum power stage input voltage

The peak-to-peak inductor current ripple is:

EQUATION 5-2:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

EQUATION 5-3:

$$I_{K(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-4:

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

The proper selection of core material and minimizing the winding resistance is required to maximize efficiency. The high-frequency operation of the MIC24053 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower-cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-5.

EQUATION 5-5:

$$p_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-6:

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times [1 + 0.0042 \times (T_H - T_{20°C})]$$

Where:

- T_H = Temperature of wire under full load
- $T_{20°C}$ = Ambient Temperature
- $R_{WINDING(20°C)}$ = Room temperature winding resistance (usually specified by the manufacturer)

5.2 Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. It also affects the stability of the control loop.

The maximum value of ESR is calculated with Equation 5-7.

EQUATION 5-7:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-8:

EQUATION 5-8:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:

D = Duty cycle

C_{OUT} = Output capacitance value

f_{SW} = Switching frequency

As described in the Theory of Operation subsection in the Functional Description section, the MIC24053 requires at least 20 mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors' value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are used for the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to the Ripple Injection subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-9:

EQUATION 5-9:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-10:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^{2} \times ESR_{COUT}$$

5.3 Input Capacitor Selection

The input capacitor for the power stage input (V_{IN}) should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning on the input supply. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple primarily depends on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-11:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-12:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-13:

$$P_{DISS(ON)} = I_{CIN(RMS)}^{1} \times ESR_{CIN}$$

5.4 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC24053 g_m amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC24053 will lose control and the output voltage is not regulated. To have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

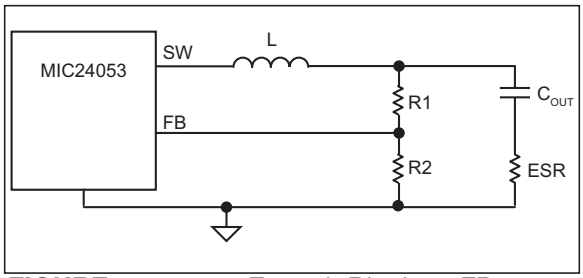


FIGURE 5-1: *Enough Ripple at FB.*

As shown in Figure 5-1, the converter is stable without any ripple injection. The feedback voltage ripple is:

EQUATION 5-14:

$$\Delta V_{FB(pp)} = \frac{R2}{R1 + R2} \times ESR_{COUT} \times \Delta I_{L(pp)}$$

Where:

$\Delta I_{L(pp)}$ = Peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

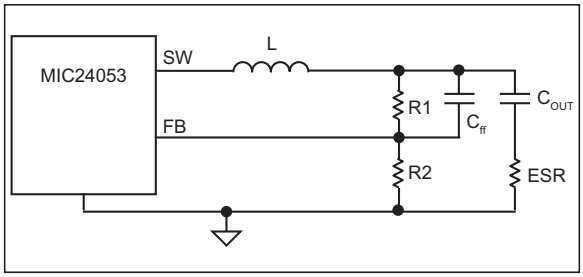


FIGURE 5-2: *Inadequate Ripple at FB.*

The output voltage ripple is fed into the FB pin through a feedforward capacitor (C_{ff}) in this situation, as shown in Figure 5-2. The typical C_{ff} value is between 1nF and 100 nF. With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

EQUATION 5-15:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)}$$

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors.

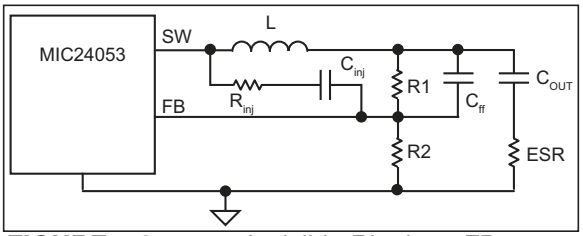


FIGURE 5-3: *Invisible Ripple at FB.*

In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the switching node (SW) using a resistor (R_{inj}) and a capacitor (C_{inj}), as shown in Figure 5-3. The injected ripple is:

EQUATION 5-16:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

EQUATION 5-17:

$$K_{div} = \frac{R1/R2}{R_{inj} \times R1/R2}$$

Where:

V_{IN} = Power stage input voltage

D = Duty Cycle

f_{SW} = Switching frequency

τ = (R1//R2//R_{inj}) × C_{ff}

In Equation 5-16 and Equation 5-17, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

EQUATION 5-18:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \gg 1$$

If the voltage divider resistors (R1 and R2) are in the kΩ range, a C_{ff} of 1 nF to 100 nF can easily satisfy the large time constant requirement. Also, a 100 nF injection capacitor (C_{inj}) is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1 nF to 100 nF if R1 and R2 are in the kΩ range.
2. Select R_{inj} according to the expected feedback voltage ripple using Equation 5-19:

EQUATION 5-19:

$$L_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then the value of R_{inj} is calculated as:

EQUATION 5-20:

$$R_{inj} = (R1 // R2) \times \left(\frac{1}{K_{div}} - 1\right)$$

3. Select C_{inj} as 100 nF, which could be considered as short for a wide range of the frequencies.

5.5 Setting Output Voltage

The MIC24053 requires two resistors to set the output voltage as shown in Figure 5-4.

The output voltage is determined by Equation 5-21:

EQUATION 5-21:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{FB} 0.8V

A typical value of R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 5-22

EQUATION 5-22:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

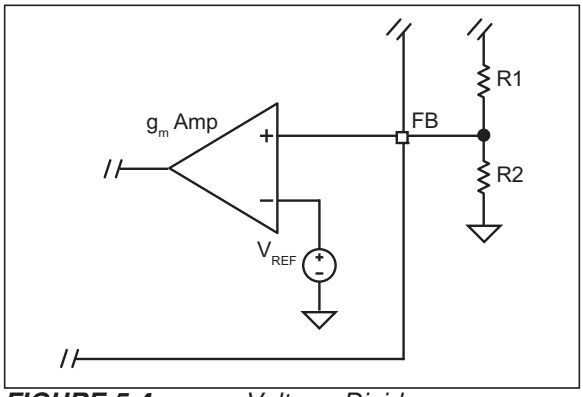


FIGURE 5-4: *Voltage-Divider Configuration.*

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC24053, as shown in Figure 5-5. The inverting input voltage (V_{INJ}) is clamped to 1.2V. As V_{OUT} increases, the swing of V_{INJ} is clamped. The clamped V_{INJ} reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC24053 should be limited to 5.5V to avoid this problem.

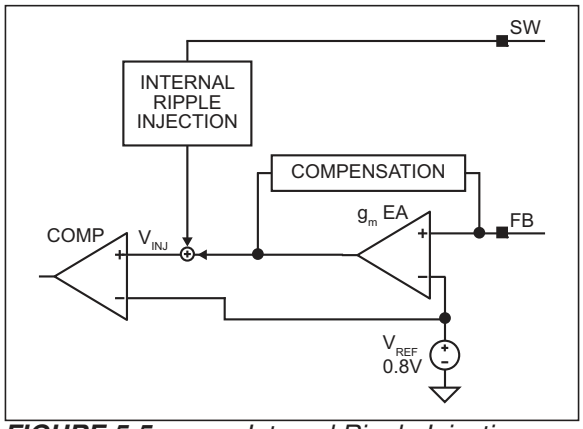


FIGURE 5-5: *Internal Ripple Injection.*

5.6 Thermal Measurements

It is a good idea to measure the IC's case temperature to make sure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get false results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heat-sink, resulting in a lower case measurement.

Two methods of temperature measurement are to use a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire, or higher (smaller wire size), to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in

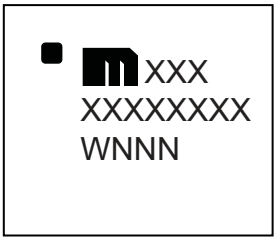
either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on small form factor ICs. However, an IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

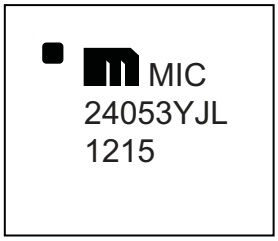
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

28-lead QFN*



Example



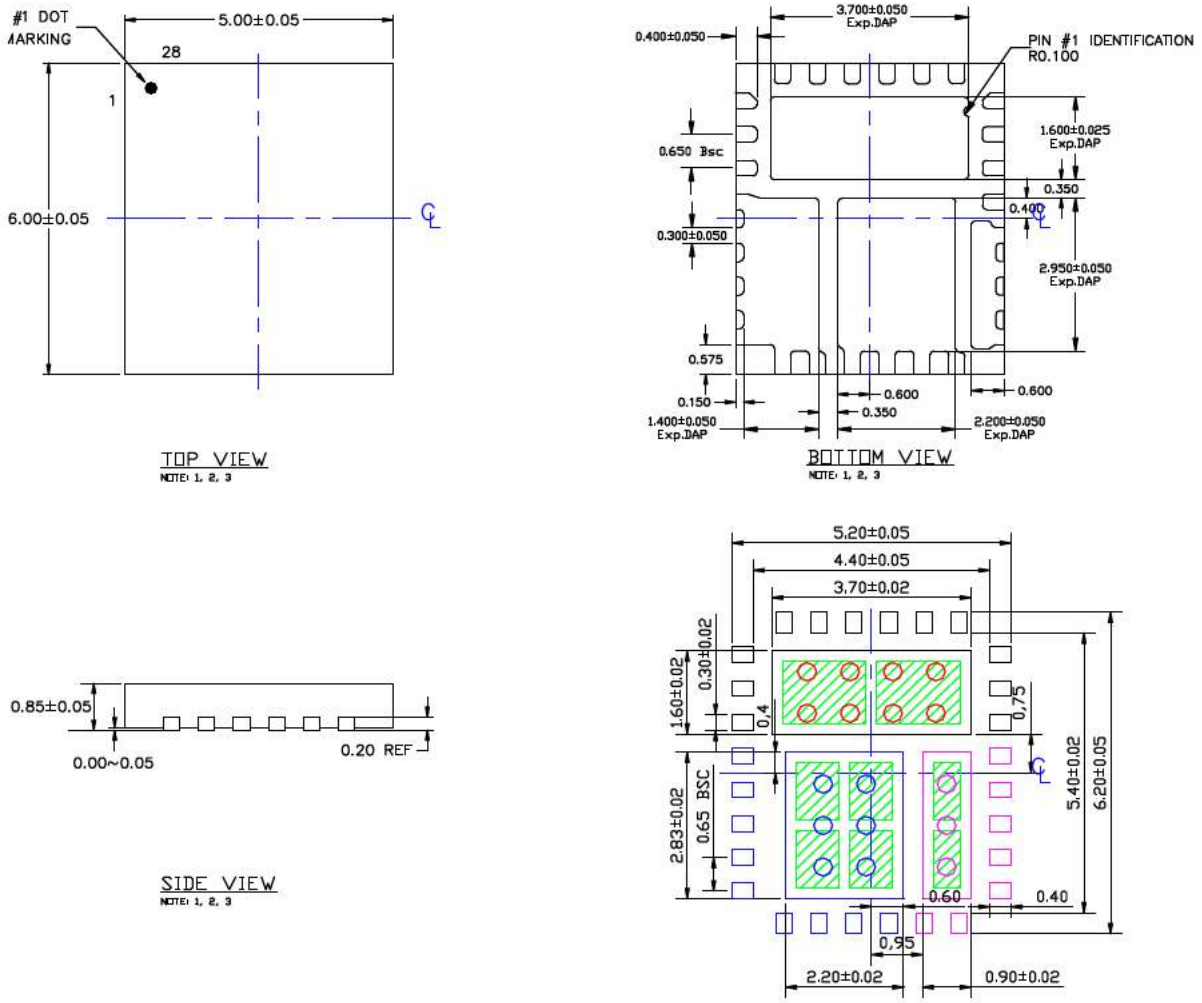
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

28-Pin 5 mm 6 mm QFN Packagev Outline and Recommended Land Pattern

DRAWING #	QFN56-28LD-PL-1	UNIT	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. BLUE COLORED PADS & PURPLE COLORED PADS REPRESENT DIFFERENTPOTENTIALS. DO NOT CONNECT TO GND.
7. RECOMMENDED SOLDER STENCIL OPENING AND VIA SIZES:

		Via size/Pitch	Solder stencil opening/Pitch	Comments
Red circle, black pad	Thermal Via	0 300-0 350mm/0 80mm	1 55x1 20mm/1 75mm	Must be connected to GND plane
Blue circle & pad		0 300-0 350mm/0 80mm	0 80x1 11mm/1 31mm	DO NOT connect to GND plane
Magenta circle & pad		0 300-0 350mm/0 80mm	0 50x1 11mm/1 31mm	DO NOT connect to GND plane

APPENDIX A: REVISION HISTORY

Revision A (November 2016)

- Converted Micrel Document MIC24053 to Microchip datasheet DS20005668A.
- Minor grammatical text changes throughout all sections.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	- XX
Device	Temperature Range	Package	Media Type

Device:	MIC24053:		12V, 9A High-Efficiency Buck Regulator with HyperSpeed Control
Temperature Range:	Y	=	Industrial Temperature Grade –40°C to +125°C
Package:	JL	=	28-Pin 5 mm × 6 mm QFN
Media Type:	TR	=	1000/Reel

Examples:

a) MIC24053YJL-TR: 12V, 9A High-Efficiency Buck Regulator with HyperSpeed Control, –40°C to +125°C Junction Temperature Range, 28-Pin 5 mm × 6 mm QFN package, 1000/Reel.

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