ABLIC

S-82F1C Series

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BATTERY PROTECTION IC FOR 1 CELL PACK WITH LOAD MONITORING PIN

Rev.1.2_00

The S-82F1C Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.
By using an external overcurrent detection resistor, the S-82F1C Series realizes high-accuracy overcurrent protection with less effect from temperature change.
The S-82F1C Series has a load monitoring pin (VM2 pin) allowing for discharge overcurrent status release through determination of VM2 pin voltage drops.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	3.500 V to 4.600 V (5 mV step)	Accuracy ±15 mV
Overcharge release voltage	3.100 V to 4.600 V*1	Accuracy ±50 mV
Overdischarge detection voltage	2.000 V to 3.000 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.000 V to 3.400 V*2	Accuracy ±75 mV
Discharge overcurrent detection voltage 1	0.003 V to 0.100 V (1 mV step)	Accuracy ±1.5 mV
Discharge overcurrent detection voltage 2	0.010 V to 0.100 V (1 mV step)	Accuracy ±3 mV
Load short-circuiting detection voltage	0.020 V to 0.100 V (1 mV step)	Accuracy ±5 mV
Charge overcurrent detection voltage	−0.100 V to −0.003 V (1 mV step)	Accuracy ±1.5 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary)
- Discharge overcurrent control function
  - Release condition of discharge overcurrent status: Load disconnection
  - Release voltage of discharge overcurrent status: $V_{RIOV} = V_{DD} \times 0.8$ (typ.)
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- High-withstand voltage: VM1 pin, VM2 pin, and CO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 2.0 μA typ., 4.0 μA max. (Ta = +25°C)
  - During power-down: 50 nA max. (Ta = +25°C)
  - During overdischarge: 0.5 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- HSNT-8(1616)

■ Block Diagram

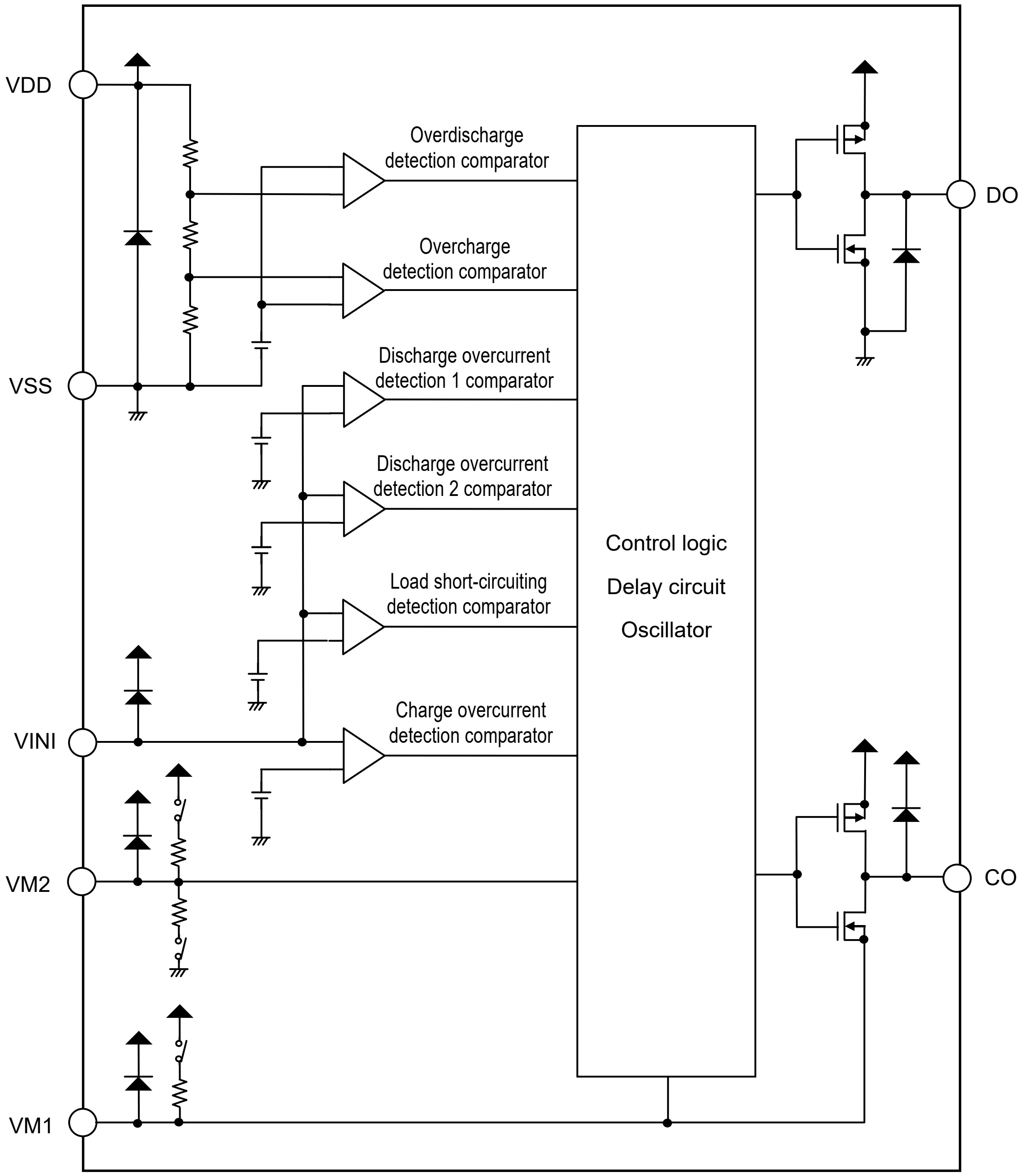


Figure 1

■ Product Name Structure

1. Product name

S-82F1C xx - A8T2 U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- A8T2: Package abbreviation and IC packing specifications*1
  - A8T2: HSNT-8(1616), Tape
- xx: Serial code*2
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HSNT-8(1616)	PY008-A-P-SD	PY008-A-C-SD	PY008-A-R-SD	PY008-A-L-SD

3. Product name list

3. 1 HSNT-8(1616)

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage $[V_{CU}]$	Overcharge Release Voltage $[V_{CL}]$	Overdischarge Detection Voltage $[V_{DL}]$	Overdischarge Release Voltage $[V_{DU}]$	Discharge Overcurrent Detection Voltage 1 $[V_{DIOV1}]$	Discharge Overcurrent Detection Voltage 2 $[V_{DIOV2}]$	Load Short-circuiting Detection Voltage $[V_{SHORT}]$	Charge Overcurrent Detection Voltage $[V_{CIOV}]$
S-82F1CAA-A8T2U	4.500 V	4.350 V	2.100 V	2.300 V	0.014 V	0.020 V	0.068 V	−0.016 V
S-82F1CAB-A8T2U	4.530 V	4.380 V	2.350 V	2.550 V	0.014 V	0.020 V	0.050 V	−0.020 V
S-82F1CAD-A8T2U	4.480 V	4.280 V	2.300 V	2.700 V	0.021V	0.040 V	0.060 V	−0.023 V

Table 2 (2 / 2)

Product Name	Delay Time Combination*1	0 V Battery Charge*2	Power-down Function*3
S-82F1CAA-A8T2U	(1)	Inhibited	Unavailable
S-82F1CAB-A8T2U	(1)	Inhibited	Unavailable
S-82F1CAD-A8T2U	(2)	Enabled	Unavailable

***1.** Refer to **Table 3** about the details of the delay time combinations.
***2.** 0 V battery charge: Enabled, inhibited
***3.** Power-down function: Available, unavailable

Remark Please contact our sales representatives for products other than the above.

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent Detection Delay Time 1 [t_{DIOV1}]	Discharge Overcurrent Detection Delay Time 2 [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]
(1)	1.0 s	64 ms	3.75 s	16 ms	280 μs	32 ms
(2)	512 ms	64 ms	16 ms	4 ms	530 μs	16 ms

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales representatives.

Table 4

Delay Time	Symbol	Selection Range						Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s	–	–	–	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms	128 ms	–	–	–	Select a value from the left.
Discharge overcurrent detection delay time 1	t_{DIOV1}	8 ms	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.
		512 ms	1.0 s	2.0 s	3.0 s	3.75 s	4.0 s	
Discharge overcurrent detection delay time 2	t_{DIOV2}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 μs	530 μs	–	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.

■ Pin Configuration

1. HSNT-8(1616)

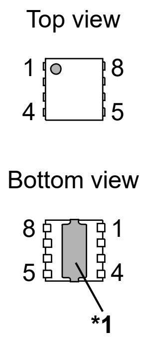


Figure 2

Table 5

Pin No.	Symbol	Description
1	VM2	Load monitoring pin
2	VM1	Input pin for external negative voltage
3	CO	Connection pin of charge control FET gate (CMOS output)
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	VSS	Input pin for negative power supply
6	VDD	Input pin for positive power supply
7	VINI	Overcurrent detection pin
8	NC*2	No connection

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open or V_{DD}.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 6	V
VINI pin input voltage	V_{VINI}	VINI	V_{DD} – 6 to V_{DD} + 0.3	V
VM1 pin input voltage	V_{VM1}	VM1	V_{DD} – 28 to V_{DD} + 0.3	V
VM2 pin input voltage	V_{VM2}	VM2	V_{DD} – 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{DD} – 28 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HSNT-8(1616)	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.015	V_{CU}	V_{CU} + 0.015	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.050	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.020	V_{CL}	V_{CL} + 0.015	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.050	V_{DL}	V_{DL} + 0.050	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.075	V_{DU}	V_{DU} + 0.075	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.050	V_{DU}	V_{DU} + 0.050	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} – 0.0015	V_{DIOV1}	V_{DIOV1} + 0.0015	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} – 0.003	V_{DIOV2}	V_{DIOV2} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.005	V_{SHORT}	V_{SHORT} + 0.005	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.0015	V_{CIOV}	V_{CIOV} + 0.0015	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	$V_{DD} \times 0.77$	$V_{DD} \times 0.80$	$V_{DD} \times 0.83$	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.7	1.1	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.9	1.2	1.5	V	2
Internal Resistance							
Resistance between VDD pin and VM1 pin	R_{VM1D}	V_{DD} = 1.8 V, V_{VM1} = 0 V	500	1250	2500	kΩ	3
Resistance between VDD pin and VM2 pin	R_{VM2D}	V_{DD} = 1.8 V, V_{VM2} = 0 V	500	1250	2500	kΩ	3
Resistance between VM2 pin and VSS pin	R_{VM2S}	V_{DD} = 3.4 V, V_{VM2} = 1.0 V	5	10	15	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM1 and VM2 pins	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, $V_{VM1} = V_{VM2}$ = 0 V	–	2.0	4.0	μA	3
Current consumption during power-down	I_{PDN}	$V_{DD} = V_{VM1} = V_{VM2}$ = 1.5 V	–	–	0.05	μA	3
Current consumption during overdischarge	I_{OPED}	$V_{DD} = V_{VM1} = V_{VM2}$ = 1.5 V	–	–	0.5	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	5	10	20	kΩ	4
CO pin resistance "L"	R_{COL}	–	5	10	20	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	1	2	4	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.7$	t_{DL}	$t_{DL} \times 1.3$	–	5
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	$t_{DIOV1} \times 0.75$	t_{DIOV1}	$t_{DIOV1} \times 1.25$	–	5
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	$t_{DIOV2} \times 0.7$	t_{DIOV2}	$t_{DIOV2} \times 1.3$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.7$	t_{SHORT}	$t_{SHORT} \times 1.3$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.7$	t_{CIOV}	$t_{CIOV} \times 1.3$	–	5

2. Ta = −20°C to +60°C*1

Table 9

(Ta = −20°C to +60°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} − 0.020	V_{CU}	V_{CU} + 0.020	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} − 0.065	V_{CL}	V_{CL} + 0.057	V	1
		$V_{CL} = V_{CU}$	V_{CL} − 0.025	V_{CL}	V_{CL} + 0.020	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} − 0.060	V_{DL}	V_{DL} + 0.055	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} − 0.085	V_{DU}	V_{DU} + 0.080	V	2
		$V_{DL} = V_{DU}$	V_{DU} − 0.060	V_{DU}	V_{DU} + 0.055	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} − 0.002	V_{DIOV1}	V_{DIOV1} + 0.002	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} − 0.003	V_{DIOV2}	V_{DIOV2} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} − 0.005	V_{SHORT}	V_{SHORT} + 0.005	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} − 0.002	V_{CIOV}	V_{CIOV} + 0.002	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	$V_{DD} \times 0.77$	$V_{DD} \times 0.80$	$V_{DD} \times 0.83$	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.7	1.2	1.7	V	2
Internal Resistance							
Resistance between VDD pin and VM1 pin	R_{VM1D}	V_{DD} = 1.8 V, V_{VM1} = 0 V	250	1250	3500	kΩ	3
Resistance between VDD pin and VM2 pin	R_{VM2D}	V_{DD} = 1.8 V, V_{VM2} = 0 V	250	1250	3500	kΩ	3
Resistance between VM2 pin and VSS pin	R_{VM2S}	V_{DD} = 3.4 V, V_{VM2} = 1.0 V	3.5	10	20	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM1 and VM2 pins	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM1} = V_{VM2} = 0 V	–	2.0	5.0	μA	3
Current consumption during power-down	I_{PDN}	V_{DD} = V_{VM1} = V_{VM2} = 1.5 V	–	–	0.1	μA	3
Current consumption during overdischarge	I_{OPED}	V_{DD} = V_{VM1} = V_{VM2} = 1.5 V	–	–	1.0	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.5	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	–	2.5	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.6$	t_{CU}	$t_{CU} \times 1.4$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.6$	t_{DL}	$t_{DL} \times 1.4$	–	5
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	$t_{DIOV1} \times 0.65$	t_{DIOV1}	$t_{DIOV1} \times 1.35$	–	5
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	$t_{DIOV2} \times 0.6$	t_{DIOV2}	$t_{DIOV2} \times 1.4$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.6$	t_{SHORT}	$t_{SHORT} \times 1.4$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.6$	t_{CIOV}	$t_{CIOV} \times 1.4$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. Ta = –40°C to +85°C*1

Table 10

(Ta = –40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.045	V_{CU}	V_{CU} + 0.030	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.080	V_{CL}	V_{CL} + 0.060	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.030	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.080	V_{DL}	V_{DL} + 0.060	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.105	V_{DU}	V_{DU} + 0.085	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.080	V_{DU}	V_{DU} + 0.060	V	2
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} – 0.002	V_{DIOV1}	V_{DIOV1} + 0.002	V	2
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} – 0.003	V_{DIOV2}	V_{DIOV2} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.005	V_{SHORT}	V_{SHORT} + 0.005	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.002	V_{CIOV}	V_{CIOV} + 0.002	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	V_{DD} × 0.77	V_{DD} × 0.80	V_{DD} × 0.83	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.7	1.2	1.7	V	2
Internal Resistance							
Resistance between VDD pin and VM1 pin	R_{VM1D}	V_{DD} = 1.8 V, V_{VM1} = 0 V	250	1250	3500	kΩ	3
Resistance between VDD pin and VM2 pin	R_{VM2D}	V_{DD} = 1.8 V, V_{VM2} = 0 V	250	1250	3500	kΩ	3
Resistance between VM2 pin and VSS pin	R_{VM2S}	V_{DD} = 3.4 V, V_{VM2} = 1.0 V	3.5	10	20	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM1 and VM2 pins	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM1} = V_{VM2} = 0 V	–	2.0	5.0	μA	3
Current consumption during power-down	I_{PDN}	V_{DD} = V_{VM1} = V_{VM2} = 1.5 V	–	–	0.1	μA	3
Current consumption during overdischarge	I_{OPED}	V_{DD} = V_{VM1} = V_{VM2} = 1.5 V	–	–	1.0	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.5	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	–	2.5	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.4	t_{CU}	t_{CU} × 1.6	–	5
Overdischarge detection delay time	t_{DL}	–	t_{DL} × 0.4	t_{DL}	t_{DL} × 1.6	–	5
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	t_{DIOV1} × 0.4	t_{DIOV1}	t_{DIOV1} × 1.6	–	5
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	t_{DIOV2} × 0.4	t_{DIOV2}	t_{DIOV2} × 1.6	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	t_{SHORT} × 0.4	t_{SHORT}	t_{SHORT} × 1.6	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	t_{CIOV} × 0.4	t_{CIOV}	t_{CIOV} × 1.6	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM1} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when setting V2 = 0.01 V, V5 = V6 = 0 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL}.

3. Discharge overcurrent detection voltage 1, discharge overcurrent release voltage (Test circuit 2)

Discharge overcurrent detection voltage 1 (V_{DIOV1}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time 1 (t_{DIOV1}) when the voltage V5 is increased after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V. Discharge overcurrent release voltage (V_{RIOV}) is defined as the voltage V6 at which V_{DO} goes from "L" to "H" when setting V5 = 0 V, V6 = 3.4 V and when the voltage V6 is then gradually decreased.

4. Discharge overcurrent detection voltage 2 (Test circuit 2)

Discharge overcurrent detection voltage 2 (V_{DIOV2}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time 2 (t_{DIOV2}) when the voltage V5 is increased after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V.

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}) when the voltage V5 is increased after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V.

6. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V5 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}) when the voltage V5 is decreased after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V.

7. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V.

8. Current consumption during power-down, current consumption during overdischarge (Test circuit 3)

8. 1 With power-down function

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = V6 = 1.5 V, V5 = 0 V.

8. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of V1 = V2 = V6 = 1.5 V, V5 = 0 V.

9. Resistance between VDD pin and VM1 pin (Test circuit 3)

R_{VM1D} is the resistance between VDD pin and VM1 pin under the set conditions of V1 = 1.8 V, V2 = V5 = V6 = 0 V.

10. Resistance between VDD pin and VM2 pin (Test circuit 3)

R_{VM2D} is the resistance between VDD pin and VM2 pin under the set conditions of V1 = 1.8 V, V2 = V5 = V6 = 0 V.

11. Resistance between VM2 pin and VSS pin (Test circuit 3)

R_{VM2S} is the resistance between the VM2 pin and VSS pin when V5 is decreased to 0 V under the set conditions V1 = 3.4 V, V2 = 0 V, V5 = V6 = 1.0 V.

12. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V, V3 = 3.0 V.

13. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM1 pin and CO pin under the set conditions of V1 = 4.7 V, V2 = V5 = 0 V, V3 = 0.4 V.

14. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V, V4 = 3.0 V.

15. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = V5 = 0 V, V4 = 0.4 V.

16. Overcharge detection delay time (Test circuit 5)

Increase the voltage V1 after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V. The overcharge detection delay time (t_{CU}) is the time period from when the voltage V1 exceeds V_{CU} until V_{CO} goes to "L".

17. Overdischarge detection delay time (Test circuit 5)

Decrease the voltage V1 after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V. The overdischarge detection delay time (t_{DL}) is the time period from when the voltage V1 falls below V_{DL} until V_{DO} goes to "L".

18. Discharge overcurrent detection delay time 1 (Test circuit 5)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V. The discharge overcurrent detection delay time 1 (t_{DIOV1}) is the time period from when the voltage V5 exceeds V_{DIOV1} until V_{DO} goes to "L".

19. Discharge overcurrent detection delay time 2 (Test circuit 5)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V. The discharge overcurrent detection delay time 2 (t_{DIOV2}) is the time period from when the voltage V5 exceeds V_{DIOV2} until V_{DO} goes to "L".

20. Load short-circuiting detection delay time (Test circuit 5)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = V5 = 0 V, V6 = 1.4 V. The load short-circuiting detection delay time (t_{SHORT}) is the time period from when the voltage V5 exceeds V_{SHORT} until V_{DO} goes to "L".

21. Charge overcurrent detection delay time (Test circuit 5)

Decrease the voltage V5 after setting V1 = 3.4 V, V2 = V5 = V6 = 0 V. The charge overcurrent detection delay time (t_{CIOV}) is the time period from when the voltage V5 falls below V_{CIOV} until V_{CO} goes to "L".

22. 0 V battery charge starting charger voltage (0 V battery charge enabled) (Test circuit 4)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V2 at which the current flowing through the CO pin (I_{CO}) exceeds 1.0 μA when the voltage V2 is gradually decreased after setting V1 = V5 = 0 V, V2 = V3 = –0.5 V.

23. 0 V battery charge inhibition battery voltage (0 V battery charge inhibited) (Test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage V1 at which V_{CO} goes to "L" (V_{CO} = V_{VM1}) when the voltage V1 is gradually decreased after setting V1 = 1.8 V, V2 = –2.0 V, V5 = V6 = 0 V.

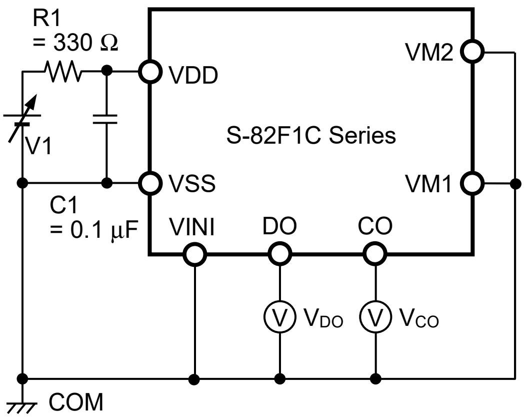


Figure 3 Test Circuit 1

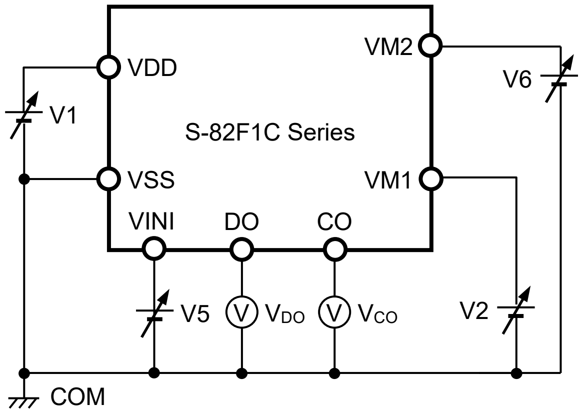


Figure 4 Test Circuit 2

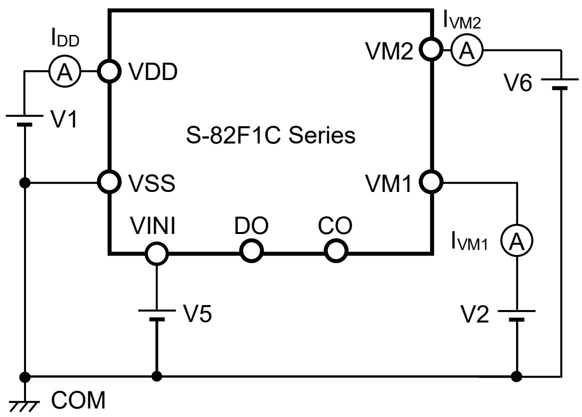


Figure 5 Test Circuit 3

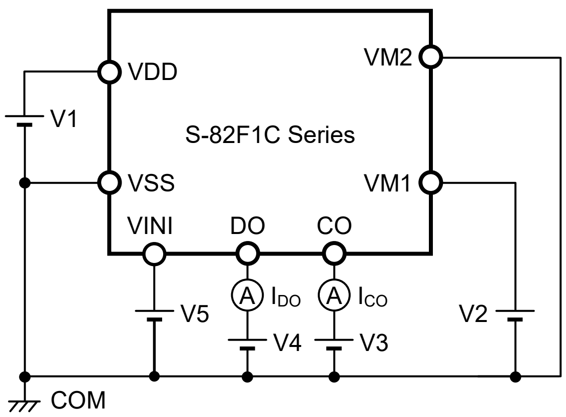


Figure 6 Test Circuit 4

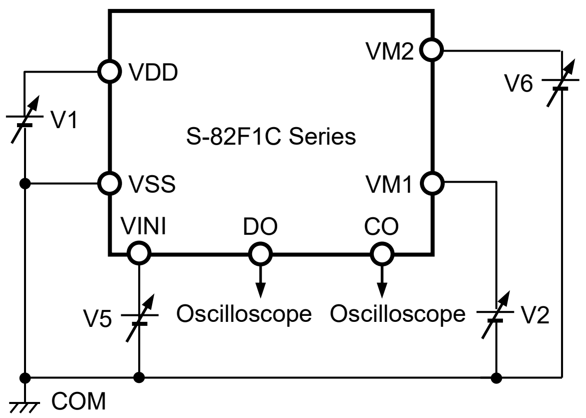


Figure 7 Test Circuit 5

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Example**".

1. Normal status

The S-82F1C Series monitors the voltage of the battery connected between VDD pin and VSS pin, the voltage between VINI pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), and the VINI pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage 1 (V_{DIOV1}), the S-82F1C Series turns both the charge and discharge control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between VDD pin and VM1 pin (R_{VM1D}), the resistance between VDD pin and VM2 pin (R_{VM2D}), and the resistance between VM2 pin and VSS pin (R_{VM2S}) are not connected in the normal status.

Caution After the battery is connected, discharging may not be carried out. In this case, the S-82F1C Series returns to the normal status by connecting a charger.

2. Overcharge status

2. 1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-82F1C Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM1 pin voltage is lower than 0.35 V typ., the S-82F1C Series releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM1 pin voltage is equal to or higher than 0.35 V typ., the S-82F1C Series releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM1 pin voltage rises by the V_f voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM1 pin voltage is equal to or higher than 0.35 V typ., the S-82F1C Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-82F1C Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
In the case that the VM1 pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below V_{CU}, the S-82F1C Series releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM1 pin voltage rises by the V_f voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM1 pin voltage is equal to or higher than 0.35 V typ., the S-82F1C Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL}. The overcharge status is released when the discharge current flows and the VM1 pin voltage goes over 0.35 V typ. by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, the S-82F1C Series turns the discharge control FET off to stop discharging. This condition is called the overdischarge status.
Under the overdischarge status, VDD pin and VM1 pin are shorted by R_{VM1D} and VDD pin and VM2 pin are shorted by R_{VM2D} in the S-82F1C Series. The VM1 pin and VM2 pin voltages are pulled up by R_{VM1D} and R_{VM2D} respectively.
When connecting a charger in the overdischarge status, the battery voltage reaches V_{DL} or higher and the S-82F1C Series releases the overdischarge status if the VM1 pin voltage falls below 0 V typ.
The battery voltage reaches the overdischarge release voltage (V_{DU}) or higher and the S-82F1C Series releases the overdischarge status if the VM1 pin voltage does not fall below 0 V typ.
R_{VM2S} is not connected in the overdischarge status.

3. 1 With power-down function

Under the overdischarge status, when voltage difference between VDD pin and VM1 pin is 0.8 V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a battery charger, the power-down function is released when the VM1 pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM1 pin voltage ≥ 0.7 V typ., the S-82F1C Series maintains the overdischarge status even when the battery voltage reaches V_{DU} or higher.
- When a battery is connected to a charger and 0.7 V typ. > the VM1 pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and the S-82F1C Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM1 pin voltage, the battery voltage reaches V_{DL} or higher and the S-82F1C Series releases the overdischarge status.

3. 2 Without power-down function

The power-down function does not work even when voltage difference between VDD pin and VM1 pin is 0.8 V typ. or lower under the overdischarge status.

- When a battery is not connected to a charger and the VM1 pin voltage ≥ 0.7 V typ., the battery voltage reaches V_{DU} or higher and the S-82F1C Series releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. > the VM1 pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and the S-82F1C Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM1 pin voltage, the battery voltage reaches V_{DL} or higher and the S-82F1C Series releases the overdischarge status.

4. Discharge overcurrent status (Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting)

When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent detection delay time 1 (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

Under the discharge overcurrent status, VM2 pin and VSS pin are shorted by R_{VM2S} in the S-82F1C Series. However, the VM2 pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, the VM2 pin voltage returns to the VSS pin voltage.
When the VM2 pin voltage returns to V_{RIOV} or lower, the S-82F1C Series releases the discharge overcurrent status.
R_{VM1D} and R_{VM2D} are not connected in the discharge overcurrent status.

5. Charge overcurrent status

When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-82F1C Series releases the charge overcurrent status when the discharge current flows and the VM1 pin voltage is 0.35 V typ. or higher by removing the charger.
The charge overcurrent detection does not function in the overdischarge status.

6. 0 V battery charge enabled

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DL}, the S-82F1C Series returns to the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.
2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

7. 0 V battery charge inhibited

This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

8. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1}, t_{DIOV2} and t_{SHORT} start when V_{DIOV1} is detected. When V_{DIOV2} or V_{SHORT} is detected over t_{DIOV2} or t_{SHORT} after the detection of V_{DIOV1}, the S-82F1C Series turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

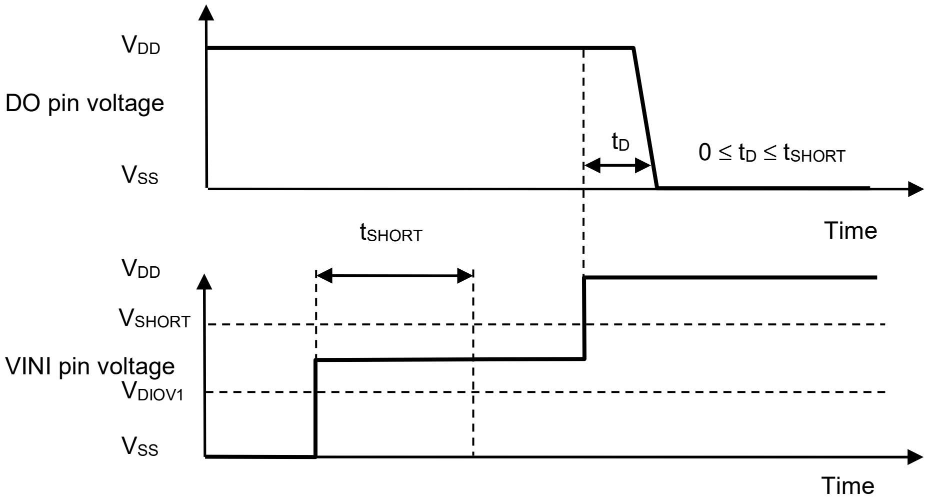
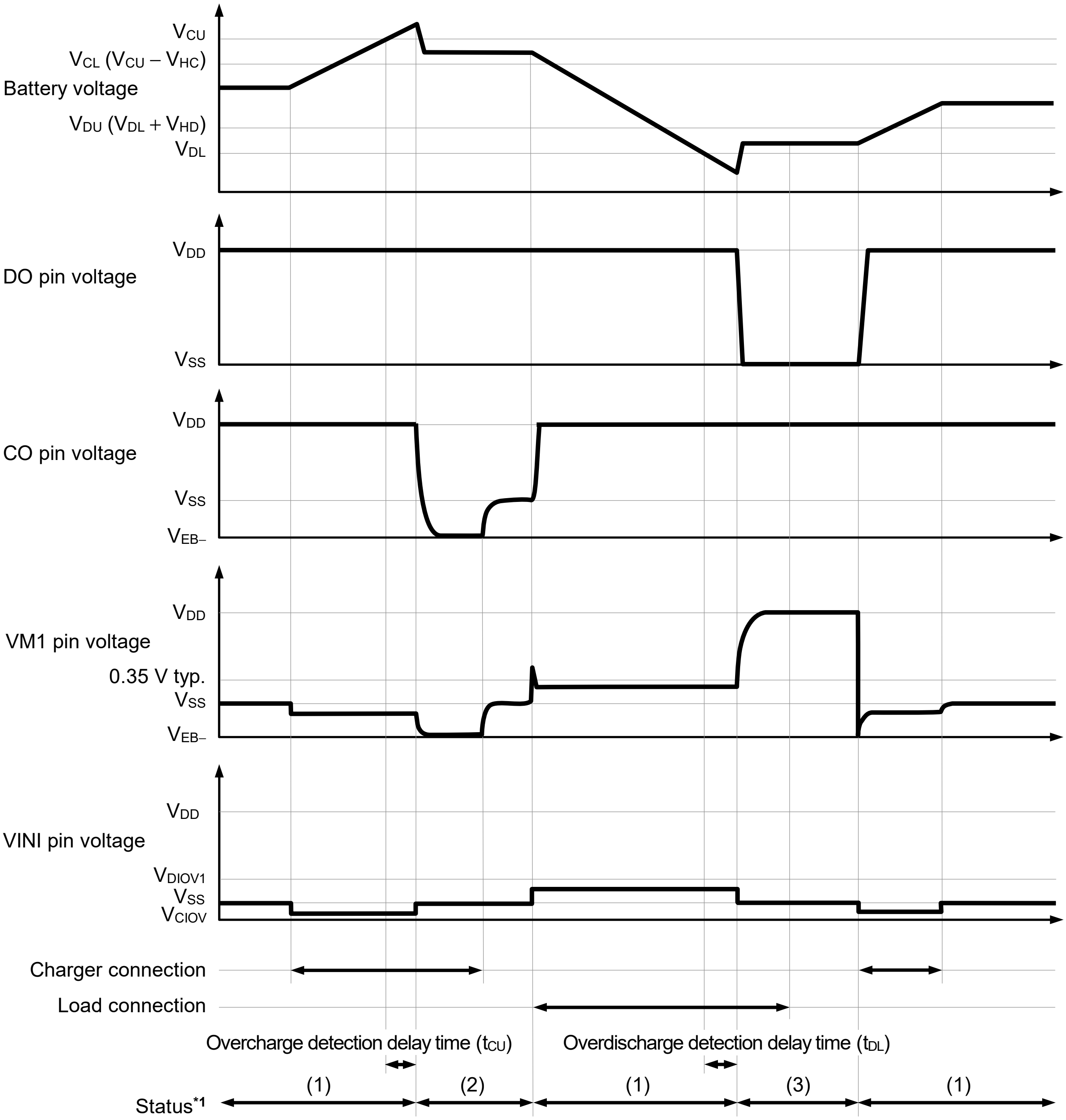


Figure 8

■ Timing Charts

1. Overcharge detection, overdischarge detection

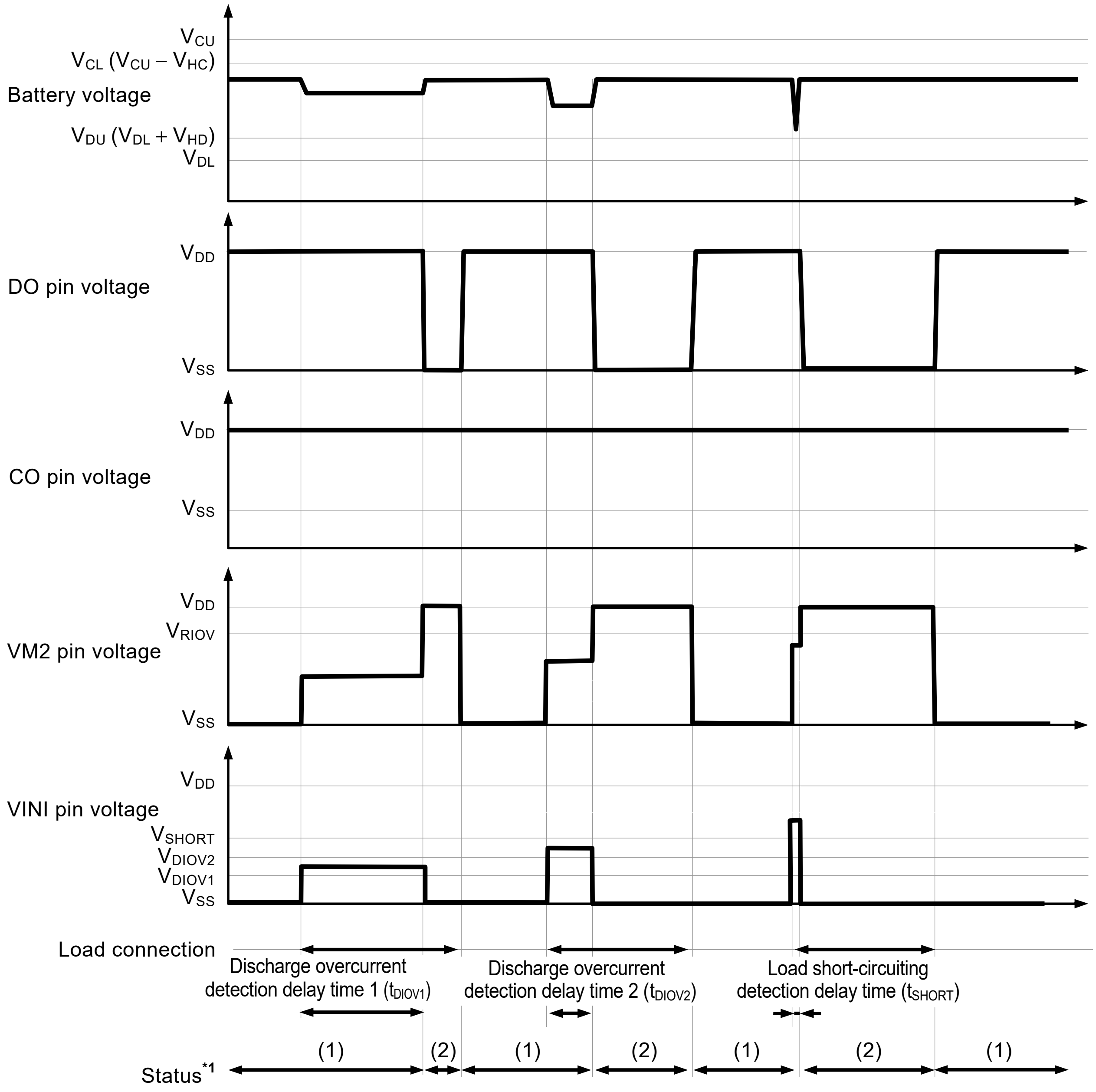


***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 9

2. Discharge overcurrent detection

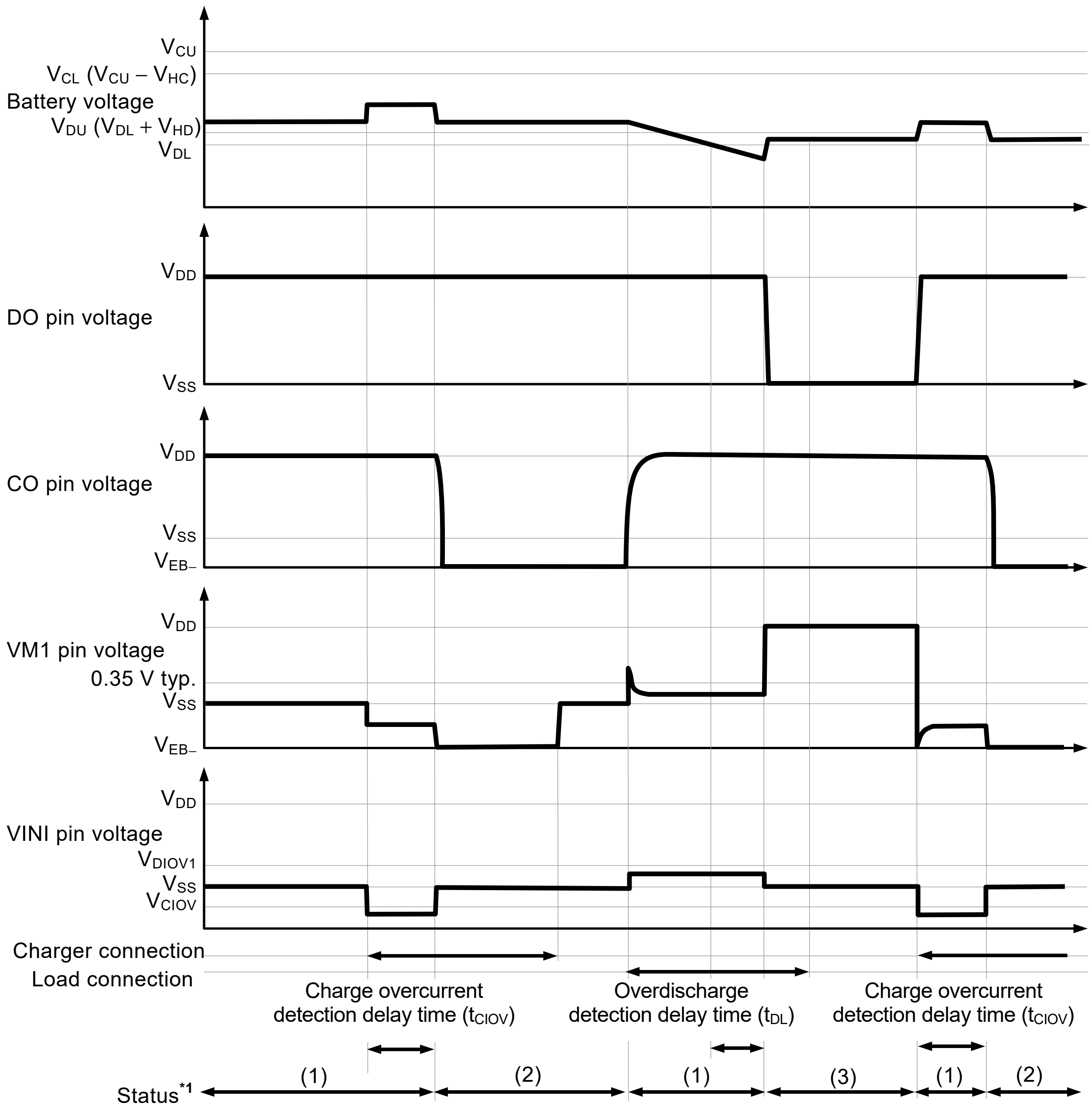


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 10

3. Charge overcurrent detection



***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 11

■ Battery Protection IC Connection Example

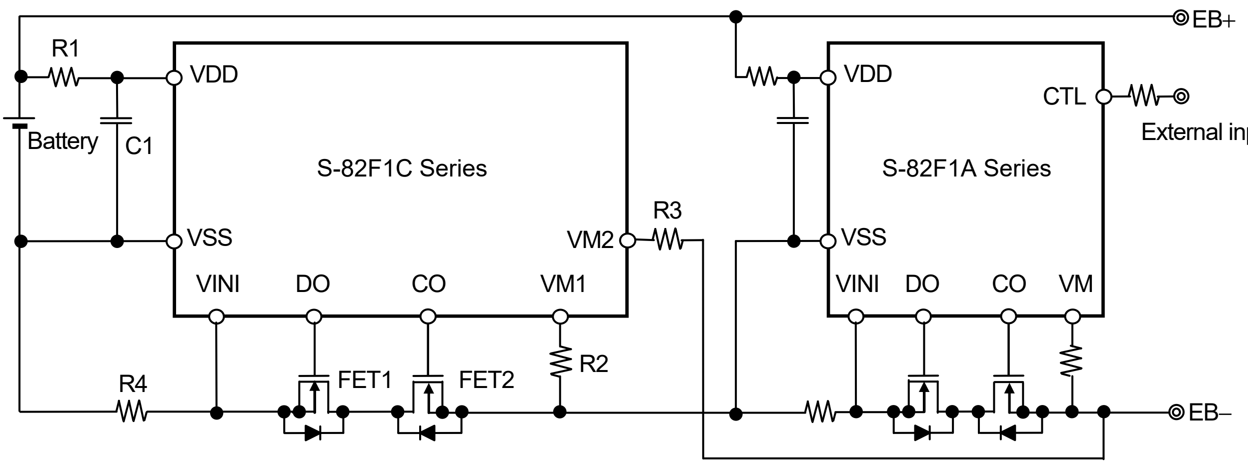


Figure 12

Table 11 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	Nch MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
FET2	Nch MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
R1	Resistor	ESD protection, For power fluctuation	270 Ω	330 Ω	1.2 kΩ*2	–
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	2.2 μF	–
R2	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	470 Ω	1.5 kΩ	–
R3	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	470 Ω	1.5 kΩ	–
R4	Resistor	Overcurrent detection	–	3 mΩ	–	–

***1.** If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** Accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values will worsen the accuracy.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

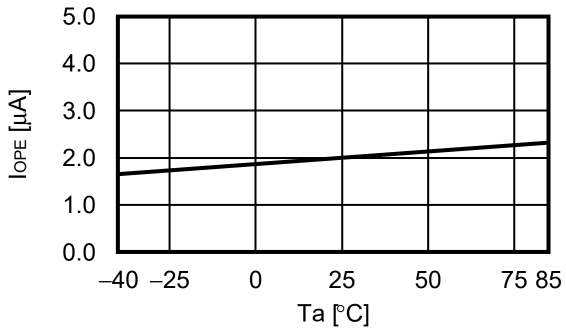
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

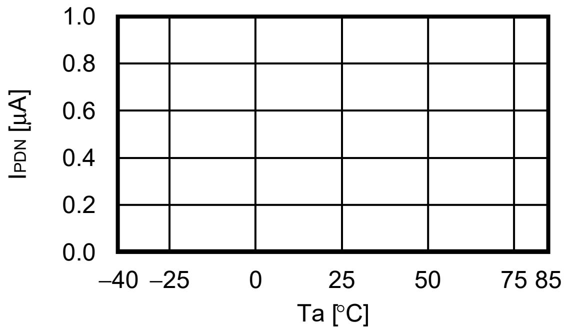
■ Characteristics (Typical Data)

1. Current consumption

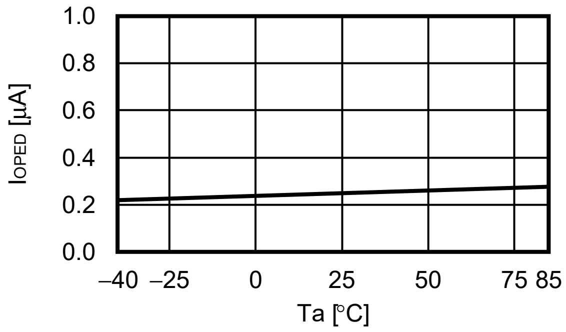
1. 1 I_{OPE} vs. Ta



1. 2 I_{PDN} vs. Ta

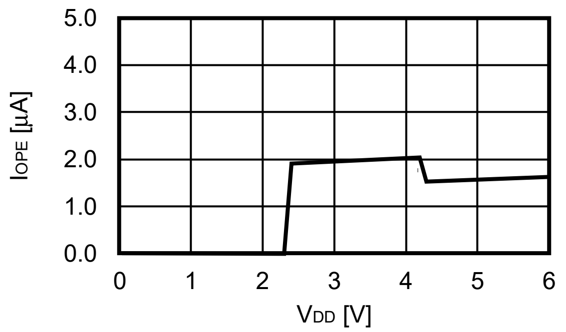


1. 3 I_{OPED} vs. Ta

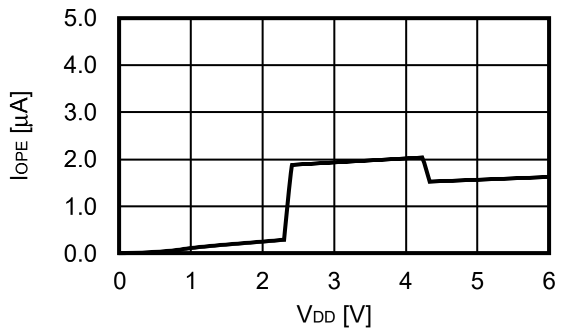


1. 4 I_{OPE} vs. V_{DD}

1. 4. 1 With power-down function

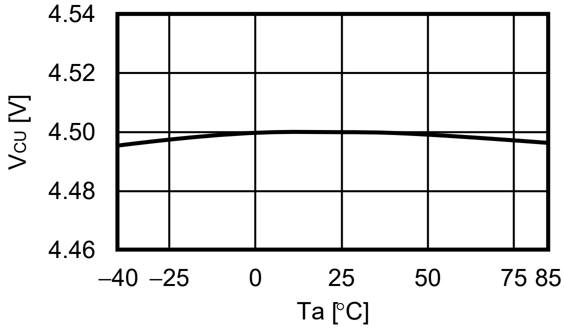


1. 4. 2 Without power-down function

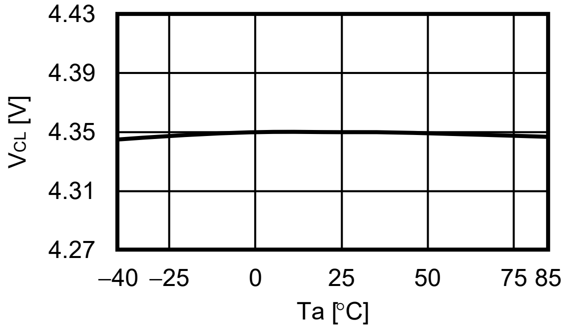


2. Detection voltage

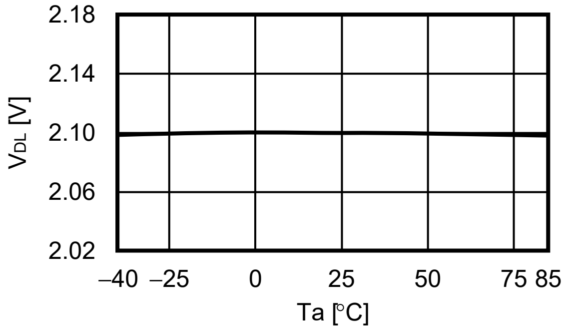
2. 1 V_{CU} vs. Ta



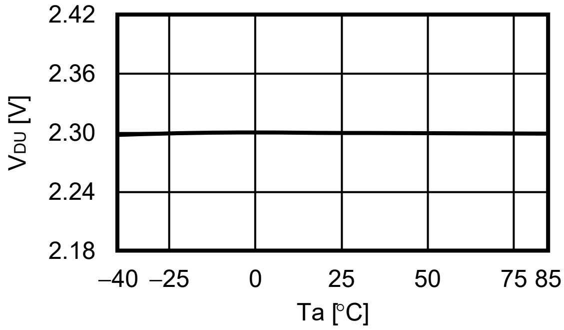
2. 2 V_{CL} vs. Ta



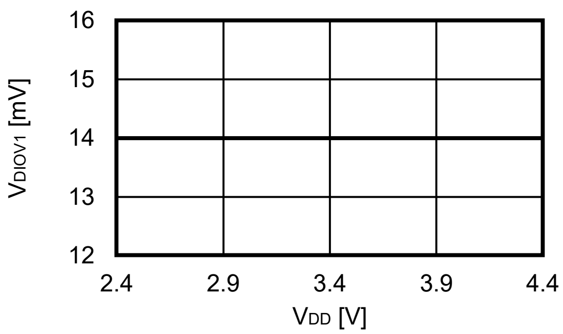
2. 3 V_{DL} vs. Ta



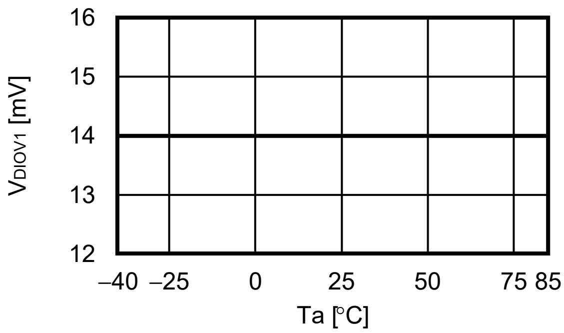
2. 4 V_{DU} vs. Ta



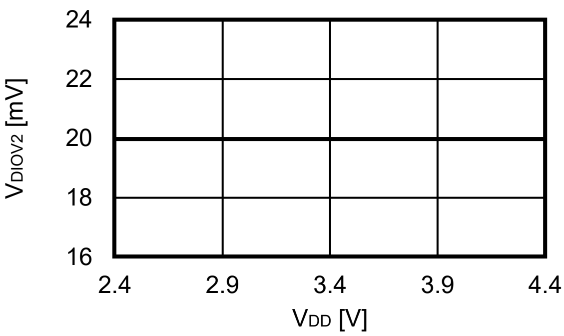
2. 5 V_{DIOV1} vs. V_{DD}



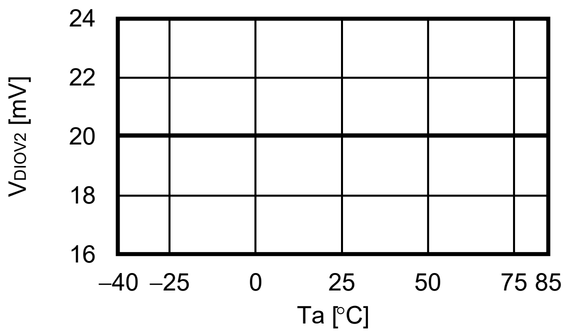
2. 6 V_{DIOV1} vs. Ta



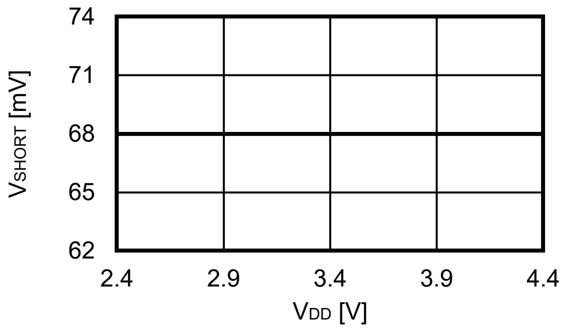
2. 7 V_{DIOV2} vs. V_{DD}



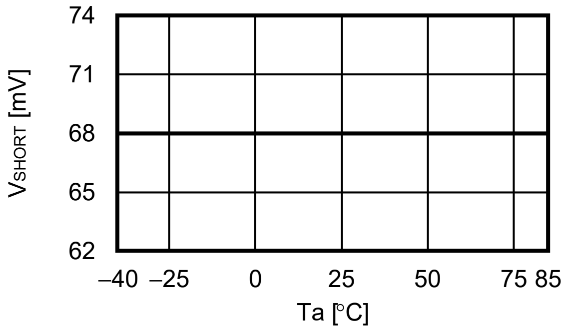
2. 8 V_{DIOV2} vs. Ta



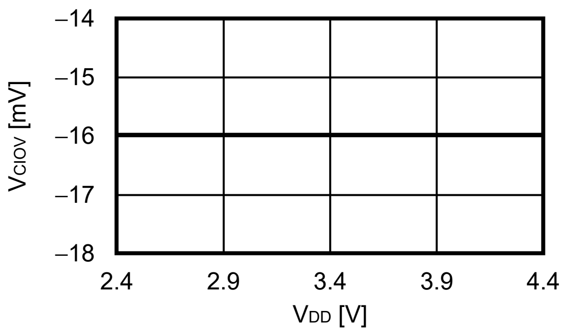
2. 9 V_{SHORT} vs. V_{DD}



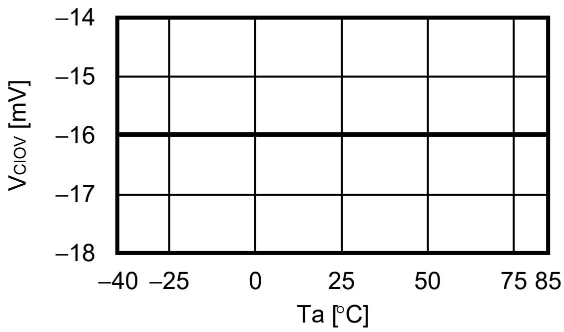
2. 10 V_{SHORT} vs. Ta



2. 11 V_{CIOV} vs. V_{DD}

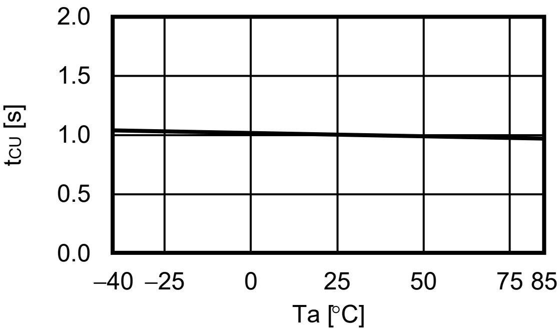


2. 12 V_{CIOV} vs. Ta

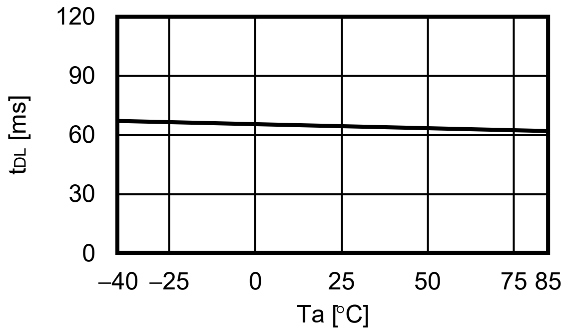


3. Delay time

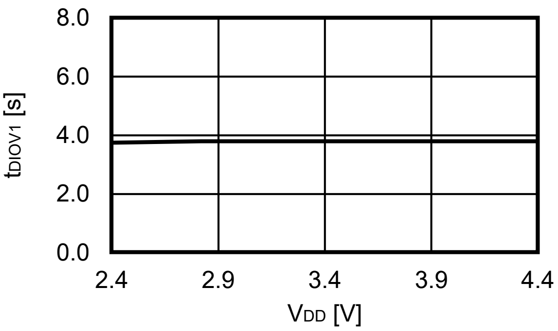
3. 1 t_{CU} vs. Ta



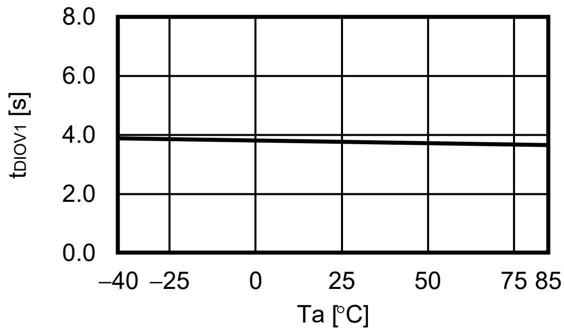
3. 2 t_{DL} vs. Ta



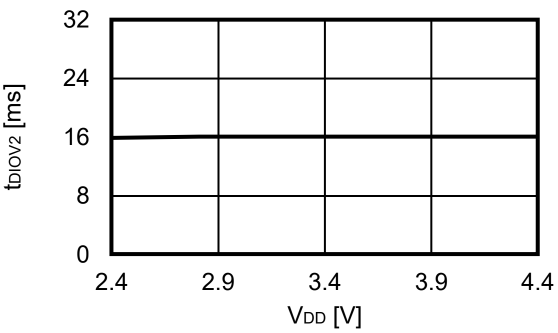
3. 3 t_{DIOV1} vs. V_{DD}



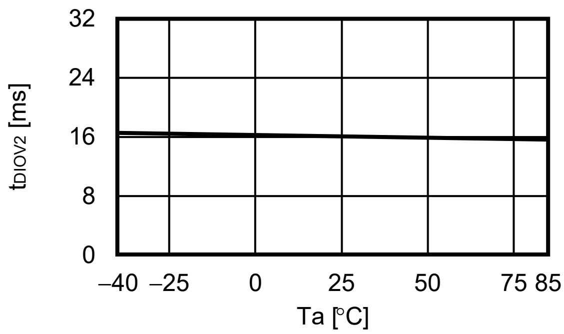
3. 4 t_{DIOV1} vs. Ta



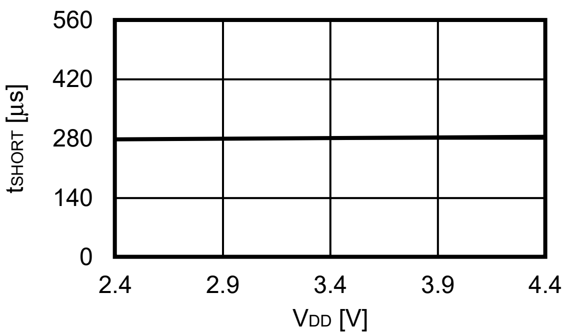
3. 5 t_{DIOV2} vs. V_{DD}



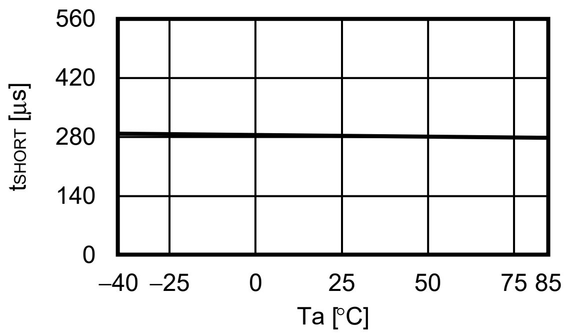
3. 6 t_{DIOV2} vs. Ta



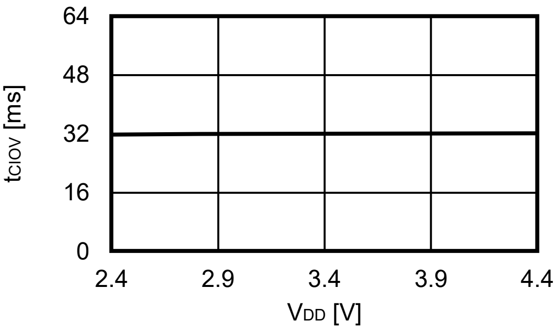
3. 7 t_{SHORT} vs. V_{DD}



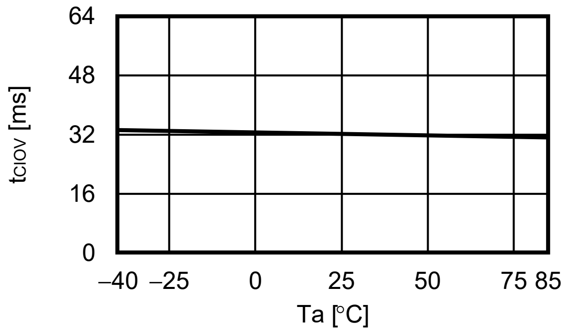
3. 8 t_{SHORT} vs. Ta



3. 9 t_{CIOV} vs. V_{DD}

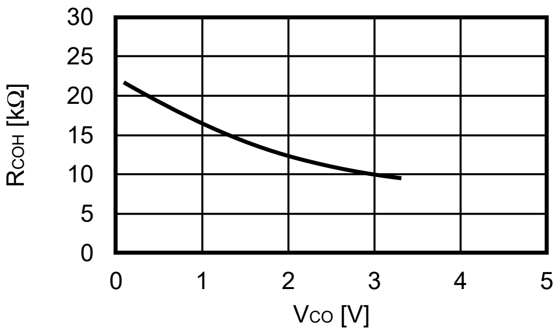


3. 10 t_{CIOV} vs. Ta

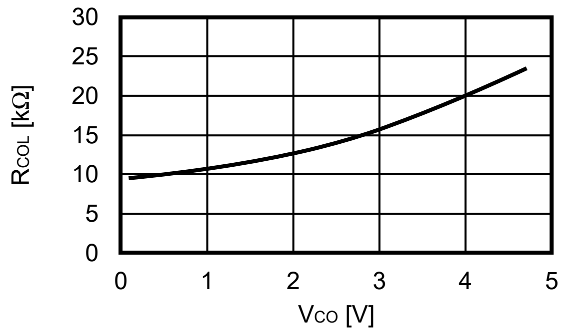


4. Output resistance

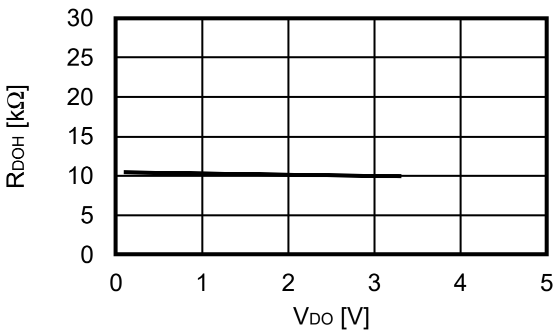
4. 1 R_{COH} vs. V_{CO}



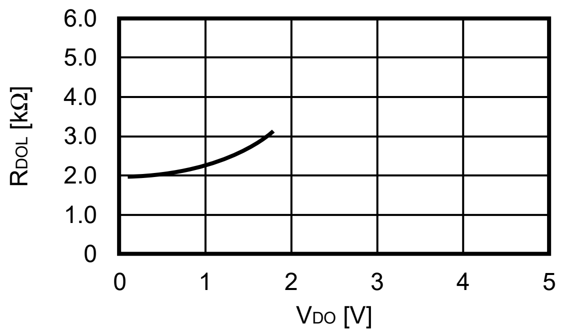
4. 2 R_{COL} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}

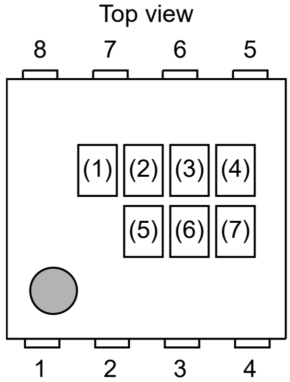


4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. HSNT-8(1616)



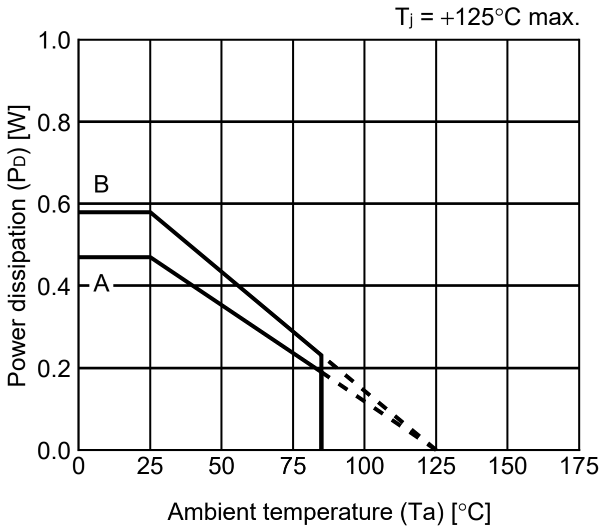
(1): Product code (Blank)
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5) to (7): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-82F1CAA-A8T2U	7	F	A
S-82F1CAB-A8T2U	7	F	B
S-82F1CAD-A8T2U	7	F	D

■ Power Dissipation

HSNT-8(1616)

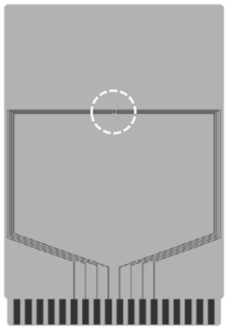


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

HSNT-8(1616) Test Board

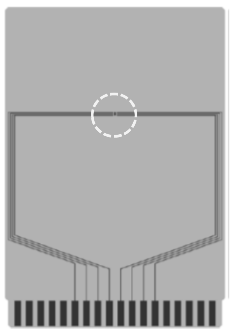
IC Mount Area

(1) **Board A**



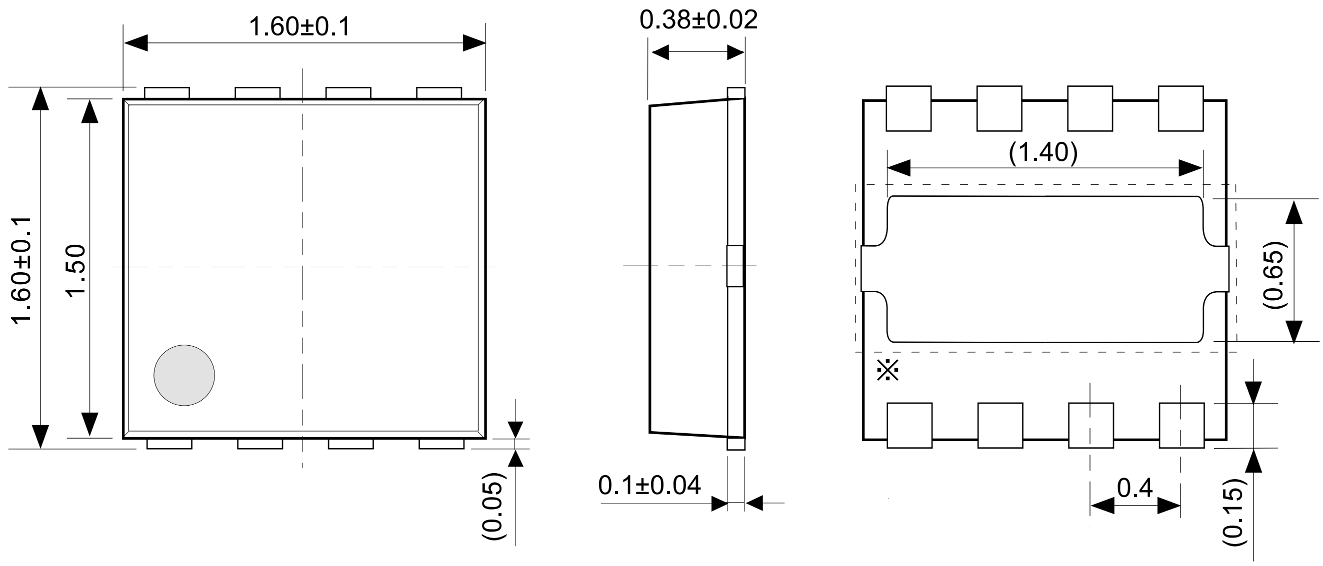
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

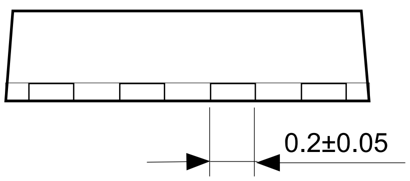
(2) **Board B**



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. HSNT8-B-Board-SD-1.0





※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

TITLE	HSNT-8-B-PKG Dimensions
No.	PY008-A-P-SD-1.0
ANGLE	
UNIT	mm

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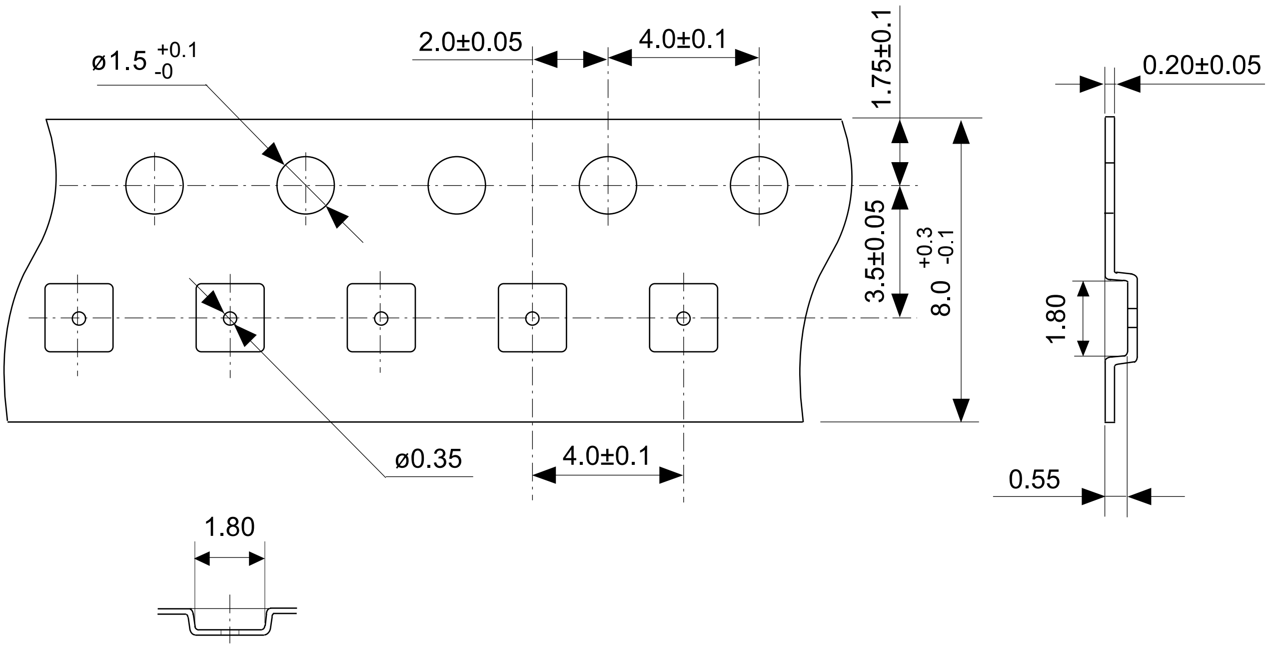
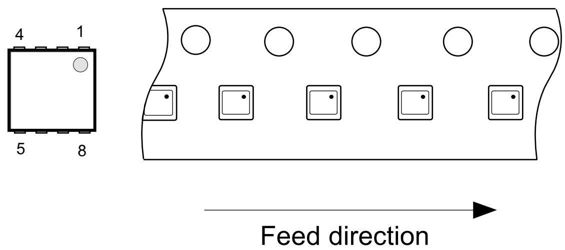
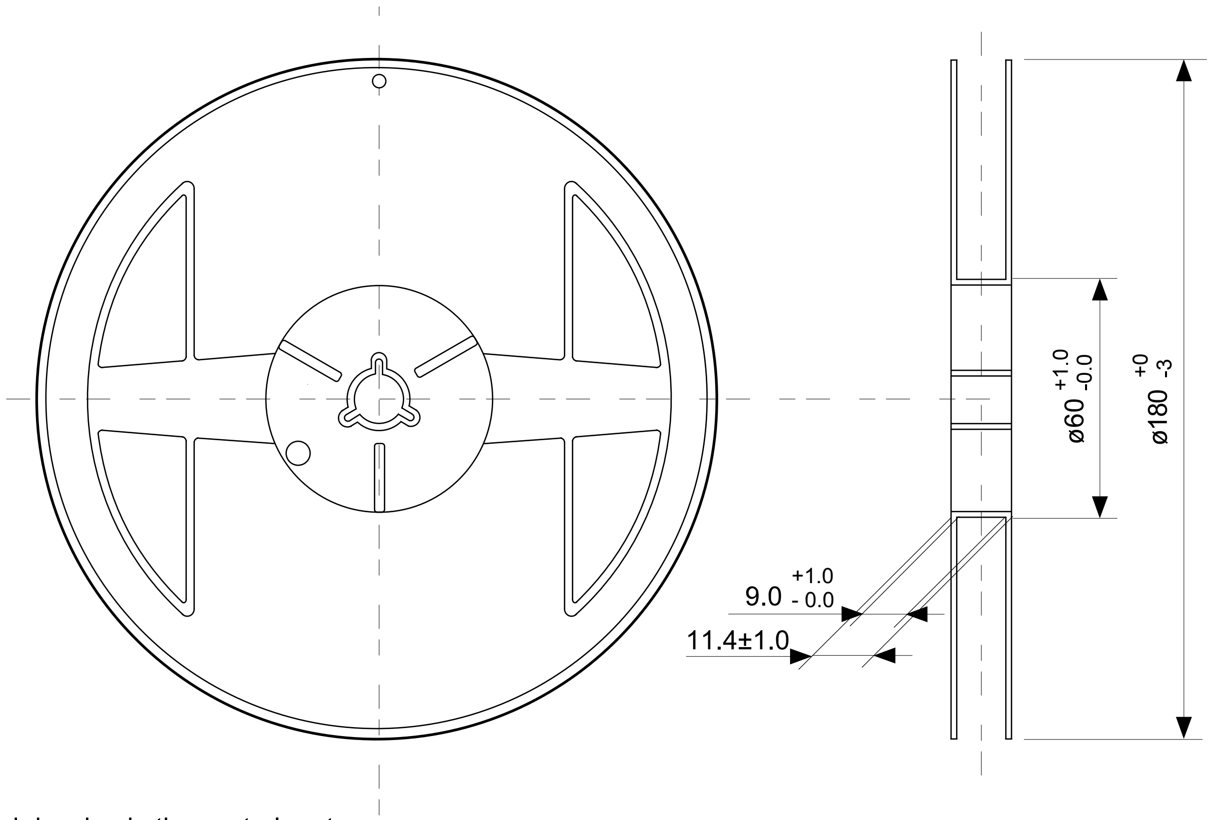




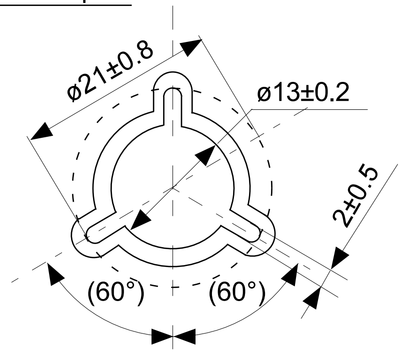
No. PY008-A-C-SD-1.0

TITLE	HSNT-8-B-Carrier Tape
No.	PY008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



No. PY008-A-R-SD-1.0

TITLE	HSNT-8-B-Reel		
No.	PY008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

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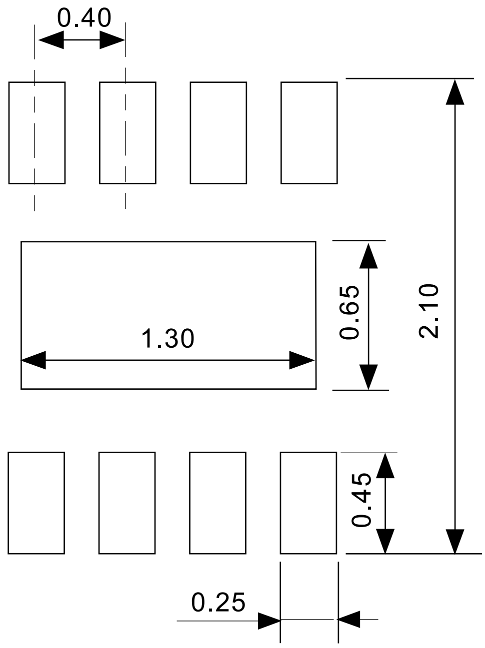
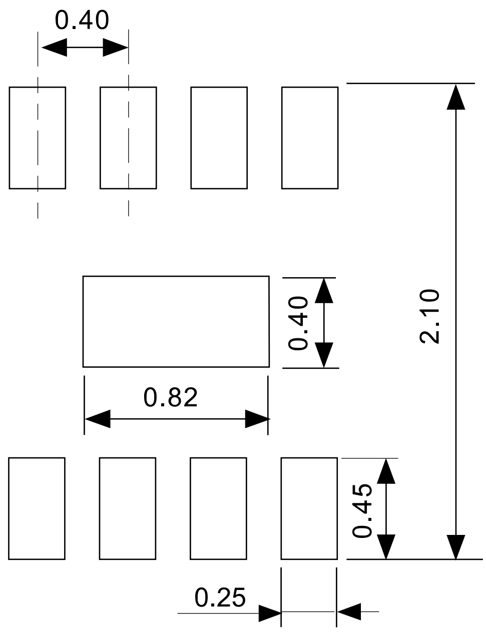
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.12 mm

No. PY008-A-L-SD-1.0

TITLE	HSNT-8-B -Land Recommendation
No.	PY008-A-L-SD-1.0
ANGLE	
UNIT	mm

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2.4-2019.07