ISL6123, ISL6124, ISL6125, ISL6126, ISL6127, ISL6128, ISL6130

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The Intersil ISL6123, ISL6124, ISL6125, ISL6126, ISL6127, ISL6128 and ISL6130 are integrated 4-channel controlled-on/controlled-off power-supply sequencers with supply monitoring, fault protection and a “sequence completed” signal ($\overline{\text{RESET}}$). For larger systems, more than four supplies can be sequenced by simply connecting a wire between the $\overline{\text{SYSRESET}}$ pins of cascaded ICs. The ISL6125 uses four active open-drain outputs to control the on/off sequencing of four supplies. The other sequencers use a patented, micropower 7x charge pump to drive four external low-cost NFET switch gates above the supply rail by 5.3V. These ICs can be biased from 5V down to 1.5V by any supply.

The 4-channel ISL6123 (ENABLE input), ISL6124 ($\overline{\text{ENABLE}}$ input) and ISL6125 offer the designer 4-rail control when all four rails must be in minimal compliance before turn-on and during operation. The ISL6123 and ISL6130 have a low-power standby mode when disabled, which is suitable for battery-powered applications.

The ISL6125 operates like the ISL6124, but instead of charge-pump-driven gate drive outputs, it has open-drain logic outputs for direct interface to other circuitry.

In contrast, for the ISL6126 and ISL6130, each of the four channels operates independently. Each GATE turns on once its individually associated input voltage requirements are met.

The ISL6127 is a pre-programmed A-B-C-D turn-on and D-C-B-A turn-off sequenced IC. Once all inputs are in compliance and $\overline{\text{ENABLE}}$ is asserted, sequencing begins. Each subsequent GATE turns on after the previous one turns on.

The ISL6128 has two groups of two channels, each with its independent I/O. It is ideal for voltage sequencing into redundant capability loads. All four inputs must be satisfied before turn-on, but a single group fault is ignored by the other group.

External resistors provide flexible voltage threshold programming of monitored rail voltages. Delay and sequencing are provided by external capacitors for ramp-up and ramp-down.

Additional I/O is provided for indicating and driving the RESET state in various configurations.

For volume applications, other programmable options and features are available. Contact Intersil sales support with your needs.

Features

- Enables Arbitrary Turn-on and Turn-off Sequencing of Up to Four Power Supplies (0.7V to 5V)
- Operates From 1.5V to 5V Supply Voltage
- Supplies V_{DD} +5.3V of Charge Pumped Gate Drive
- Adjustable Voltage Slew Rate for Each Rail
- Multiple Sequencers Can be Daisy-Chained to Sequence an Infinite Number of Independent Supplies
- Glitch Immunity
- Undervoltage Lockout for Each Supply
- 1µA Sleep State (ISL6123, ISL6130)
- Active High (ISL6123, ISL6130) ENABLE or Low (ISL6124, ISL6125, ISL6126, ISL6127, ISL6128) $\overline{\text{ENABLE}}$ Input
- Active Open Drain Version Available (ISL6125)
- Voltage-determined Sequence (ISL6126, ISL6130)
- Pre-programmed Sequence Available (ISL6127)
- Dual Channel Groupings (ISL6128)
- QFN Package
- Pb-free (RoHS-compliant)

Applications

- Graphics Cards
- FPGA/ASIC/Microprocessor/PowerPC Supply Sequencing
- Network Routers
- Telecommunications Systems

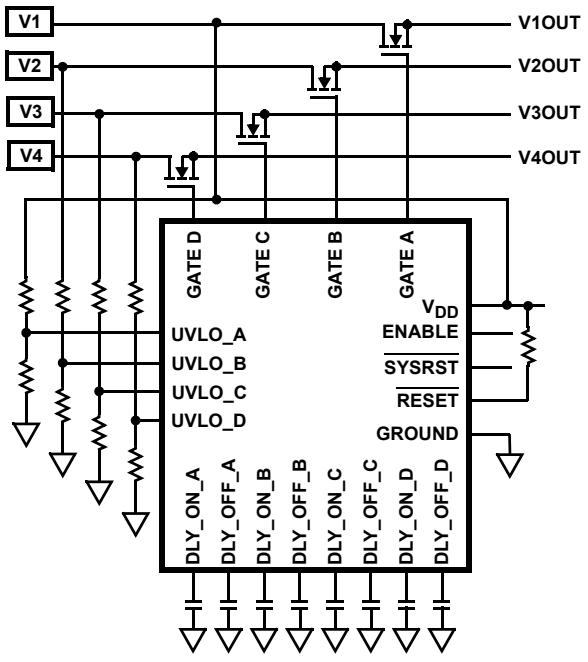


FIGURE 1. TYPICAL ISL6123 APPLICATION

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6123IRZA	61 23IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6124IRZA	61 24IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6125IRZA	61 25IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6126IRZA	61 26IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6127IRZA	61 27IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6128IRZA	61 28IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6130IRZA	61 30IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6123EVAL1Z	ISL6123 Evaluation Platform			
ISL6125EVAL1Z	ISL6125 Evaluation Platform			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6123, ISL6124, ISL6125, ISL6126, ISL6127, ISL6128, ISL6130. For more information on MSL please see Tech Brief TB363.

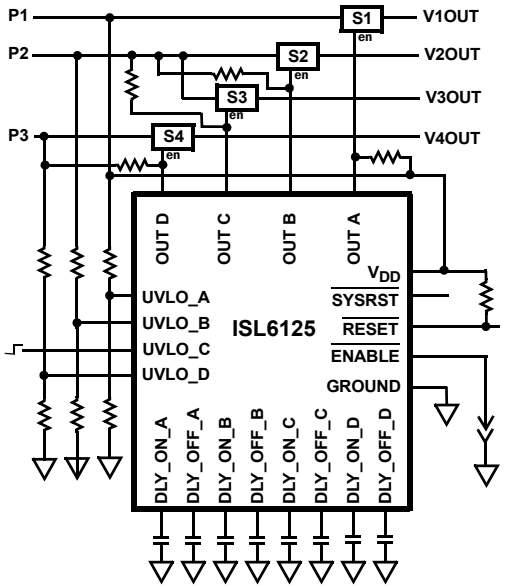


FIGURE 2. ISL6125 APPLICATION

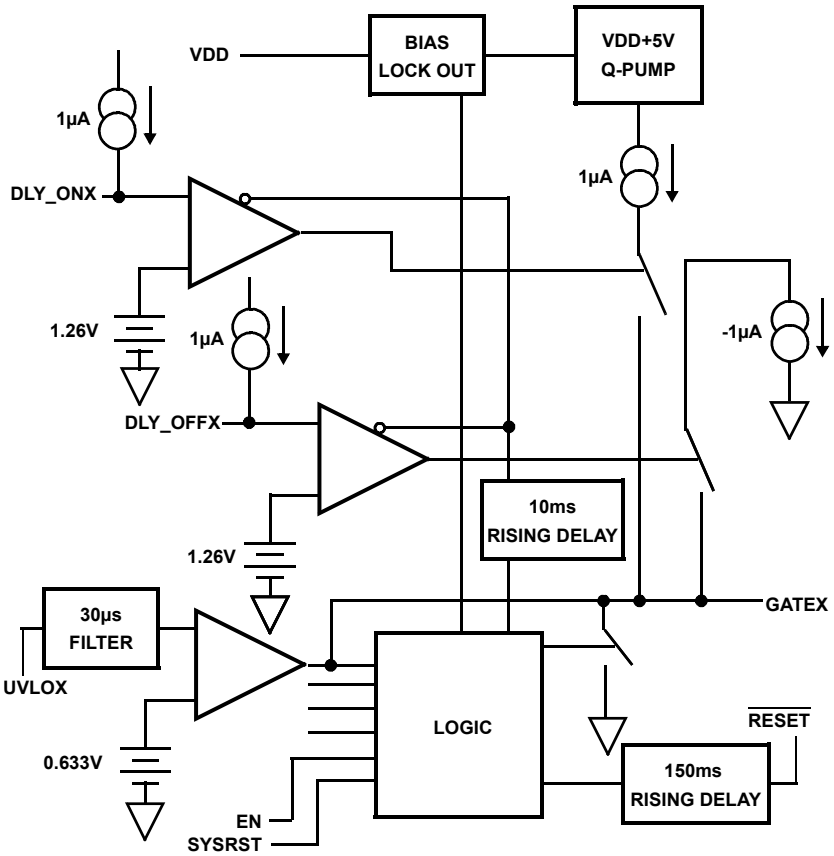
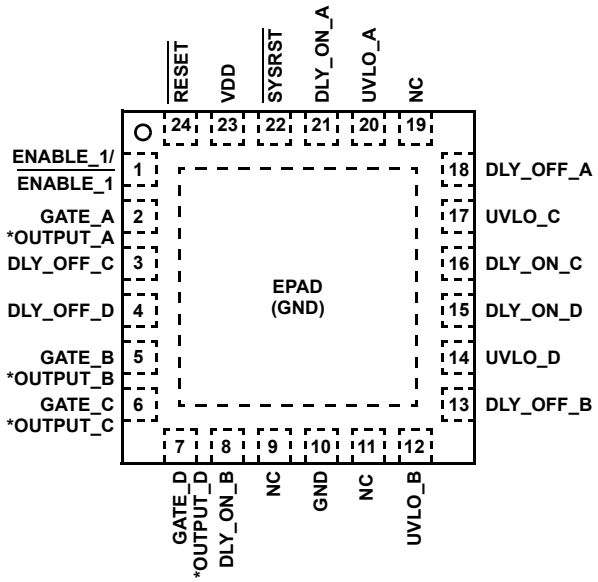


FIGURE 3. ISL6123 BLOCK DIAGRAM (1/4)

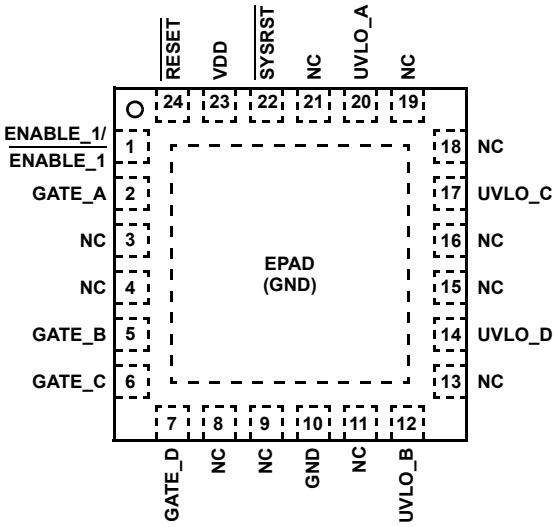
Pin Configurations

ISL6123, ISL6124, ISL6125
(24 LD QFN)
TOP VIEW

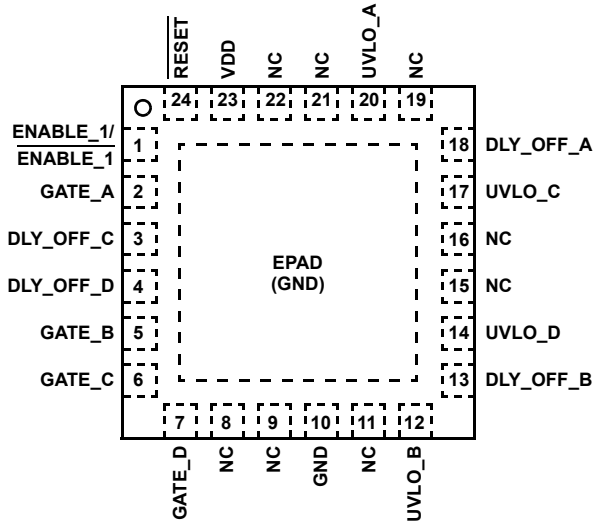


*OUTPUT_A, OUTPUT_B, OUTPUT_C, OUTPUT_D ARE UNIQUE TO ISL6125

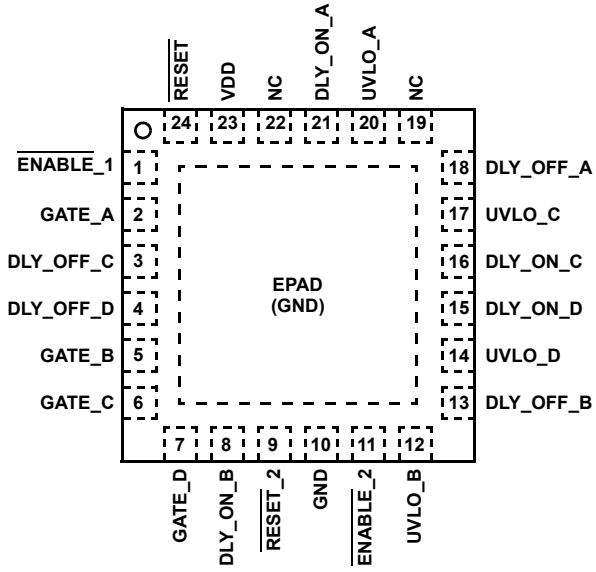
ISL6127
(24 LD QFN)
TOP VIEW



ISL6126, ISL6130
(24 LD QFN)
TOP VIEW



ISL6128
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER				DESCRIPTION
	ISL6123, ISL6124, ISL6125	ISL6126, ISL6130	ISL6127	ISL6128	
V_{DD}	23	23	23	23	Chip Bias. Bias IC from nominal 1.5V to 5V.
GND	10	10	10	10	Bias Return. IC ground.
ENABLE_1/ $\overline{\text{ENABLE\_1}}$	1	1	1	1	Input to start on/off sequencing. Input to initiate start of programmed sequencing of supplies on or off. Enable functionality disabled for 10ms after UVLO is satisfied. ISL6123 and ISL6130 have ENABLE, and ISL6124, ISL6125, ISL6126 and ISL6127 have $\overline{\text{ENABLE}}$. Only ISL6128 has two $\overline{\text{ENABLE}}$ inputs; one for each 2-channel grouping. $\overline{\text{ENABLE\_1}}$ is for (A, B), and $\overline{\text{ENABLE\_2}}$ is for (C, D).
ENABLE_2/ $\overline{\text{ENABLE\_2}}$	NC	NC	NC	11	
$\overline{\text{RESET}}$	24	24	24	24	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ provides low signal 150ms after all GATEs are fully enhanced. Delay is for stabilization of output voltages. $\overline{\text{RESET}}$ asserts low upon UVLO not being satisfied or ENABLE/$\overline{\text{ENABLE}}$ being deasserted. $\overline{\text{RESET}}$ outputs are open-drain, N-channel FET and are guaranteed to be in correct state for VDD down to 1V and are filtered to ignore fast transients on VDD and UVLO_X. $\overline{\text{RESET\_2}}$ only exists on ISL6128 for (C, D) group I/O.
$\overline{\text{RESET\_2}}$	NC	NC	NC	9	
UVLO_A	20	20	20	20	Undervoltage Lockout/Monitoring Input. Provides a programmable UV lockout referenced to an internal 0.633V reference. Filtered to ignore short (<30µs) transients below programmed UVLO level.
UVLO_B	12	12	12	12	
UVLO_C	17	17	17	17	
UVLO_D	14	14	14	14	
DLY_ON_A	21			21	Gate On Delay Timer Output. Allows programming of delay and sequence for VOUT turn-on using a capacitor to ground. Each capacitor charged with 1µA 10ms after turn-on initiated by ENABLE/$\overline{\text{ENABLE}}$. Internal current source provides delay to associated FET GATE turn-on.
DLY_ON_B	8			8	
DLY_ON_C	16			16	
DLY_ON_D	15			15	
DLY_OFF_A	18	18		18	Gate Off Delay Timer Output. Allows programming of delay and sequence for VOUT turn-off through ENABLE/$\overline{\text{ENABLE}}$ via a capacitor to ground. Each capacitor charged with 1µA internal current source to an internal reference voltage, causing corresponding gate to be pulled down, thus turning off FET.
DLY_OFF_B	13	13		13	
DLY_OFF_C	3	3		3	
DLY_OFF_D	4	4		4	
GATE_A	2	2	2	2	FET Gate Drive Output. Drives external FETs with 1µA current source to soft-start ramp into load.
GATE_B	5	5	5	5	
GATE_C	6	6	6	6	
GATE_D	7	7	7	7	
OUTPUT_A	2 (ISL6125)				On ISL6125 only, these are ACTIVE open drain outputs that can be pulled up to a maximum of VDD voltage.
OUTPUT_B	5 (ISL6125)				
OUTPUT_C	6 (ISL6125)				
OUTPUT_D	7 (ISL6125)				
$\overline{\text{SYSRST}}$	22		22		System Reset I/O. As an input, allows for immediate and unconditional latch-off of all GATE outputs when driven low. This input can also be used to initiate programmed sequence with ‘zero’ wait (no 10ms stabilization delay) from input signal on this pin being driven high to first GATE. As an output, when there is a UV condition, this pin pulls low. If common to other $\overline{\text{SYSRST}}$ pins in a multiple IC configuration, it causes immediate and unconditional latch-off of all other GATEs on all other ISL612X sequencers.
GND	EPAD	EPAD	EPAD	EPAD	Ground. Die Substrate. Can be left floating.
NC	9, 19	8, 9, 11, 15, 16, 19, 21, 22	3, 4, 8, 9, 11, 13, 15,16,18, 19, 21	19, 22	No Connect

ISL612X and ISL6130 Variant Feature Matrix

PART NAME	EN/$\overline{EN}$	CMOS/ TTL	GATE DRIVE OR OPEN DRAIN OUTPUTS	REQUIRED CONDITIONS FOR INITIAL START-UP	NUMBER OF UVLO INPUTS MONITORED BY EACH $\overline{RESET}$	NUMBER OF CHANNELS THAT TURN OFF WHEN ONE UVLO FAULTS	PRESET OR ADJUSTABLE SEQUENCE	NUMBER OF UVLO AND PAIRS OF I/O	FEATURES
ISL6123	EN	TTL	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart, Low Bias Current Sleep
ISL6124	$\overline{EN}$	CMOS	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart
ISL6125	$\overline{EN}$	CMO	Open Drain	4 UVLO 1 EN	4 UVLO	4 Open Drain	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart, Open Drain Sequenced Outputs
ISL6126	$\overline{EN}$	CMOS	Gate Drive	1 UVLO 1 EN	4 UVLO	1 Gate	Voltage Determined ON Time Adjustable Off	4 Monitors with 1 I/O	Gates Independent On as UVLO Valid
ISL6127	$\overline{EN}$	CMOS	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Preset	4 Monitors with 1 I/O	Auto Restart
ISL6128	$\overline{EN}$	CMOS	Gate Drive	4 UVLO 2 EN	2 UVLO	2 Gates	Preset	2 Monitors with 2 I/O	Dual Redundant Operation
ISL6130	EN	TTL	Gate Drive	1 UVLO 1 EN	4 UVLO	1 Gate	Voltage Determined ON Time Adjustable Off	4 Monitors with 1 I/O	Gates Independent On as UVLO Valid Low Bias Current Sleep

Absolute Maximum Ratings (Note 6)

V_{DD} ..... +6.0V
GATE ..... -0.3V to V_{DD}+6V
ISL6125 LOGIC $\overline{OUT}$ ..... -0.3V to V_{DD} + 0.3V
UVLO, ENABLE, $\overline{ENABLE}$, $\overline{SYSRST}$ ..... -0.3V to V_{DD} + 0.3V
$\overline{RESET}$, DLY_ON, DLYOFF ..... -0.3V to V_{DD} + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package (Notes 4, 5)	46	8

Maximum Junction Temperature ..... +125°C
Maximum Storage Temperature Range ..... -65°C to +150°C

Operating Conditions

V_{DD} Supply Voltage Range ..... +1.5V to +5.5V
Temperature Range (T_A) ..... -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 1.5V to +5V, T_A = T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
UVLO						
Falling Undervoltage Lockout Threshold	$V_{UVLOvth}$	T_J = +25°C	619	633	647	mV
Undervoltage Lockout Threshold Tempco	$TC_{UVLOvth}$			40		µV/°C
Undervoltage Lockout Hysteresis	$V_{UVLOhys}$			10		mV
Undervoltage Lockout Threshold Range	RUVLOvth	Max $V_{UVLOvth}$- Min $V_{UVLOvth}$		7		mV
Undervoltage Lockout Delay	TUVLOdel	ENABLE satisfied		10		ms
Transient Filter Duration	t_{FIL}	V_{DD}, UVLO, ENABLE glitch filter		30		µs
DELAY ON/OFF						
Delay Charging Current	DLY_ichg	V_{DLY} = 0V	**0.92**	1	**1.08**	µA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)		0.08		µA
Delay Charging Current Temperature Coefficient	TC_DLY_ichg			0.2		nA/°C
Delay Threshold Voltage	DLY_Vth		**1.238**	1.266	**1.294**	V
Delay Threshold Voltage Temperature Coefficient	TC_DLY_Vth			0.2		mV/°C
ENABLE/$\overline{ENABLE}$, $\overline{RESET}$ AND $\overline{SYSRST}$ I/O						
ENABLE Threshold	V_{ENh}			1.2		V
$\overline{ENABLE}$ Threshold	V_{ENh}			0.5 V_{DD}		V
ENABLE/$\overline{ENABLE}$ Hysteresis	V_{ENh} -V_{ENl}	Measured at V_{DD} = 1.5V		0.2		V
ENABLE/$\overline{ENABLE}$ Lockout Delay	t_{delEN_LO}	UVLO satisfied		10		ms
ENABLE/$\overline{ENABLE}$ Input Capacitance	Cin_en			5		pF
$\overline{RESET}$ Pull-up Voltage	Vpu_rst			V_{DD}		V
$\overline{RESET}$ Pull-Down Current	$I_{\overline{RST}pd1}$	V_{DD} = 1.5V, $\overline{RST}$ = 0.1V		5		mA
	$I_{\overline{RST}pd3}$	V_{DD} = 3.3V, $\overline{RST}$ = 0.1V		13		mA
	$I_{\overline{RST}pd5}$	V_{DD} = 5V, $\overline{RST}$ = 0.1V		17		mA

Electrical Specifications V_{DD} = 1.5V to +5V, $T_A = T_J$ = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$\overline{\text{RESET}}$ Delay after GATE High	$T_{\overline{RST}del}$	GATE = V_{DD}+5V		160		ms
$\overline{\text{RESET}}$ Output Low	$V_{\overline{RST}l}$	Measured at V_{DD} = 5V with 5k pull-up resistors			**0.1**	V
RESET Output Capacitance	C_{OUT_RST}			10		pF
$\overline{\text{SYSRST}}$ Pull-Up Voltage	Vpu_srst			V_{DD}		V
$\overline{\text{SYSRST}}$ Pull-Down Current	Ipu_1.5	V_{DD} = 1.5V		5		µA
	Ipu_5	V_{DD} = 5V		100		µA
$\overline{\text{SYSRST}}$ Low Output Voltage	Vol_srst	V_{DD} = 1.5V, I_{OUT} = 100µA		150		mV
$\overline{\text{SYSRST}}$ Output Capacitance	Cout_srst			10		pF
$\overline{\text{SYSRST}}$ Low to GATE Turn-Off	t_{delSYS_G}	GATE = 80% of V_{DD} + 5V		40		ns
GATE						
GATE Turn-On Current	I_{GATEon}	GATE = 0V	**0.8**	1.1	**1.4**	µA
GATE Turn-Off Current	$I_{GATEoff\_I}$	GATE = V_{DD}, Disabled	**-1.4**	-1.05	**-0.8**	µA
GATE Current Range	I_{GATE_range}	Within IC I_{GATE} max-min			**0.35**	µA
GATE Turn-On/Off Current Temperature Coefficient	TC_I_{GATE}			0.2		nA/°C
GATE Pull-Down High Current	$I_{GATEoff\_h}$	GATE = V_{DD}, UVLO = 0V		88		mA
GATE High Voltage	V_{GATEh}	V_{DD} < 2V, T_J = +25°C		V_{DD} + 4.9V		V
	V_{GATEh}	V_{DD} > 2V	**V_{DD} + 5V**	V_{DD} + 5.3V		V
GATE Low Voltage	V_{GATEl}	Gate Low Voltage, V_{DD} = 1V		0	**0.1**	V
ISL6125 OPEN DRAIN						
Open Drain On Resistance	R_{DSON_5V}	V_{DD} = 5V, $\overline{EN}$ = V_{DD}		25		Ω
	$R_{DSON\_3.3V}$	V_{DD} = 3.3V, $\overline{EN}$ = V_{DD}		32		Ω
	$R_{DSON\_2.5V}$	V_{DD} = 2.5V, $\overline{EN}$ = V_{DD}		40		Ω
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V		0.20	**0.5**	mA
	$I_{VDD\_3.3V}$	V_{DD} = 3.3V		0.14		mA
	$I_{VDD\_1.5V}$	V_{DD} = 1.5V		0.10		mA
ISL6123, ISL6130 Stand By IC Supply Current	I_{VDD_sb}	V_{DD} = 5V, ENABLE = 0V			**1**	µA
V_{DD} Power-on Reset	V_{DD_POR}				**1**	V

NOTE:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Descriptions and Operation

The ISL612X sequencer family consists of several 4-channel voltage sequencing controllers in various functional and personality configurations. All are designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to V_{DD} + 5.3V (VQP) in a user-programmed sequence.

With the 4-channel ISL6123, ENABLE must be asserted high, and all four voltages to be sequenced must be above their respective user-programmed undervoltage lockout (UVLO) levels before programmed output turn-on sequencing can begin. Sequencing order and delay are determined by the choice of external capacitor values on the DLY_ON and

DLY_OFF pins. Once all four UVLO inputs and ENABLE are satisfied for 10ms (t_{delEN_LO}), the four DLY_ON capacitors are simultaneously charged with 1µA current sources to the DLY_Vth level of 1.27V. As each DLY_ON pin reaches the DLY_Vth level, its associated GATE turns on, with a 1µA source current to the charge pump voltage (VQP) of V_{DD} + 5.3V. Thus, all four GATEs sequentially turn on in the user defined order. Once at DLY_Vth, the DLY_ON pins discharge so they are ready when next needed.

After the entire turn-on sequence has been completed and all GATEs have reached the charge pumped voltage (VQP), a 160ms delay ($T_{\overline{RST}del}$) is started to ensure stability, after which the $\overline{RESET}$ output is released to go high.

After turn-on, if any input falls below its UVLO point for longer than the glitch filter period (~30µs), it is considered a fault. $\overline{RESET}$ and $\overline{SYSRST}$ are pulled low, and all GATEs are simultaneously also pulled low. In this mode, the GATEs are pulled low with 88mA.

Normal shutdown mode is entered when no UVLO is violated and ENABLE is deasserted. When ENABLE is deasserted, $\overline{RESET}$ is immediately asserted and pulled low. Next, all four shutdown ramp capacitors on the DLY_OFF pins are charged with a 1µA source. When any ramp-capacitor reaches DLY_Vth, a latch is set, and a current is sunk on the respective GATE pin to turn off its external MOSFET. When the GATE voltage is approximately 0.6V, the GATE is pulled down the rest of the way at a higher current level. Each individual external FET is thus turned off, which removes the voltages from the load in the user programmed sequence.

The ISL6123 and ISL6124 have the same functionality, except for the ENABLE active polarity; the ISL6124 has an $\overline{ENABLE}$ input. Additionally, the ISL6123 and ISL6130 also have an ultra low-power sleep state when ENABLE is low.

The ISL6125 has the same personality as the ISL6124, but instead of charged-pump-driven GATE outputs, it has open-drain outputs that can be pulled up to a maximum of V_{DD}.

The ISL6126 and ISL6130 are different in that their on sequence is not time determined but voltage determined. Each of the four channels operate independently. Once the IC is biased and any one of the UVLO inputs is greater than the 0.63V internal reference, and the ENABLE input is also satisfied, the associated GATE for the satisfied UVLO input turns on.

In turn, the other UVLO inputs must be satisfied for the associated GATEs to turn on. After a period of 160ms ($T_{\overline{RST}del}$) once all GATEs are fully on (GATE voltage = VQP), $\overline{RESET}$ is released to go high.

The UVLO inputs can be driven by either a previously turned-on output rail offering a voltage-determined sequence or by logic signal inputs. Any subsequent UVLO level that is less than its programmed level pulls the associated GATE and $\overline{RESET}$ output low (if previously released) but does not latch-off the other GATEs.

Predetermined turn-off is accomplished by deasserting ENABLE. This causes $\overline{RESET}$ to latch low and all four GATE outputs to follow the programmed turn-off sequence, similarly to the ISL6124.

The ISL6127 is a 4-channel sequencer pre-programmed for A-B-C-D turn-on and D-C-B-A turn-off. After all four UVLO and ENABLE inputs are satisfied for ~10ms, the sequencing starts. The next GATE in the sequence starts to ramp up once the previous GATE has reached ~VQP-1V. After a period of 160ms ($T_{\overline{RST}del}$) after the last GATE is at VQP, the $\overline{RESET}$ output is deasserted. If any UVLO is unsatisfied, $\overline{RESET}$ is pulled low, SYSRST is pulled low, and all GATEs are simultaneously turned off. When $\overline{ENABLE}$ is signaled high, the D GATE starts to pull low. Once below 0.6V, the next GATE starts to pull low, and so on, until all GATEs are at 0V. Unloaded, this turn-off sequence completes in <1ms.

This variant offers a lower cost and size implementation because the external delay capacitors are not used. Because the delay capacitors are not used, this IC cannot delay the start of subsequent GATEs. Thus, necessary stabilization or system housekeeping need to be considered.

The ISL6128 is a 4-channel device that groups the four channels into two groups of two channels each. Each group of A, B and C, D, has its own $\overline{ENABLE}$ and RESET I/O pins. All four UVLO and both $\overline{ENABLE}$s must be satisfied for sequencing to start. The A, B group turns on first, 10ms after the second $\overline{ENABLE}$ is pulled low, with A then B turning on, followed by C then D.

Once the preceding GATE = VQP, the next DLY_ON pin starts to charge its capacitor; thus, all four GATEs turn on. Approximately 160ms after D GATE = VQP, the $\overline{RESET}$ output is released to go high. Once any UVLO is unsatisfied, only the related group's $\overline{RESET}$ and two GATEs are pulled low. The related EN input must be cycled for the faulted group to be turned on again.

Normal shutdown is invoked by signaling both $\overline{ENABLE}$ inputs high, which causes the two related GATEs to shut down in reverse order from turn-on. DLY_X capacitors adjust the delay between GATES during turn-on and turn-off, but not the order.

During bias up, the $\overline{RESET}$ output is guaranteed to be in the correct state, with V_{DD} lower than 1V.

Upon power-up, the SYSRST pin follows V_{DD} with a weak internal pull-up. It is both an input and an output connection and can provide two functions. As an input, if it is pulled low, all GATEs are unconditionally shut off, and $\overline{RESET}$ pulls low (Figure 8). This input can also be used as a no-wait enabling input. If all inputs (ENABLE and UVLO) are satisfied, it does not wait through the ~10ms enable delay to initiate DLY_ON capacitor charging when released to go high. As an output, it is useful when implementing multiple sequencers in a design needing simultaneous shutdown, as with a kill switch across all sequencers. Once any UVLO is unsatisfied longer than tFIL, the related $\overline{SYSRST}$ pulls low. It also pulls low all other $\overline{SYSRST}$ inputs that are on a common connection. By doing so, it unconditionally shuts down all outputs across multiple sequencers.

Except for the ISL6128 after a fault, restart of the turn-on sequence is automatic, once all requirements are met. This allows for no interaction between the sequencer and a controller IC, if desired. The ENABLE and $\overline{RESET}$ I/O do allow for a higher

level of feedback and control, if desired. The ISL6128 requires that the related $\overline{\text{ENABLE}}$ be cycled for restart of its associated group GATEs. If no capacitors are connected between DLY_ON or DLY_OFF pins and ground, then all such related GATEs start to turn on immediately after the 10ms (TUVLOdel) ENABLE stabilization timeout has expired. The GATEs start to turn off immediately when ENABLE is asserted.

If some of the rails are sequenced together to reduce cost and eliminate the effect of capacitor variance on the timing, a common capacitor can be connected to two or more DLY_ON or DLY_OFF pins. In this case, multiply the capacitor value by the number of common DLY_X pins to obtain the desired timing.

Table 1 shows the nominal time delay on the DLY_X pins for various capacitor values, from the start of charging to the 1.27V reference. This table does not include the 10ms of ENABLE lockout delay during a start-up sequence, but it does represent the time from the end of the ENABLE lockout delay to the start of GATE transition. There is no ENABLE lockout delay for a sequence-off, so this table illustrates the delay to GATE transition from a disable signal.

TABLE 1. NOMINAL DELAY TO SEQUENCING THRESHOLD

DLY PIN CAPACITANCE	TIME(s)
Open	0.00006
100pF	0.00013
1000pF	0.0013
0.01µF	0.013
0.1µF	0.13
1µF	1.3
10µF	13

NOTE: Nom. T_{DEL_SEQ} = Capacitor (µF)*1.3MΩ.

Figure 4 shows the turn-on and Figure 5 shows the nominal turn-off timing diagram of the ISL6123 and ISL6124.

The ISL6125 is similar to the ISL6124 except that, instead of charge pumped GATE outputs, there are sequenced open-drain outputs that can be pulled up to a maximum of V_{DD}.

Delay and flexible sequencing possibilities include multiple series, parallel, or adjustable capacitors that can be used to easily fine-tune timing over that offered by standard value capacitors.

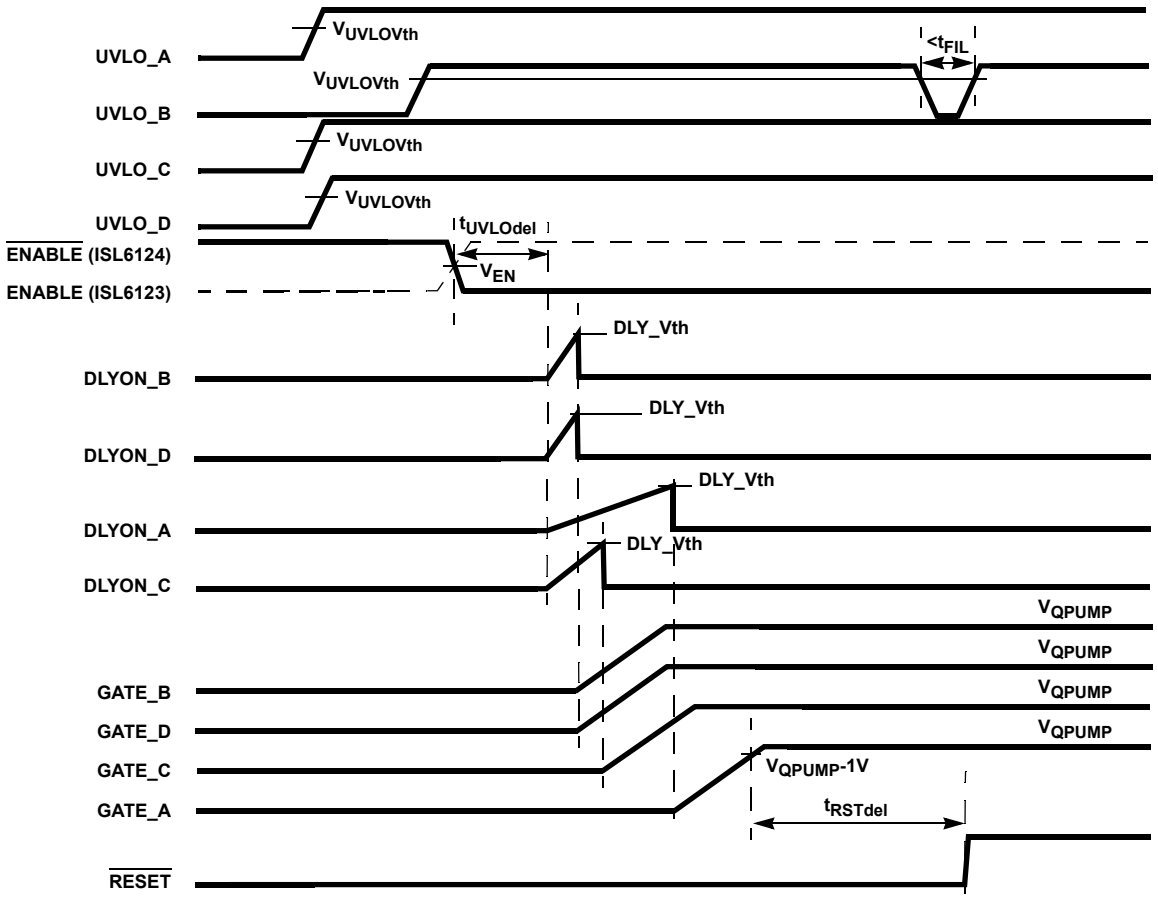


FIGURE 4. ISL6123, ISL6124 TURN-ON AND GLITCH RESPONSE TIMING DIAGRAM

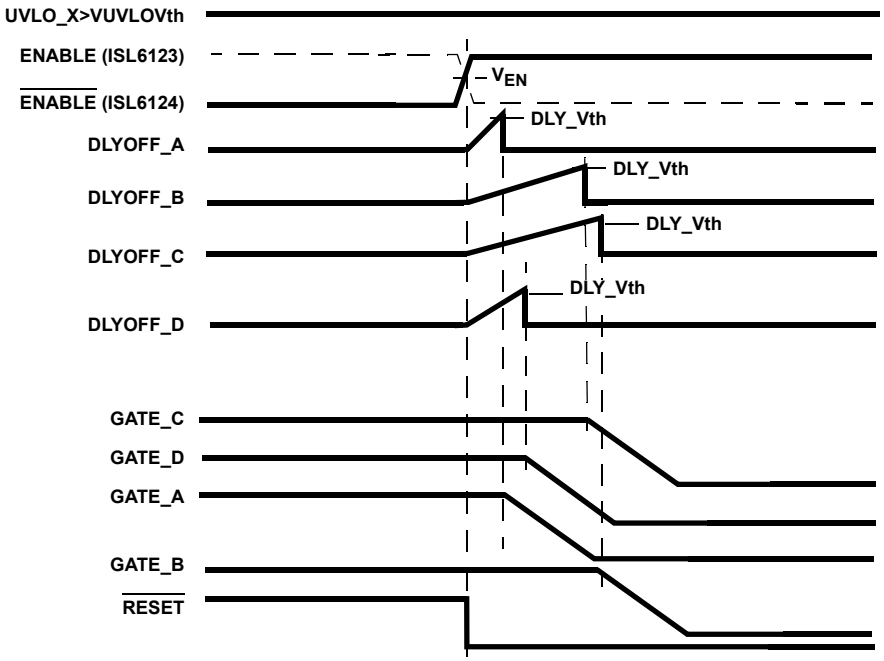


FIGURE 5. ISL6123, ISL6124 TURN-OFF TIMING DIAGRAM

Typical Performance Curves

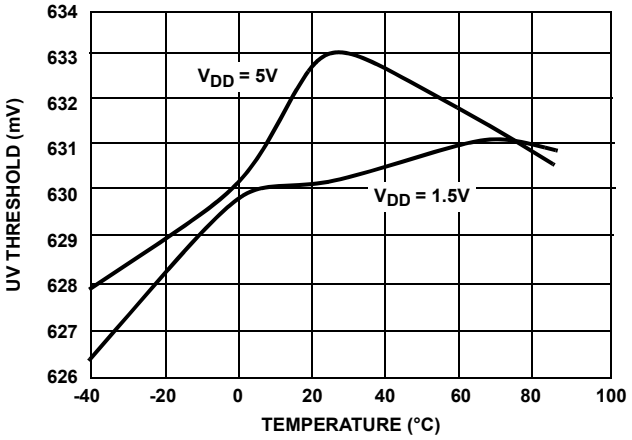


FIGURE 6. UVLO THRESHOLD VOLTAGE

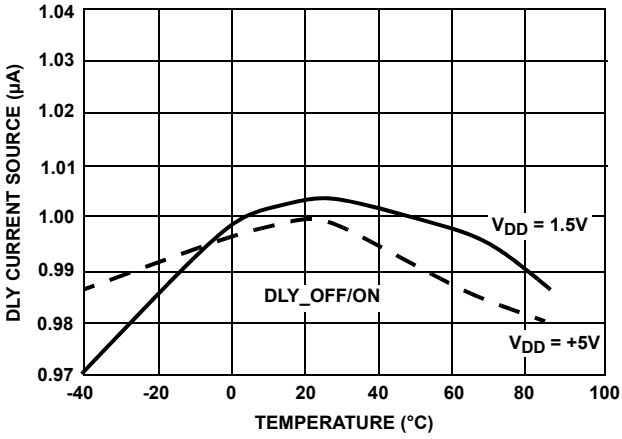


FIGURE 7. DLY CHARGE CURRENT

Typical Performance Curves (Continued)

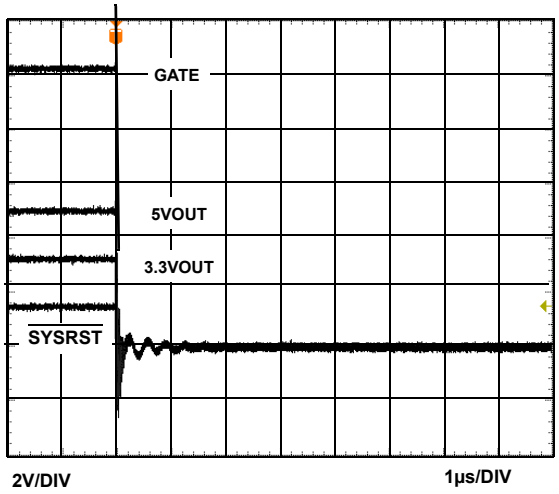


FIGURE 8. $\overline{\text{SYSRST}}$ LOW TO OUTPUT LATCH-OFF

Using the ISL6123EVAL1Z Platform

The ISL6123EVAL1Z platform layout illustrates the small implementation size for a typical 4-rail sequencing application. The platform allows evaluation of the ISL6123, ISL6124, ISL6126, ISL6127, ISL6128 and ISL6130. See Figure 17 for schematic and photograph of evaluation platform and Table 2 for the component listing.

Significant current loading of the GATE or capacitive loading of the DLY_ON and OFF pins will affect functionality and performance.

The default configuration of the ISL6123EVAL1Z circuit is built around the following design assumptions:

1. Using the ISL6123IR.
2. The four supplies being sequenced are 5V (IN_A), 3.3V (IN_B), 2.5V (IN_D) and 1.5V (IN_C). The UVLO levels are ~80% of nominal voltages. Resistors are chosen such that the total resistance of each divider is ~10k. Using standard value resistors to approximate 80% of nominal voltage supply = 0.63V on UVLO input.
3. The desired order turn-on sequence is 5V first, then 3.3V about 12ms later, then the 2.5V supply about 19ms later, and lastly, the 1.5V supply about 40ms later.
4. The desired turn-off sequence is first both 1.5V and 3.3V supplies at the same time, then the 2.5V supply about 50ms later, and lastly, the 5V supply about 72ms after that.

LED off indicates sequence has completed and $\overline{\text{RESET}}$ has released and pulled high.

The board is shipped with the ISL6123 installed and with each of the other released variant types loose packed. As this sequencer family has a common function pinout for most variants, no major modifications to the board are necessary to evaluate the other ICs. See Figure 18 for the ISL6125-specific evaluation board and schematic.

All scope shots are taken from the ISL6123EVAL1Z board. Figures 9 and 10 illustrate the desired turn-on and turn-off sequences, respectively. The sequencing order and delay between voltages sequencing is set by external capacitance values; sequences other than those illustrated can be accomplished.

Figures 11 and 12 illustrate the timing relationships between the EN input; the $\overline{\text{RESET}}$, DLY and GATE outputs; and the V_{OUT} voltage for a single channel being turned on and off, respectively. $\overline{\text{RESET}}$ is not shown in Figure 11 as it asserts 160ms after the last GATE goes high.

All IC family variants share a similar function for DLY_X capacitor charging and GATE and $\overline{\text{RESET}}$ operation. Figures 13 through 16 illustrate the principal feature and functional differences for each of the ISL6125, ISL6126, ISL6127 and ISL6128 variants.

Figure 13 shows the ISL6125 open-drain outputs being sequenced on and off, along with the $\overline{\text{RESET}}$ relationship, which is similar to all other family variants.

Figure 14 illustrates the independent input feature of the ISL6126 which, once $\overline{\text{EN}}$ is low, allows for each UVLO to be individually satisfied and for its associated GATE to turn on. Only when the last variable V_{IN} is satisfied, as shown, does $\overline{\text{RESET}}$ release, to signal all input voltages are valid.

Figure 15 shows the ISL6127 pre-programmed ABCD turn-on and DCBA turn-off order of sequencing, with minimal non-adjustable delay between each.

Figure 16 demonstrates the independence of the ISL6128, the redundant 2-rail sequencer. It shows that either one of the two groups can be turned off, and the ABCD order of restart with capacitor programmable delay, once both EN inputs are pulled low.

Using the ISL6125EVAL1Z Platform

The ISL6125EVAL1Z is the ISL6125-specific evaluation board that allows evaluation of the ISL6125 and the ISL6130 with their open-drain outputs (contact Intersil sales support with your needs). The UVLO levels, sequence and delays are programmed exactly like the other ISL612X ICs except that the ISL6125 and ISL6130 have sequenced, open-drain outputs rather than charge-pump-driven GATE outputs. See Figure 18 for the ISL6125EVAL1Z schematic and photograph and Table 3 for the component listing.

Typical Performance Waveforms

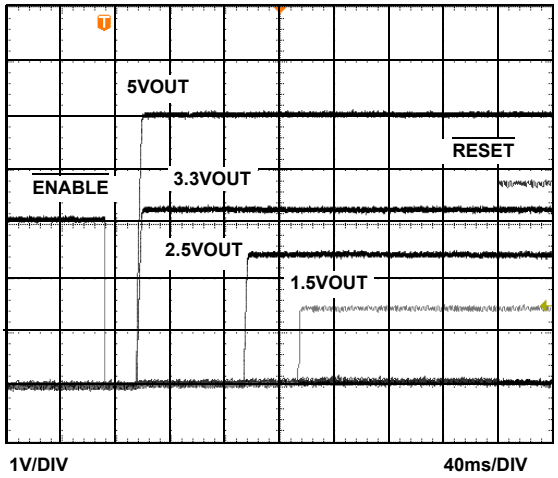


FIGURE 9. ISL6124 SEQUENCED TURN-ON

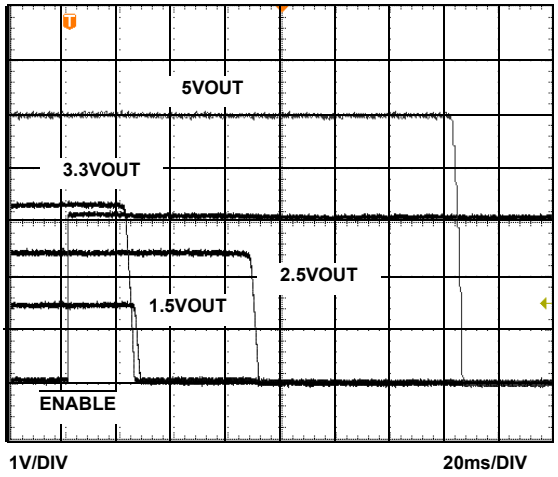


FIGURE 10. ISL6124 SEQUENCED TURN-OFF

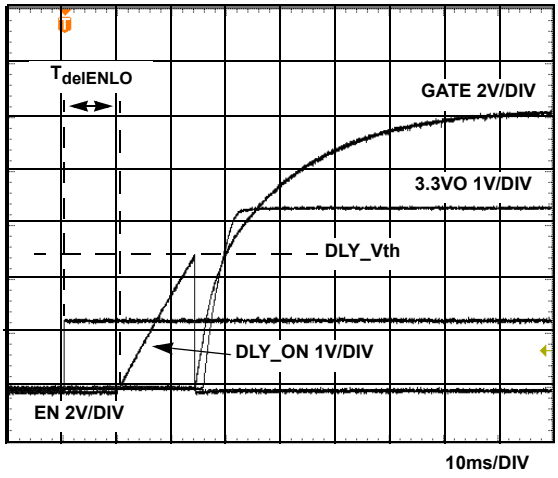


FIGURE 11. ISL6123 SINGLE CHANNEL TURN-ON

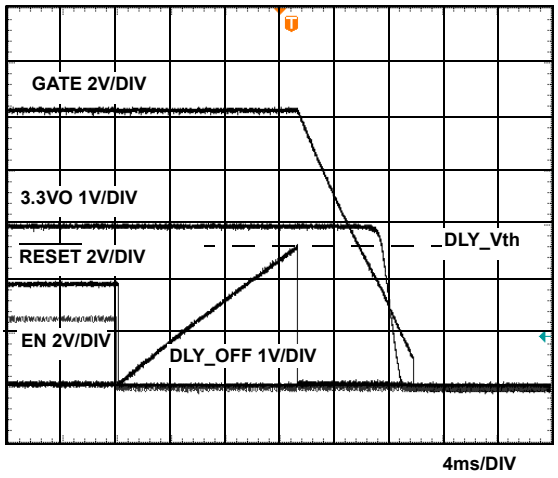


FIGURE 12. ISL6123 SINGLE CHANNEL TURN-OFF

Typical Performance Waveforms (Continued)

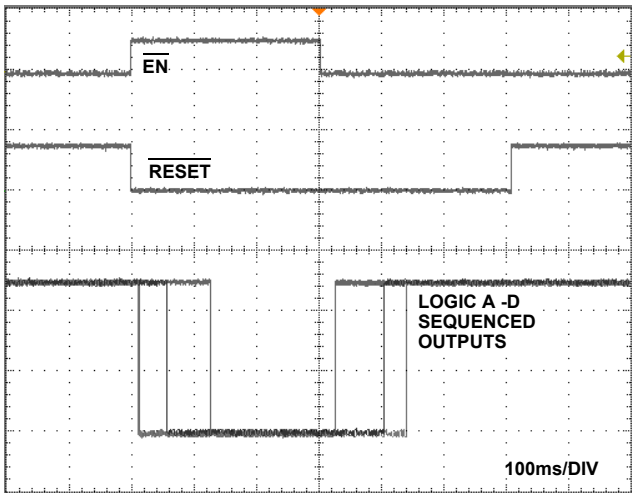


FIGURE 13. ISL6125 LOGIC OUTPUTS SEQUENCED ON AND OFF AND $\overline{\text{RESET}}$ RELATIONSHIP

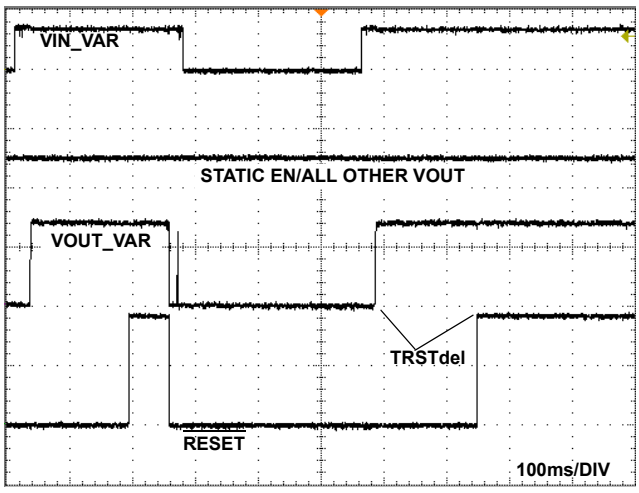


FIGURE 14. ISL6126 UVLO INPUT/OUTPUT INDEPENDENCE AND $\overline{\text{RESET}}$ RELATIONSHIP

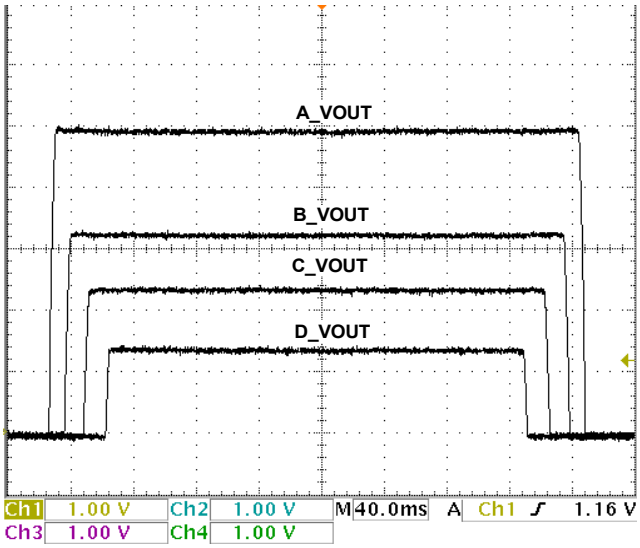


FIGURE 15. ISL6127 PRE-PROGRAMMED ABCD TURN-ON AND DCBA TURN-OFF

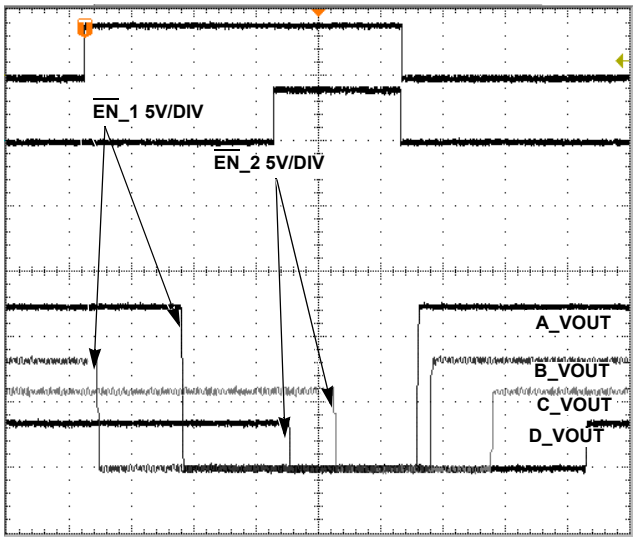


FIGURE 16. ISL6128 GROUP INDEPENDENT TURN-OFF AND DELAY ADJUSTABLE PRE-PROGRAMMED TURN-ON

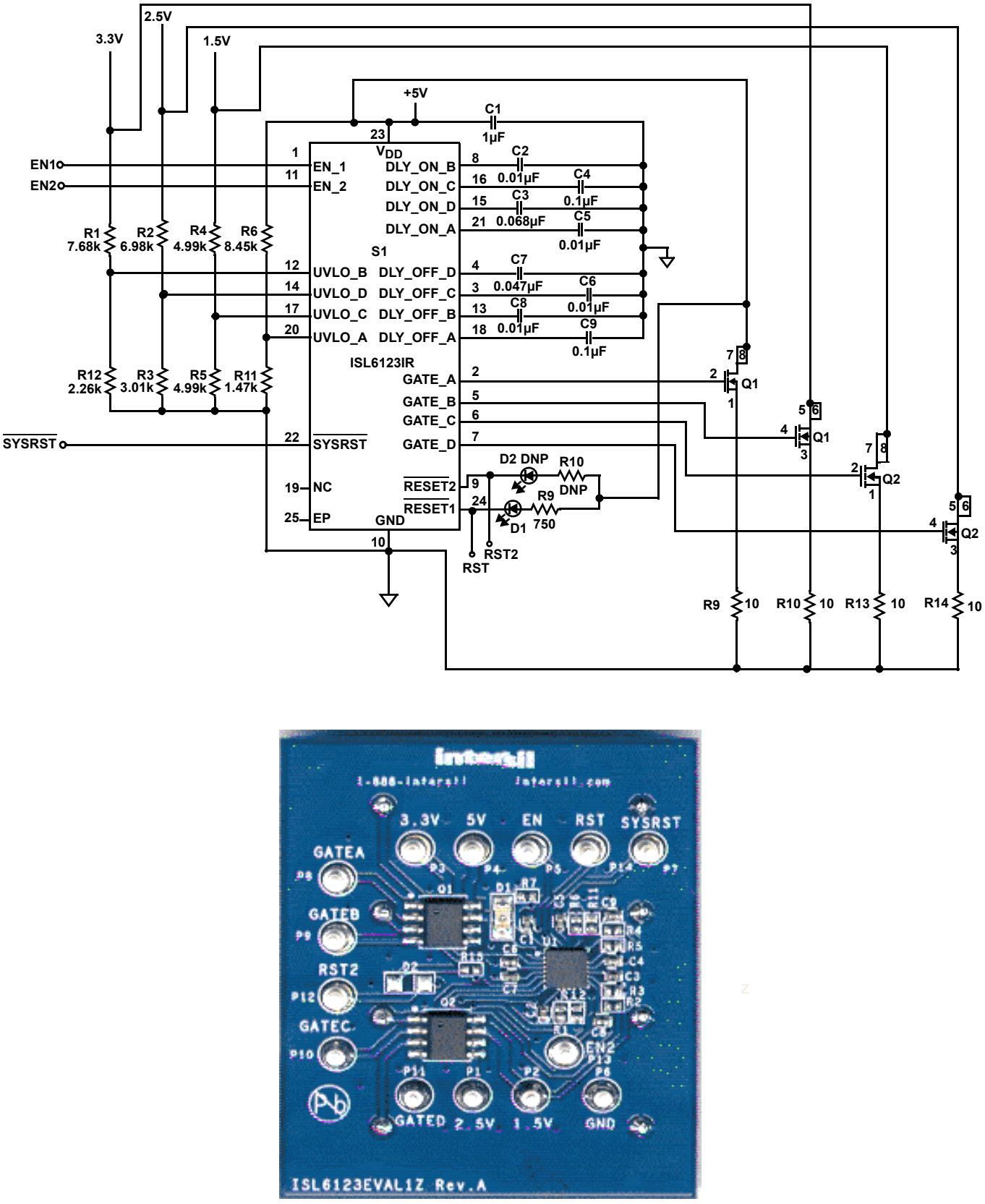
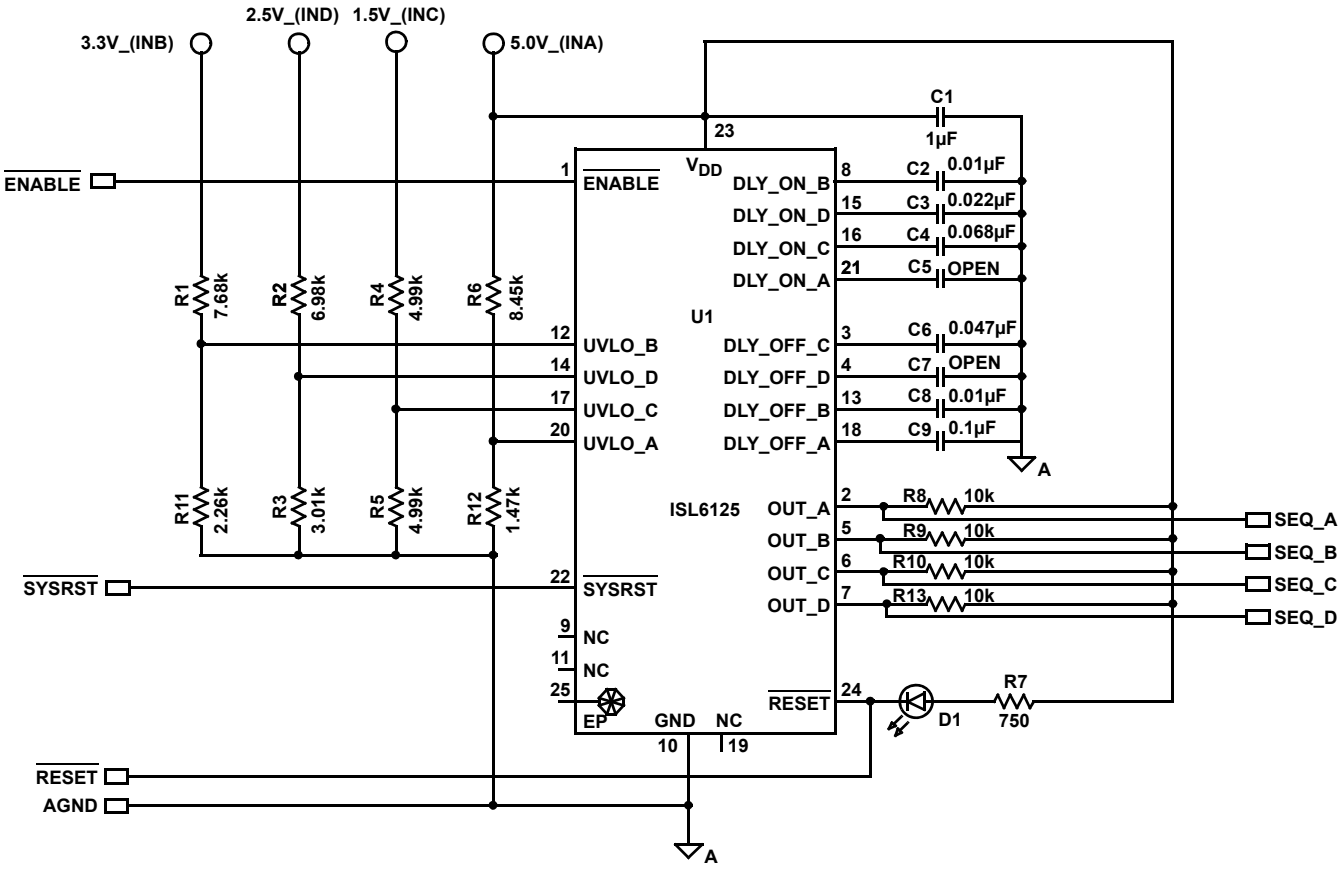


FIGURE 17. ISL6123EVAL1Z SCHEMATIC AND PHOTOGRAPH



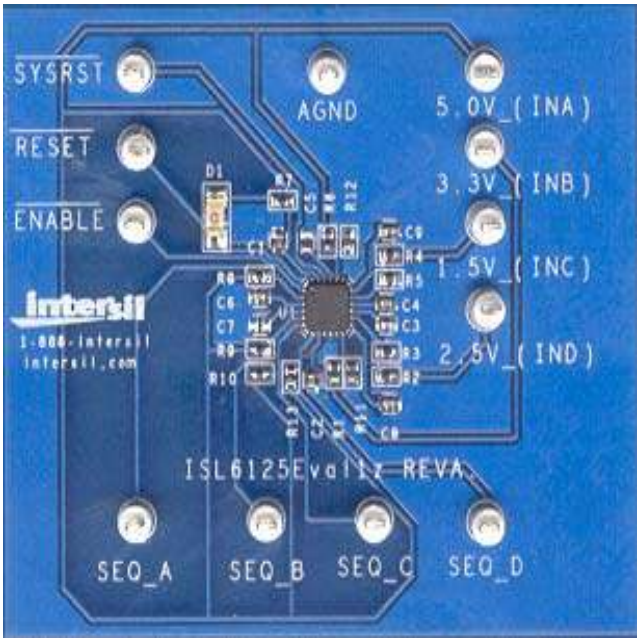


FIGURE 18. ISL6125EVAL1Z SCHEMATIC AND PHOTOGRAPH

TABLE 2. ISL6123EVAL1Z BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6123	Intersil, ISL6123, Four Supply Sequencer
Q1, Q2	Voltage Rail Switches	FDS6990S or equivalent, Dual N-Channel MOSFET
R6	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R11	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R12	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R2	2.5V to UVLO_D Resistor for Divider String	6.98kΩ 1%, 0402
R3	UVLO_D to GND Resistor for Divider String	3.01kΩ 1%, 0402
R4	1.5V to UVLO_C Resistor for Divider String	4.99kΩ 1%, 0402
R5	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	RESET LED Current Limiting Resistor	750Ω 10%, 0402
C5	5V turn-on Delay Capacitor A (~10ms)	DNP, 0402
C9	5V turn-off Delay Capacitor A (~140ms)	0.1µF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Capacitor B (~13ms)	0.01µF 10%, 6.3V, 0402
C8	3.3V turn-off Delay Capacitor B (~13ms)	0.01µF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Capacitor D (~25ms)	0.022µF 10%, 6.3V, 0402
C7	2.5V turn-off Delay Capacitor D (0ms)	DNP, 0402
C4	1.5V turn-on Delay Capacitor C (~100ms)	0.068µF 10%, 6.3V, 0402
C6	1.5V turn-off Delay Capacitor C (~60ms)	0.047µF 10%, 6.3V, 0402
C1	Decoupling Capacitor	1µF, 0402
D1	RESET Indicating LED	0805, SMD LEDs Red
D2	RESET Indicating LED	DNP
R9	5V Load Resistor	10W 20%, 3W
R10	3.3V Load Resistor	10Ω 20%, 3W
R13	2.5V Load Resistor	10Ω 20%, 3W
R14	1.5V Load Resistor	10Ω 20%, 3W
	Test Points Labeled as to Function	

TABLE 3. ISL6125EVAL1Z COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6125, Four Supply Sequencer	Intersil, ISL6125, Four Supply Sequencer with Open Drain Outputs
R6	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R12	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R11	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R2	2.5V to UVLO_D Resistor for Divider String	6.98kΩ 1%, 0402
R3	UVLO_D to GND Resistor for Divider String	3.01kΩ 1%, 0402
R4	1.5V to UVLO_C Resistor for Divider String	4.99kΩ 1%, 0402
R5	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	RESET LED Current Limiting Resistor	750Ω 10%, 0805
C5	5V turn-on Delay Capacitor A	DNP, 0402
C9	5V turn-off Delay Capacitor A (135ms)	0.1µF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Capacitor B (13.7ms)	0.01µF 10%, 6.3V, 0402
C8	3.3V turn-off Delay Capacitor B (13.7ms)	0.01µF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Capacitor D (28ms)	0.022µF 10%, 6.3V, 0402
C7	2.5V turn-off Delay Capacitor D	DNP, 0402
C4	1.5V turn-on Delay Capacitor C (98ms)	0.068µF 10%, 6.3V, 0402
C6	1.5V turn-off Delay Capacitor C (59ms)	0.047µF 10%, 6.3V, 0402
C1	Decoupling Capacitor	0.1µF, 0805
D1	$\overline{\text{RESET}}$1 Indicating LED	0805, SMD LED
R8	SEQ_OUTPUT_A Pull-Up Resistor	10kΩ, 0402
R9	SEQ_OUTPUT_B Pull-Up Resistor	10kΩ, 0402
R10	SEQ_OUTPUT_C Pull-Up Resistor	10kΩ, 0402
R13	SEQ_OUTPUT_D Pull-Up Resistor	10kΩ, 0402

Application Implementations

Multiple Sequencer Implementations

The ISL6123, ISL6124, ISL6125 and ISL6127 devices can be configured to control sequencing of more than four voltages. A particular configuration may be preferable to another, depending on concerns. The fundamental questions to determine which configuration is best suited for your applications are:

1. What level of voltage assurance is needed prior to sequencing on, and can the voltage supplies be grouped into high and low criticality?
2. Is there a critical maximum time window in which all supplies must be present at load, or is there a first and a second group preference, possibly with some work done in between the two groups of voltages being present?

Three configurations are described and illustrated here.

In applications for which the integrity of critical voltages must be assured prior to sequencing, additional monitoring of the critical supplies is needed. If voltage compliance is critical for either undervoltage or overvoltage, voltage supervisors can be used to provide this additional assurance across multiple sequencers. Figure 19 is a block diagram of a voltage-compliant, high-assurance, low-risk configuration showing the ISL6131 or ISL6132 supervisor and a mix of FET switched outputs and logic output sequencers (ISL6124 and ISL6125 ICs).

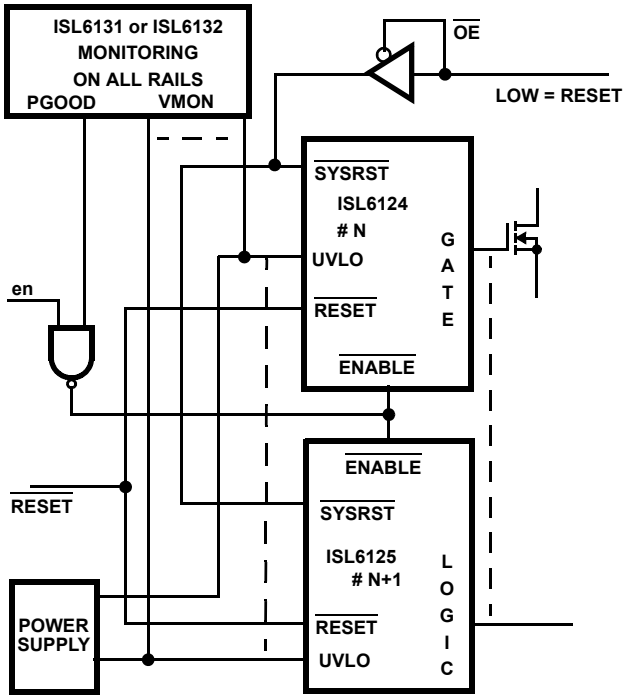


FIGURE 19. ISL612X AND ISL613X VOLTAGE COMPLIANT SEQUENCING BLOCK DIAGRAM

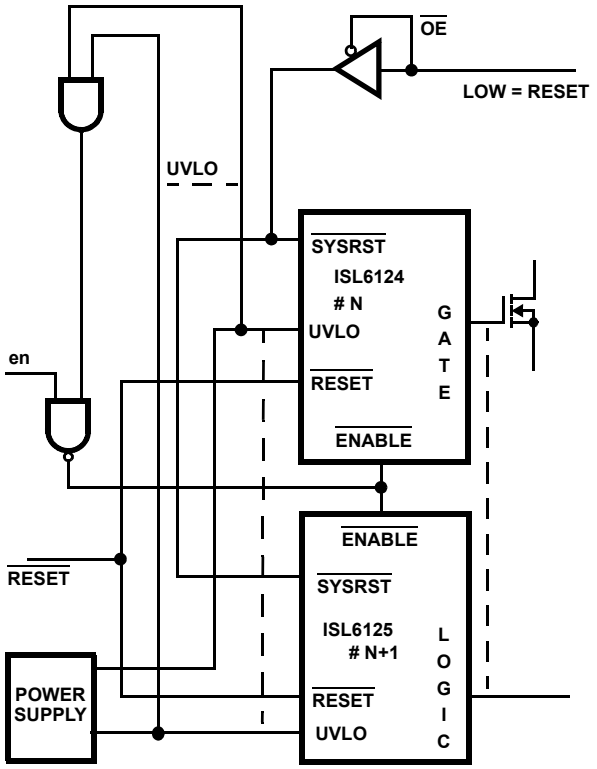


FIGURE 20. MULTIPLE ISL612X USING LOGIC GATES FOR VOLTAGE PRESENCE DETECT

If the mere presence of some voltage potential is adequate prior to sequencing on, then a small number of standard logic and gates can be used to accomplish this. The block diagram in Figure 20 illustrates this voltage presence configuration.

In either case, the sequencing is straightforward across multiple sequencers, as all DLY_ON capacitors simultaneously start charging ~10ms after the common ENABLE input signal is delivered. This allows the choice of capacitors to be related to each other and is no different than using a single sequencer. When the common enabling signal is de-asserted, these configurations execute the turn-off sequence across all sequencers as programmed by the DLY_OFF capacitor values.

In both cases, with all the $\overline{\text{SYSRST}}$ pins bused together, once the turn-on sequence is complete, simultaneous shutdown upon any UVLO input failure is assured. $\overline{\text{SYSRST}}$ output momentarily pulls low and turns off all GATE and LOGIC outputs.

Some applications may require or allow groups of supplies to be brought up in sequence and for supplies within each group to be sequenced. Figure 21 shows a configuration that allows the first group of supplies to turn on before the go second group starts. This arrangement does not necessarily preclude adding the assurance of all supplies prior to turn-on sequencing, as previously shown. It does prevent the turn-on sequence from completing, if there is one unsatisfied UVLO input in a group.

This configuration involves waiting through the $T_{UVLOdel}$ and $T_{\overline{RST}del}$ (total of ~160ms) for each sequencer IC in the chain before the final $\overline{\text{RESET}}$ releases. Once ENABLE on the first sequencer is de-asserted, all $\overline{\text{RESET}}$ outputs quickly pull low. This allows the sequenced turn-off of this configuration to ripple through several banks as quickly as the user-programmed (by DLY_OFF) sequence capacitors allow.

Again, with common bused $\overline{\text{SYSRTS}}$ pins, simultaneous shutdown of all GATEs and LOGIC down upon an unsatisfied UVLO input is assured, once all FETs or LOGIC outputs are on. If a GATE drive option IC is used to drive both FETs and logic signals, then care must be taken to ensure the charged pump GATE does not overdrive and damage the logic input. A simple resistor divider can be used to lower the GATE to a suitable voltage for the logic input, as shown in Figure 21.

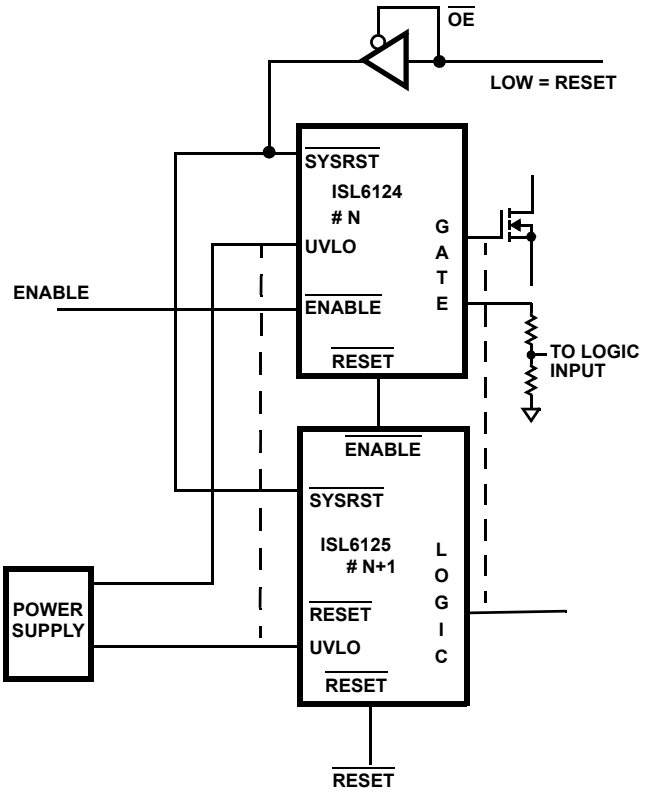


FIGURE 21. MULTIPLE ISL612X SERIAL CONFIGURATION

Voltage Tracking

In some applications, voltages may have to track each other as they ramp up and down, whereas others may just need sequencing. In these cases, tracking can be accomplished and has been demonstrated over a wide range of load currents (1A to 10A) and load capacitances (10µF to 3300µF) with the ISL612X family. Figure 22 and Figure 23 illustrate output voltage ramping tracking performance. Note that differences are less than 0.5V. With the relevant GATE pins tied together in a star pattern, so that resistance between any two GATE pins is equivalent (1k to 10k), GATE ramping voltage is shared. With the same or similar enough FETs, this behavior is also observed.

It is suggested that this circuit implementation be prototyped and evaluated for the particular expected loads prior to committing to manufacturing build.

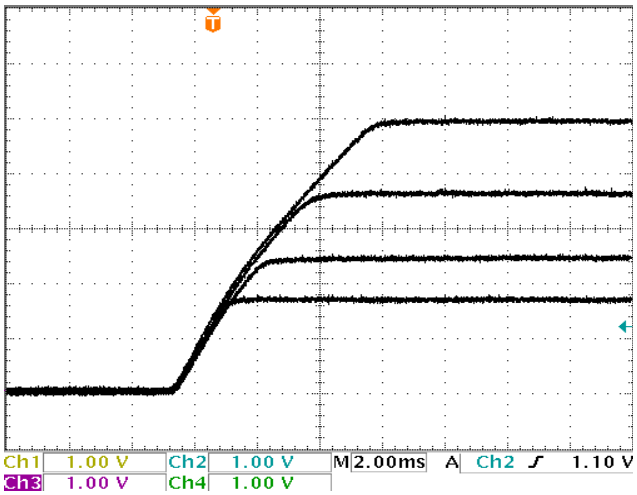


FIGURE 22. OUTPUT VOLTAGE ON LOW TO HIGH TRACKING

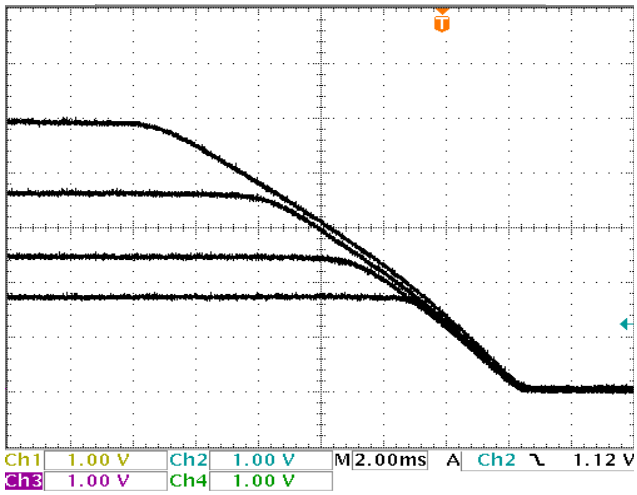


FIGURE 23. OUTPUT VOLTAGE ON HIGH TO LOW TRACKING

Negative Voltage Sequencing

The ISL612X family can use the charged pump GATE output to drive FETs that would control and sequence negative voltages down to a nominal -5V with minimal additional external circuitry. Figure 24 shows simultaneous turn-on of the 5V bipolar supplies, and then simultaneous turn-off of the +2.5V and both positive supplies after the -5V. Figure 25 shows the minimal additional external circuitry to accomplish this. The 5V zener diode is used to level-shift the GATE drive down by 5V to prevent premature turn-on when GATE = 0V. Once GATE drive voltage > Vz, then FET Vgs > 5V, ensuring full turn-on once GATE gets to V_{DD} + 5.3V. Turn-on and turn-off ramp rates can be adjusted with the FET gate series resistor value. The -V rail is sequenced normally via the DLY_X capacitor value, although adjustments in prototyping should be factored in to fine-tune for actual circuit requirements.

Figures 26 and 27 illustrate a high-accuracy -V detection circuit using the ISL6131 and a low-cost, low-accuracy -V detection circuit, respectively.

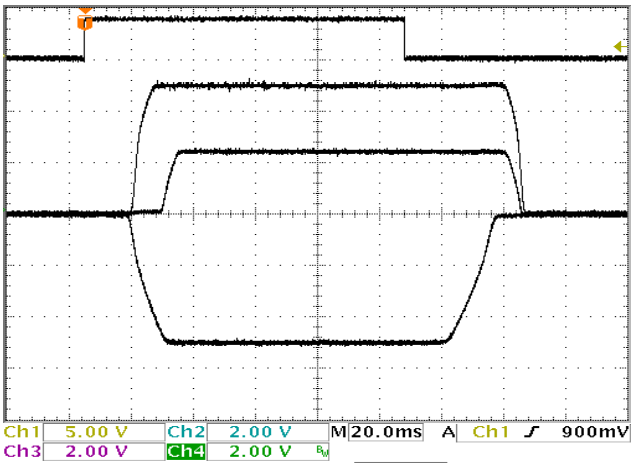
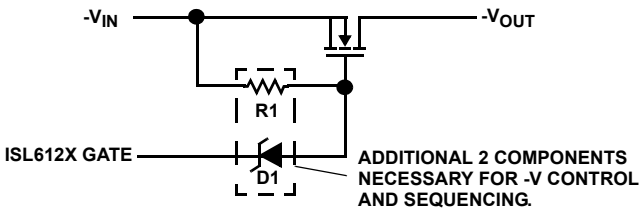
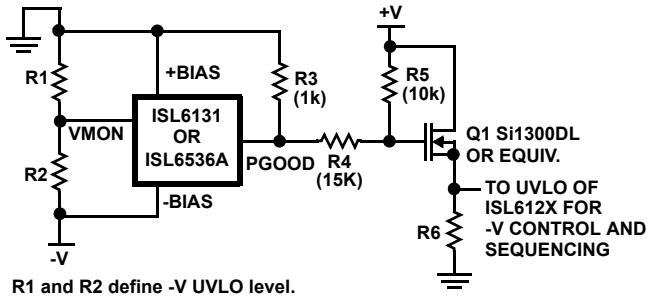


FIGURE 24. ±VOLTAGE SEQUENCING



D1 necessary to prevent premature turn-on. R1 is used to hold FET Vgs = 0V until D1 Vz is overcome. R1 value can be changed to adjust -V ramp rates. Choose an R1 value between 4MW and 10MW initially, and fine-tune resistor value for the particular need.

FIGURE 25. -VOLTAGE FET DRIVE CIRCUIT



R1 and R2 define -V UVLO level.
R3 ensures supervisor (ISL6131 or ISL6536A) PGOOD pull-up.
R4 and R5 provide Q1 gate bias between 0V and +V to 0V (resistor values suitable for -V = -5V and +V = +3.3V).

FIGURE 26. HIGH ACCURACY -V LOCK OUT

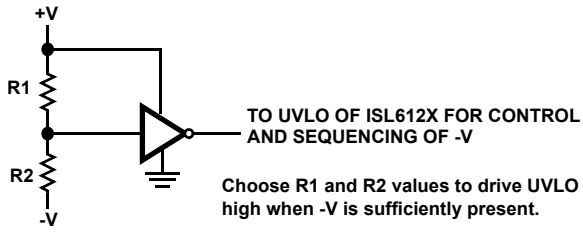


FIGURE 27. LOW ACCURACY -V PRESENCE DETECTION

Application Considerations

Timing Error Sources

In any system there are variance contributors. For the ISL612x family, timing errors are mainly contributed by three sources.

Capacitor Timing Mismatch Error

Obviously, the absolute capacitor value is an error source; thus, lower-percentage tolerance capacitors help to reduce this error source. Figure 28 illustrates a difference of 0.57ms between two DLY_X outputs ramping to DLY_X threshold voltage. These 5% capacitors were from a common source. In applications where two or more GATEs or LOGIC outputs must have concurrent transitions, it is recommended that a common GATE drive be used to eliminate this timing error.

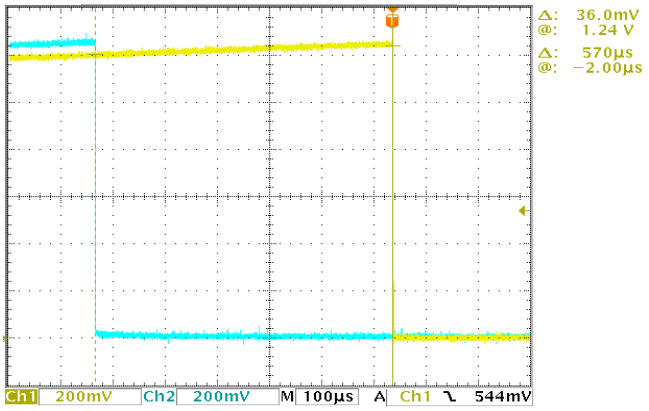


FIGURE 28. CAPACITOR TIMING MISMATCH

DLY_X Threshold Voltage and Charging Current Mismatch

The two other error sources come from the IC itself and are found across the four DLY_X outputs. These errors are the DLY_X threshold voltage (DLY_Vth) variance when the GATE_X charging and discharging current latches are set, and the DLY_X charging current (DLY_ichg) variances to determine the time to next sequencing event. Both of these parameters are bounded by specification. Figure 29 shows that, with a common capacitor, the typical error contributed by these factors is insignificant, since both DLY_X traces overlay each other.

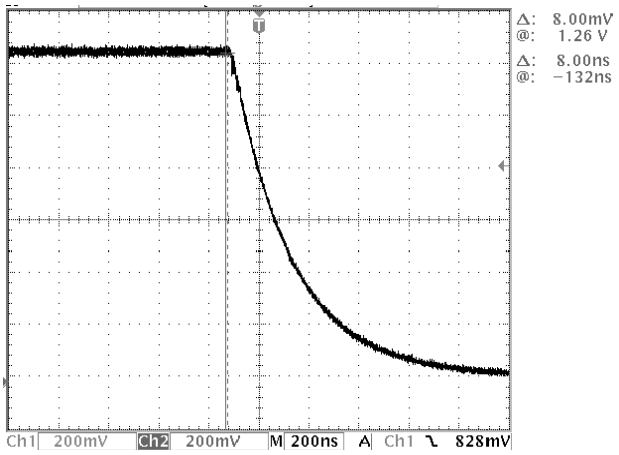


FIGURE 29. DLY_VTH AND DLY_ICHG TIMING MISMATCH

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
6/13/2012	FN9005.12	Added ISL6125 specific information throughout the document for clarification / differentiation. - Page 1, Figure 1: “Improved Typical Application Diagram” - Page 2, Figure 2“Improved ISL6125 Application Diagram” - Page 3, Pin Configuration diagram ISL6123, ISL6124, ISL6125 table, added "OUTPUT_A, OUTPUT_B, OUTPUT_C and OUTPUT_D,” to diagram. -Page 4, Pin Descriptions table added OUTPUT_A, OUTPUT_B, OUTPUT_C and OUTPUT_D
5/24/2011	FN9005.11	- On Page 1, Features: added “ENABLE” to Active High information for ISL6123 and ISL6130. - On Page 2, Ordering Information table: updated evaluation board; changed ISL612XSEQEVAL1Z to ISL6123EVAL1Z. Removed obsolete parts: ISL6123IR, ISL6124IR, ISL6125IR, ISL6126IR, ISL6127IR, ISL6128IR. - On Page 4, Pin Descriptions: changed Description for ENABLE/$\overline{\text{ENABLE}}$ pins from “ISL6123, ISL6124, ISL6125, ISL6126, ISL6127 and ISL6130 have ENABLE.” to “ISL6123 and ISL6130 have ENABLE, and ISL6124, ISL6125, ISL6126 and ISL6127 have $\overline{\text{ENABLE}}$.” - On Page 6, Thermal Information: changed theta-ja from 48 to 46; changed theta-jc from 9 to 8. - On Page 6, Electrical Specifications: added "ISL6125 Open Drain" specs for "Open Drain On Resistance”. - On Page 11: changed heading “Using the ISL612XSEQEVAL1Z Platform” to “Using the ISL6123EVAL1Z Platform” and edited this section to reflect attributes of revised evaluation board. - On Page 14: replaced Figure 16, "EVAL BOARD CHANNEL 1 SCHEMATIC AND ISL612XSEQEVAL1Z PHOTOGRAPH” with "ISL6123EVAL1Z SCHEMATIC AND PHOTOGRAPH” - On Page 16: replaced Table 2, "ISL612XSEQEVAL1Z BOARD CHANNEL 1 COMPONENT LISTING” with "ISL6123EVAL1Z BOARD COMPONENT LISTING”
10/15/2008	FN9005.10	Corrected pinout information in table and diagram.
2/27/2008	FN9005.9	- Updated evaluation boards discussion to indicate Pb-free versions throughout document. - Clarified pinouts and pin description tables. - Added Pb-free reflow link to Thermal Information.
2/5/2007	FN9005.8	Added ISL6130 to datasheet.
10/12/2006	FN9005.7	Made corrections and clarifications to discussions of evaluation board.
3/9/2006	FN9005.6	Clarified block diagram and applications text.
12/2/2005	FN9005.5	- Clarified text of SYSRST functional description. - Added bias and several SYSRST# and RST# typical parameters numbers. - Cleared up tracking scope shot mismatch.
6/10/2005	FN9005.4	Improved ESD to 2.5kV.
8/18/2004	FN9005.3	Added Pb-free options.
1/14/2004	FN9005.2	Minor edits
10/3/2003	FN9005.1	Minor edits
7/15/2003	FN9005.0	New document

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Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL6123, ISL6124, ISL6125, ISL6126, ISL6127, ISL6128, ISL6130.

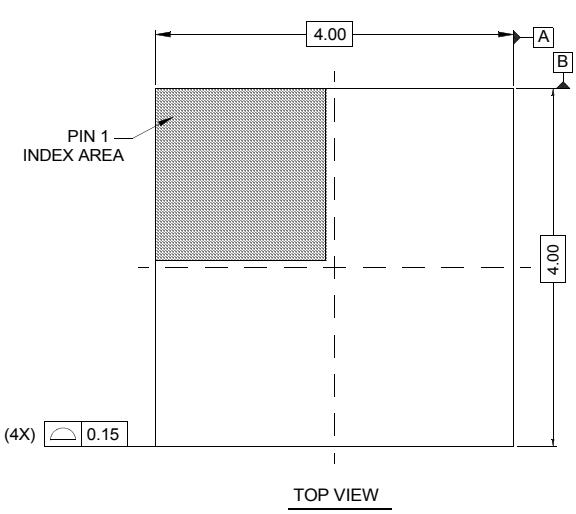
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff.

FITs are available from our website at: http://rel.intersil.com/reports/search.php

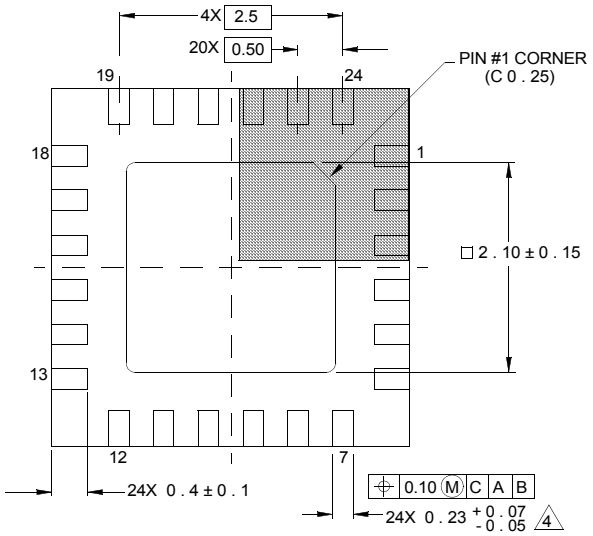
Package Outline Drawing

L24.4x4

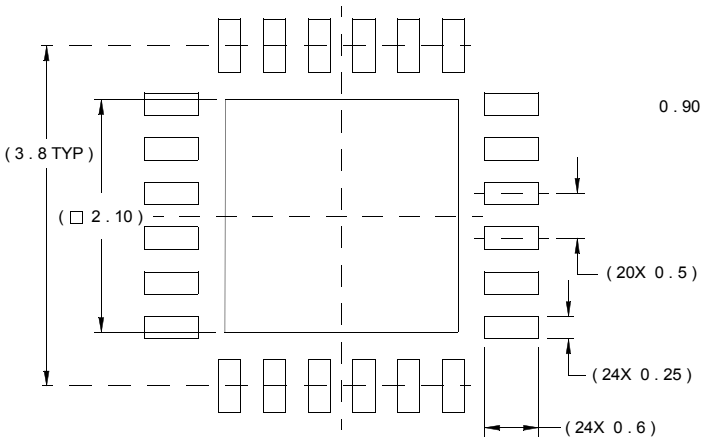
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



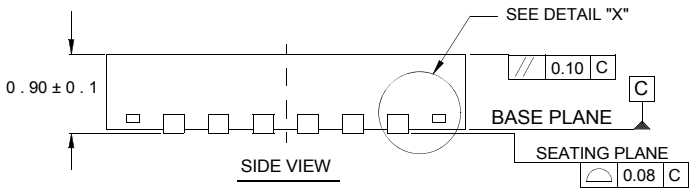
TOP VIEW



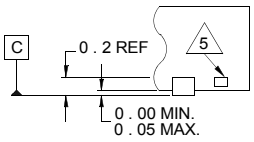
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.