FEATURES

- **Complementary Emitter-Coupled-Logic Outputs**
- **50Ω Line Driving Capability**
- **Excellent Stability; Resists Oscillation**
- **Propagation Delay at 5mV Overdrive, Over Full Operating Temperature Range:**
  - **Industrial Temperature Range ..... 9.5ns Max**
  - **Military Temperature Range ..... 12.0ns Max**
- **Over 100MHz Output Bandwidth**
- **Space-Saving 8-Pin DIP**
- **High Performance, Low Price**
- **Available in Die Form**

ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP 8-PIN	SO 8-PIN	
CPM08BZ*	—	MIL
CMP08FZ	CMP08FS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The CMP-08 is a very high-speed voltage comparator which provides complementary Emitter-Coupled-Logic (ECL) outputs. It is particularly suitable for level-crossing detection and sinewave-squaring applications with input amplitude as low as 2 millivolts.

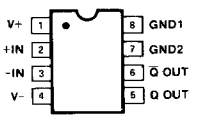
Fiber-optics and communications circuits will find the CMP-08 attractive. Its high sensitivity, low drift, stability, and wide-band operation make CMP-08 excellent for signal recovery and pulse-shaping applications. With its ECL-logic outputs and bandwidth over 100MHz, the performance of CMP-08 is double that of comparable TTL-output devices.

The CMP-08 offers consistent delay, with low delay variation as a function of temperature or overdrive. This provides excellent timing resolution in 10-30MHz computer peripheral applications. If necessary, conversion to TTL levels can be easily performed after initial processing with ECL logic.

The CMP-08 is specified for operation using +5V and −5.2V supplies. With 5% supply tolerance, input voltage range includes −3.0V to +2.7V over all operating temperatures. In applications such as video systems, the CMP-08 input voltage range and sensitivity permit a dynamic range of over 60dB to be achieved. For added flexibility, the positive input voltage limit may be extended by using a +6V positive supply rather than +5V. It is also possible to use a −5V supply, when the −5.2V supply is not available.

When AC system layout rules are used, the excellent stability of CMP-08 eliminates the need for an on-chip latch. If needed, the latch function may be performed within digital logic. With its space-saving 8-pin DIP and low price, the CMP-08 provides an excellent alternative to Am685-type devices.

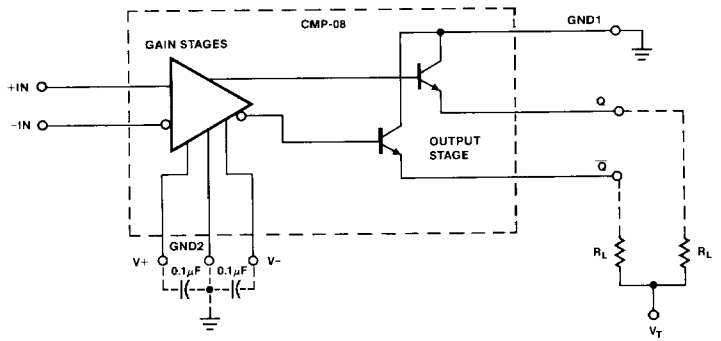
PIN CONNECTIONS



8-PIN CERDIP (Z-Suffix)

8-PIN SO (S-Suffix)

CONNECTION DIAGRAM



THE CMP-08 INCLUDES OPEN-EMITTER OUTPUTS. OUTPUT TERMINATION RESISTORS R_L, TO TERMINATION VOLTAGE V_T, MUST BE PROVIDED BY THE USER. SEE APPLICATIONS INFORMATION FOR SUGGESTED VALUES.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage ..... +6.5V
Negative Supply Voltage ..... –6.0V
Input Voltage ..... ±4V
Differential Input Voltage ..... ±6V
Output Current 30mA
Operating Temperature Range (Note 2)
CMP-08B ..... –55°C to +125°C
CMP-08F ..... –40°C to –85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... –65°C to +165C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin SO (S)	160	44	°C/W

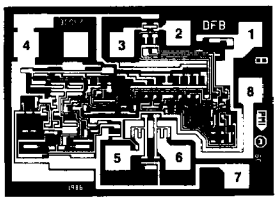
NOTES:
1. Beyond which the useful life may be impaired.
2. Device in thermal equilibrium with 500 LFPM transverse airflow.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V– = –5.2V, V_T = –2V, R_L = 50Ω; –55°C ≤ T_A ≤ +125°C for CMP-08B; –40°C ≤ T_A ≤ +85°C for CMP-08F, unless otherwise noted.

			CMP-08F			CMP-08B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 50Ω	–2.5	—	+2.5	–3.0	—	+3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	—	5	—	—	5	—	µV/°C
Input Offset Current	I_{OS}		–1.3	—	+1.3	–1.6	—	+1.6	µA
Input Bias Current	I_B		—	—	13	—	—	16	µA
Input Voltage Range	CMVR	(Note 3)	–3.0	—	+2.7	–3.0	—	+2.7	V
Common-Mode Rejection Ratio	CMRR		80	—	—	80	—	—	dB
Power Supply Rejection Ratio	PSRR	(Note 1)	80	—	—	80	—	—	dB
Small Signal Gain, Linear Region	A_V	T_A = 25°C	800	1200	—	800	1200	—	V/V
Input Resistance	R_{IN}	T_A = 25°C	6	—	—	6	—	—	kΩ
Input Capacitance	C_{IN}	T_A = 25°C	—	3	—	—	3	—	pF
Output HIGH Voltage (Note 2)	V_{OH}	T_A = 25°C T_A = T_A (MIN) T_A = T_A (MAX)	–0.960 –1.060 –0.890	— — —	–0.810 –0.890 –0.700	–0.960 –1.100 –0.850	— — —	–0.810 –0.920 –0.620	V
Output LOW Voltage (Note 2)	V_{OL}	T_A = 25°C T_A = T_A (MIN) T_A = T_A (MAX)	–1.950 –1.950 –1.950	— — —	–1.650 –1.660 –1.625	–1.950 –1.950 –1.950	— — —	–1.650 –1.660 –1.575	V
V+ Supply Current	I+		—	—	15	—	—	15	mA
V– Supply Current	I–		—	—	26	—	—	26	mA
SWITCHING CHARACTERISTICS									
Propagation Delay	t_{PD}	(Notes 4, 6)	—	6.5	9.5	—	6.5	12	ns
Output Edge Rate	t_R, t_F	T_A = 25°C (Note 5)	—	2	—	—	2	—	ns

NOTES:
1. Tested with a ±5% supply variation.
2. Specifications apply when the device is in thermal equilibrium with 500 LFPM transverse airflow. Actual test limits must be corrected for thermal offset between test conditions and airflow equilibrium.
3. Specified input voltage range is for V+ = +5V ±5% and for V– = –5.2V ±5%. CMVR will change if other supply voltages are used. Recommended supply limits are V+ = +4.75V to +6.3V, V– = –4.7V to –5.7V. CMVR is guaranteed by I_B and CMRR tests.
4. Propagation delay is specified for 100mV input voltage step, 5mV overdrive beyond the offset voltage.
5. Output rise/fall time 20%–80% with input amplitude 20mV peak-to-peak, 2ns input rise/fall time.
6. This parameter is sample tested at 25°C. Typical number represents 25°C operation.

DICE CHARACTERISTICS



DIE SIZE: 0.056 × 0.041 inch, 2296 sq. mils (1.42 × 1.04 mm, 1.48 sq. mm)

1. **V+** **Positive Supply**
2. **+IN** **Noninverting Input**
3. **−IN** **Inverting Input**
4. **V−** **Negative Supply**
5. **Q** **True Output**
6. **$\overline{Q}$** **Complement Output**
7. **GND2** **Circuit Ground**
8. **GND1** **Output Ground**

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V+ = +5V, V− = −5.2V, V_T = −2V, R_L = 50Ω, T_A = 25°C, unless otherwise noted.

			CMP-08N		
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	R_S = 50Ω	−2.2	+2.2	mV
Input Offset Current	I_{OS}		−1.0	+1.0	μA
Input Bias Current	I_B		—	10	μA
Input Voltage Range	CMVR	(Note 1)	−3.0	+2.7	V
Common-Mode Rejection Ratio	CMRR		80	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +4.75V to +5.25V, V− = −4.94V to −5.46V	80	—	dB
Small-Signal Gain, Linear Region	A_V		800	—	V/V
Input Resistance	R_{IN}		6	—	kΩ
Output HIGH Voltage	V_{OH}	(Note 2)	−0.960	−0.810	V
Output LOW Voltage	V_{OL}	(Note 2)	−1.950	−1.650	V
V+ Supply Current	I+		—	15	mA
V− Supply Current	I−		—	26	mA

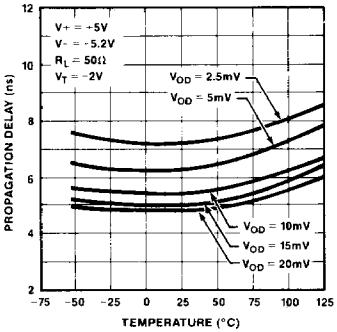
NOTES:

1. CMVR is measured using V+ = +4.75V, V− = −4.94V (worst-case).
2. The V_{OH} and V_{OL} specifications are temperature sensitive. Since T_A = 25°C at wafer sort does not correspond to the same junction temperature as T_A = 25°C for packaged units, the actual test limits are corrected to allow for temperature offset.

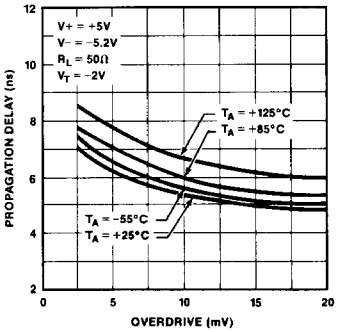
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

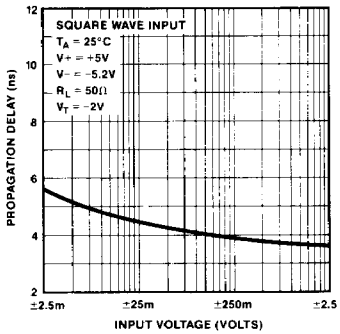
PROPAGATION DELAY vs TEMPERATURE



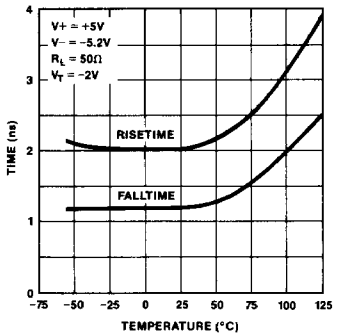
PROPAGATION DELAY vs INPUT OVERDRIVE



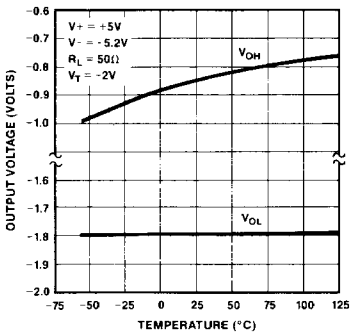
PROPAGATION DELAY vs INPUT SIGNAL LEVEL



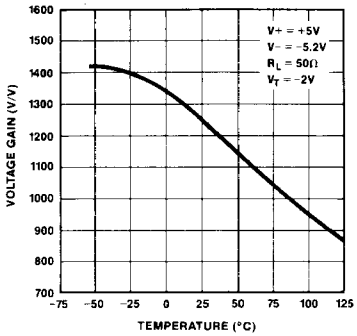
OUTPUT RISE AND FALL TIME vs TEMPERATURE



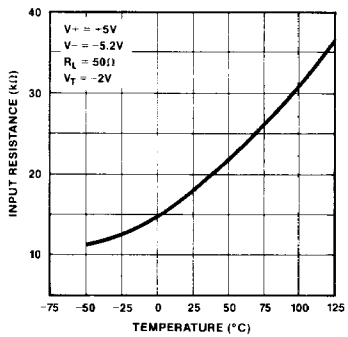
OUTPUT LEVEL vs TEMPERATURE



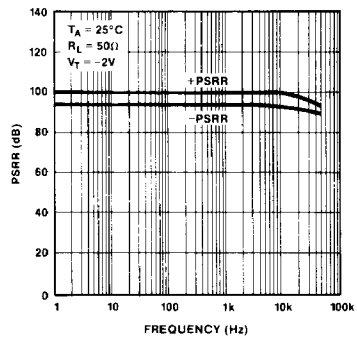
VOLTAGE GAIN vs TEMPERATURE



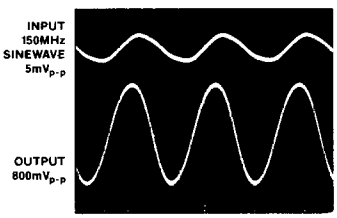
INPUT RESISTANCE vs TEMPERATURE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

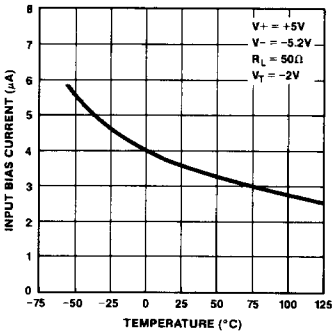


RESPONSE TO 150MHz INPUT SIGNAL

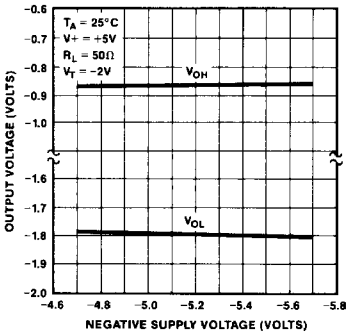


TYPICAL PERFORMANCE CHARACTERISTICS

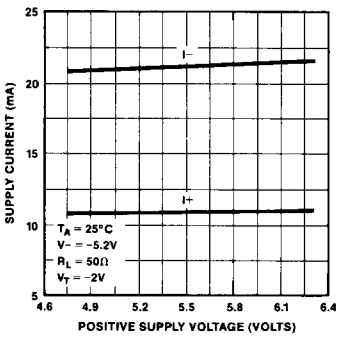
INPUT BIAS CURRENT vs TEMPERATURE



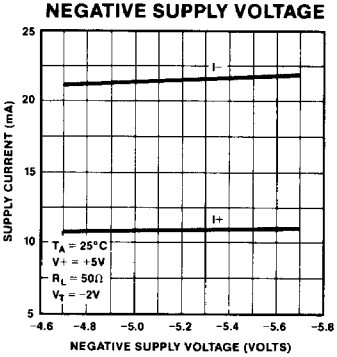
OUTPUT LEVEL vs NEGATIVE SUPPLY VOLTAGE



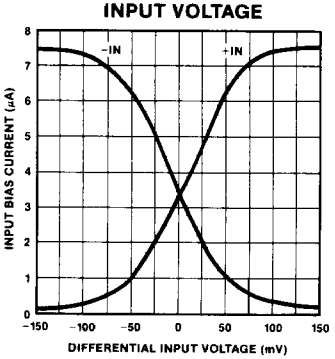
SUPPLY CURRENT vs POSITIVE SUPPLY VOLTAGE



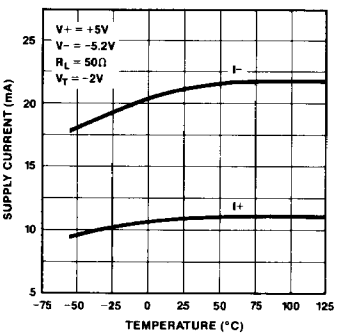
SUPPLY CURRENT vs NEGATIVE SUPPLY VOLTAGE



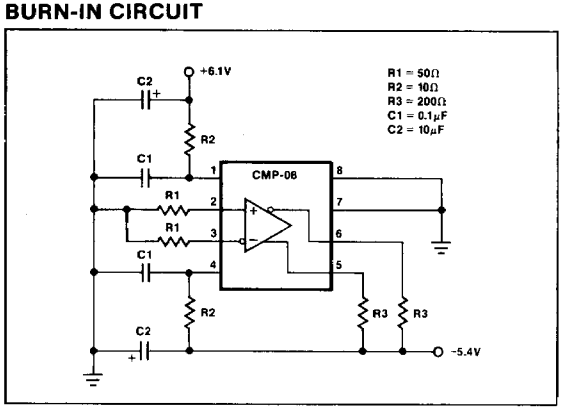
INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

POWER SUPPLIES

The CMP-08 uses a V+ positive supply, V− negative supply, and GND. Recommended operating limits for V+ are +4.75V to +6.3V. Recommended operating limits for V− are −4.7V to −5.7V.

The GND2 pin is the circuit ground for internal bias and logic level reference. The GND1 pin is output signal return ground for the output transistor collectors.

OUTPUT TERMINATION AND LOADING

The CMP-08 outputs are ECL-logic open-emitter transistors. Each output requires a pulldown resistor, which must be provided on the circuit board. Output logic level DC limits are specified for pulldown $R_L = 50\Omega$ to termination voltage $V_T = -2V$.

When the −2V termination voltage is available, the practical pulldown resistor range is 50Ω to 100Ω. If the user does not wish to provide a −2V supply, then pulldown may be to −5.2V with 200Ω to 300Ω resistors. Alternatively, each output may be loaded with 82Ω to GND and 130Ω to −5.2V, to generate the Thevenin equivalent of 50Ω to −2V.

The effect of various termination values on output logic levels may be estimated by assuming 7Ω as the output source resistance. There are AC effects as well. The CMP-08 is a high-gain broadband device, with stability dependent to some extent on output loading.

Optimum damping is achieved when both outputs are equally terminated with 50Ω to −2V or the Thevenin equivalent, with capacitive load below 10pF per output, and less than 5pF load mismatch. Avoid the use of only one output. Some loss of input resolution may occur when termination resistance exceeds 50Ω, or with greater capacitive loading.

INPUT RESOLUTION

All comparators have input resolution limited by gain and noise. Fast, broadband devices generally have less input resolution than traditional, slow comparators. The CMP-08 offers a good combination of input resolution and performance.

To obtain "hard" output logic voltage swing over the full operating temperature range, a mimimum input voltage increment of about 1.5mV is required. Smaller input increments can be resolved if the CMP-08 outputs are used differentially, or if the CMP-08 drives the data input to a latch or flip-flop.

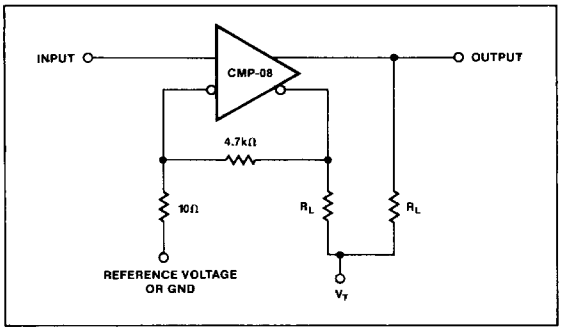
In the linear transfer region, the CMP-08 broadband noise is approximately 0.1mV RMS, or 0.5mV peak-to-peak. This provides a limit to the repeatability of any comparison decision.

ADDING HYSTERESIS

With its excellent stability, the CMP-08 will not require hysteresis in most applications. Hysteresis may be beneficial if the input voltage may come to rest within 2mV of threshold, or if the input slew rate is below 0.5V/ns through threshold. The use of hysteresis will provide sharp output transitions even when inputs are slow, and will reduce the likelihood of invalid output transitions due to noise.

Figure 1 shows hysteresis added to a CMP-08 circuit, with single-ended input and output signals. Pulldown resistors R_L to termination voltage V_T are required as usual. With the illustrated values of 4.7kΩ to output and 10Ω to ground, switching points at −1.1mV and −3.9mV are typically obtained. In most DC-coupled applications, the hysteresis trip points must be offset to other values. This may be accomplished by connecting the 10Ω resistor to a reference voltage other than ground, provided that the reference voltage is carefully decoupled. In small-signal applications, variations in switching points due to output voltage variations, resistance tolerance, and offset voltage must be taken into account. Note that the source resistance seen at the feedback node has been kept small, to avoid excessive phase shift due to RC time constants.

FIGURE 1: Optional Hysteresis Circuit



INPUT VOLTAGE RANGE

The CMP-08 positive common-mode input voltage range extends at least to 2.05V below the V+ supply. The negative common-mode range extends at least to 1.94V above the V− supply.

The application of either input signal above the positive common-mode range may cause undesirable operation. On the negative end, the CMP-08 will function properly if one or the other input is outside the common-mode range (but within the absolute maximum limits), provided that the other input is within the common-mode range.

In all cases, the maximum differential signal between +IN and −IN must be kept within the ±6V absolute maximum rating.

CIRCUIT BOARD DESIGN

The CMP-08 is a high-gain broadband device. The circuit board must use RF design practices for proper operation. Wire-wrap techniques are unlikely to be successful.

The V+ and V− supplies must be decoupled to ground using low inductance capacitors installed adjacent to the CMP-08 supply pins. The use of 0.1μF ceramic capacitors with closely trimmed leads (or leadless) is recommended.

The circuit board should include a solid ground plane, at least in the neighborhood of the CMP-08 and overlying its input and output signal traces. When a −2V termination supply is used, it should be decoupled to ground adjacent to the CMP-08 output pulldown resistors.

Best operation is obtained when the CMP-08 is soldered directly to the circuit board. Successful operation is also obtained with the use of low-profile machined-contact sockets, which are designed for high-speed applications.

ECL-TO-TTL TRANSLATION

The MC10125 or MC10H125 quad ECL-to-TTL translator devices may be used to convert the CMP-08 ECL outputs to a TTL-compatible signal.