

IS31FL3748

24 × 4 DOTS MATRIX LED DRIVER

March 2022

GENERAL DESCRIPTION

IS31FL3748 is a matrix LED driver with 24 high voltage (28V) constant current channels. It supports from one to four power scan to become a 24×n (n=1~4) matrix LED driver. Each channel can be pulse width modulated (PWM) with 7-bit/8-bit precision for smooth LED brightness control. In addition, each channel can be controlled by a 7-bit/8-bit output current control register (Dot correction, current scale, SL), which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is designed to be 40mA, which can be adjusted by three 7-bit/8-bit global control registers (one group for R for channels 3×I, one group for G for channels 3×I+1, and one group for B for channels 3×I+2, where I= 0 to 7). Proprietary algorithms are used in IS31FL3748 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via HSB (high speed series bus, up to 10MHz), DSB (Manchester encoded, daisy chained serial bus, up to 2MHz), SPI (12MHz) bus or I2C (1MHz) interface.

IS31FL3748 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature. It internally generates 4.8V V_{OUT} to power the internal logic operation, which can also be external powered from 3V to 5.5V.

IS31FL3748 is available in QFN-48 (6mm×6mm) package and can work over temperature range from -40°C to +125°C.

FEATURES

- Support 24 constant current channels
- 4 PMOS high side switches
- Tolerate up to 30V, nominal operation voltage between 4.5V to 28V
- Optional built-in LDO to generate 4.8V supply for internal logic
- Interface
 - DSB (Daisy Chained Serial Bus, 2MHz)
 - HSB (High Speed Series Bus: 10MHz)
 - SPI (12MHz)
 - I2C (1MHz) Interface
- SDB pin rising edge reset the interface
- For DSB and HSB
 - Built-in PWM generator: 7-bit/dot
 - Built-in Dot correction, current scale, SL: 7-bit/dot
 - 7-bit × 3 global current adjustment
- For SPI and I2C
 - Built-in PWM generator: 8-bit/dot
 - Built-in Dot correction, current scale, SL: 8-bit/dot
 - 8-bit × 3 global current adjustment
- Power noise reduction method
 - 4 groups delay to minimize the power ripple
 - Channel to channel timing skew (one sys-clock skew to reduce transient noise)
- Spread spectrum
- LED open detection and fault reporting (For I2C and SPI)
- Over temperature protection, over voltage protection, under voltage protection
- Operating temperature: -40°C to 125°C
- QFN-48 (6mm×6mm) package

APPLICATIONS

- White good display panel
- Pachinko
- Gaming machine

IS31FL3748

TYPICAL APPLICATION CIRCUIT

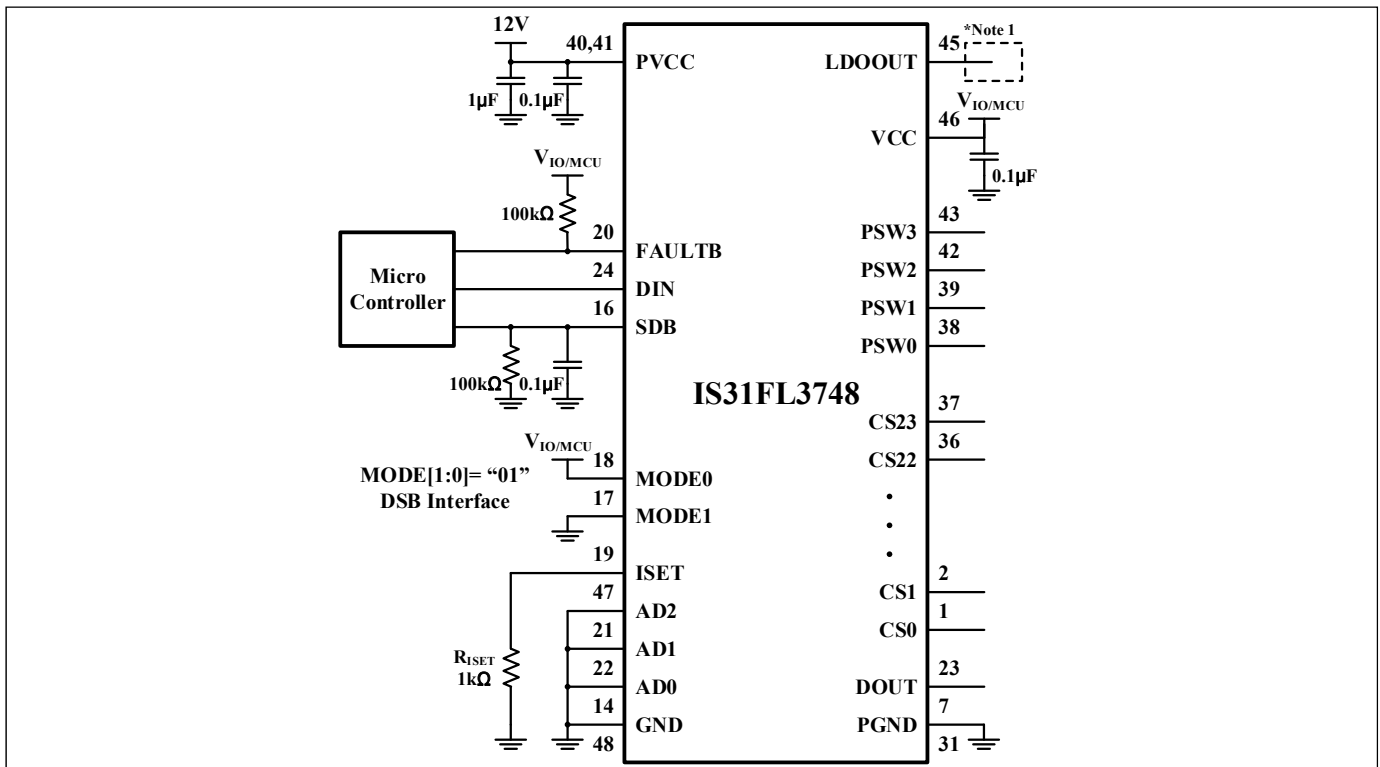


Figure 1 Typical Application Circuit (DSB Interface)

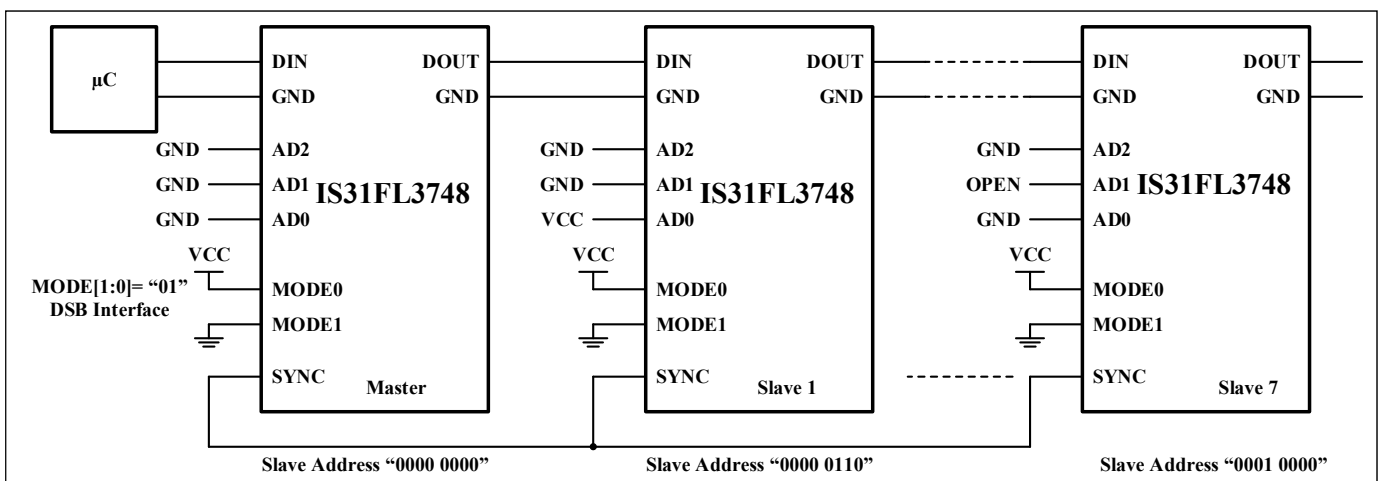


Figure 2 DSB Cascade Connection

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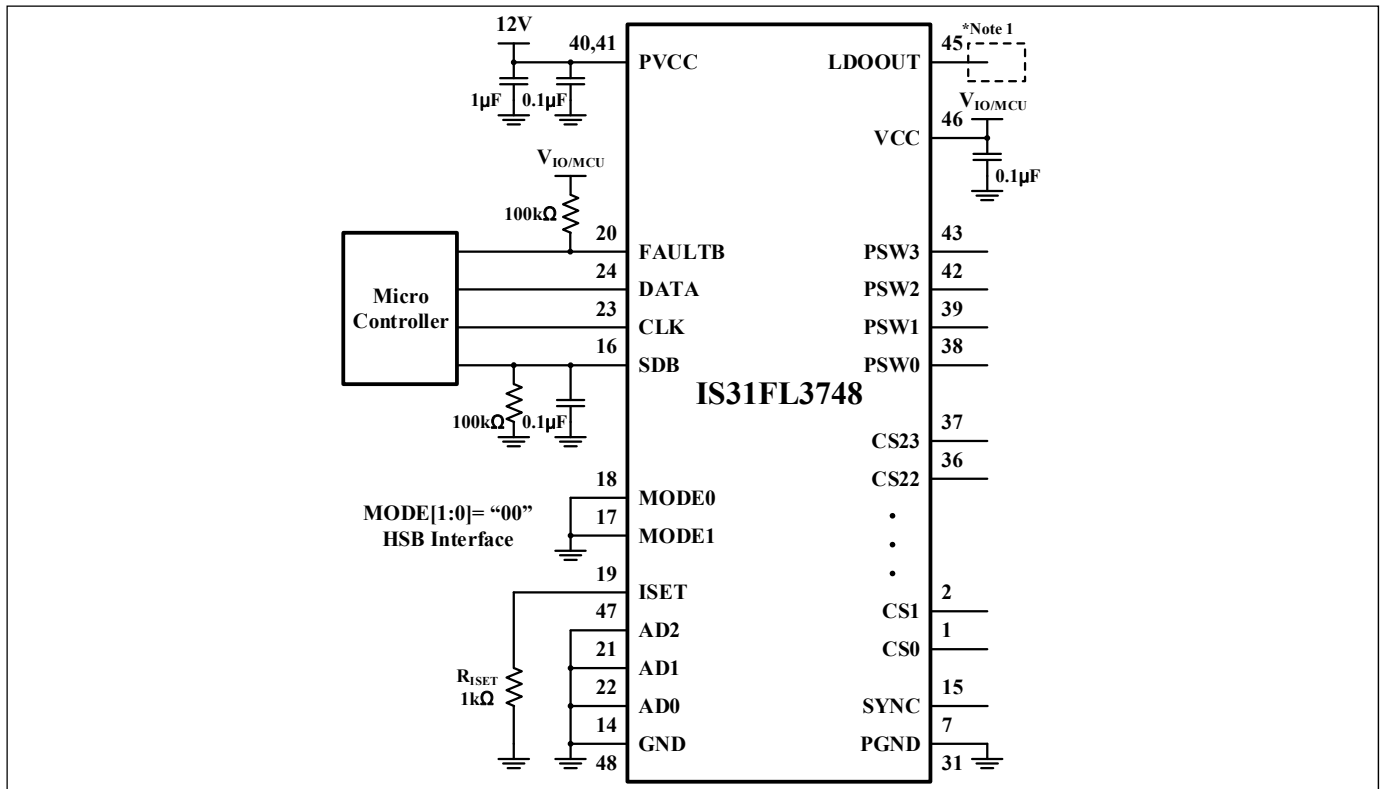


Figure 3 Typical Application Circuit (HSB Interface)

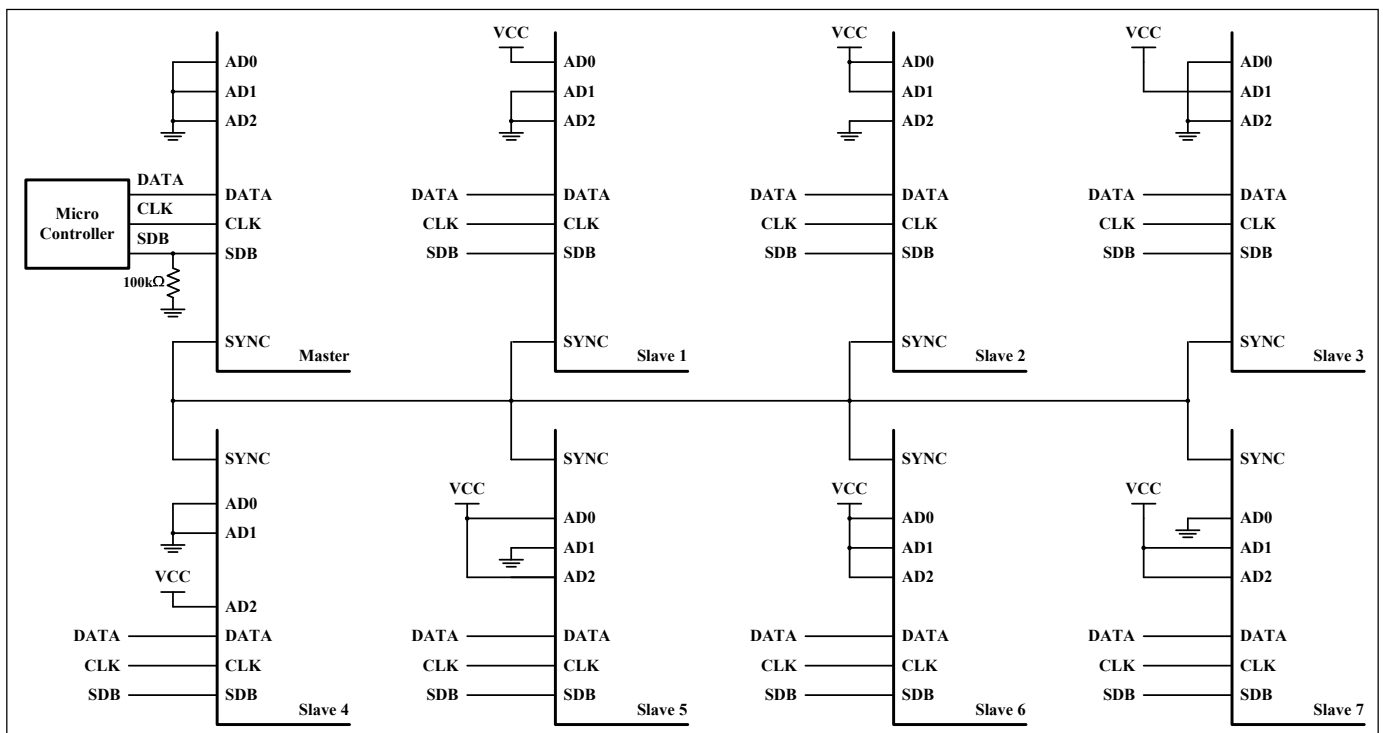


Figure 4 Typical Application Circuit: More Than One Slave in System (HSB Interface)

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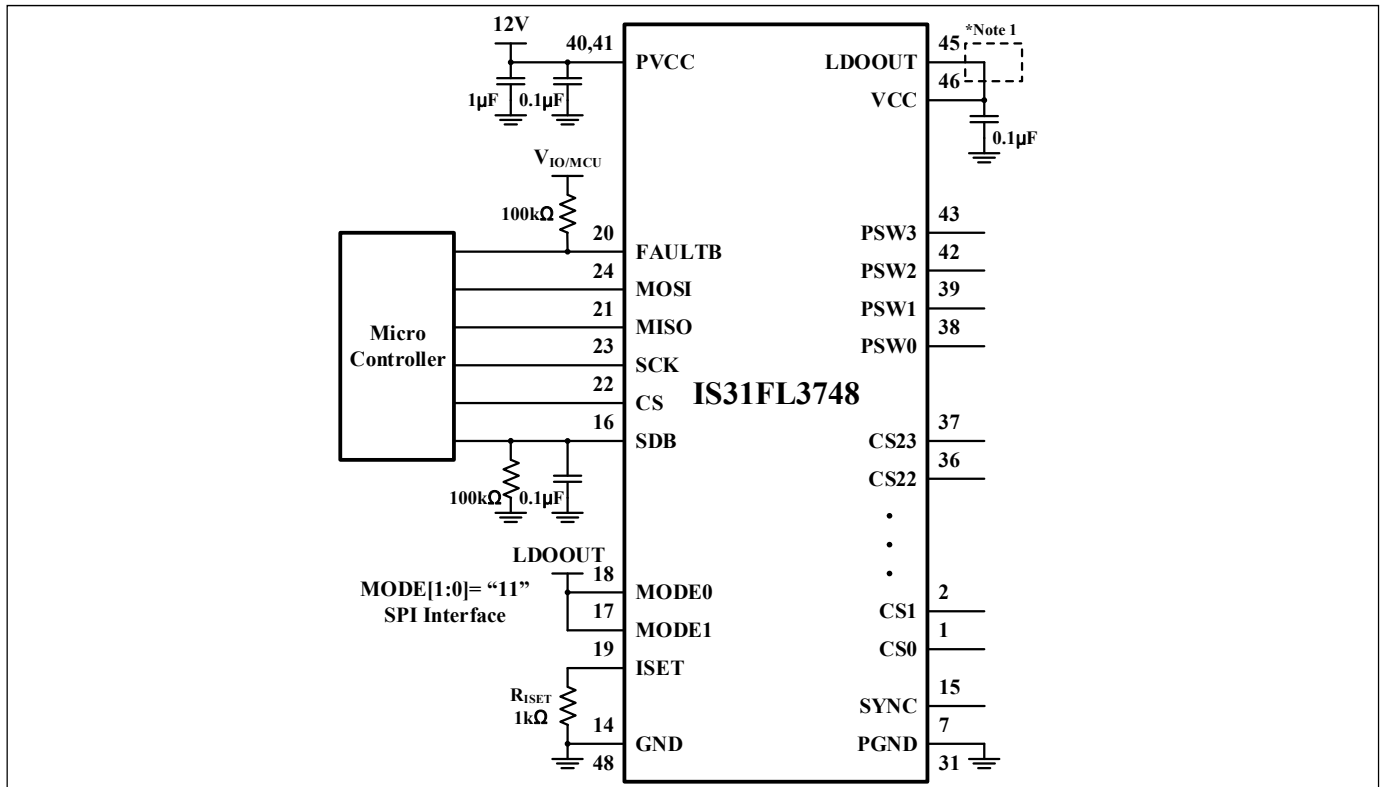


Figure 5 Typical Application Circuit (SPI Interface)

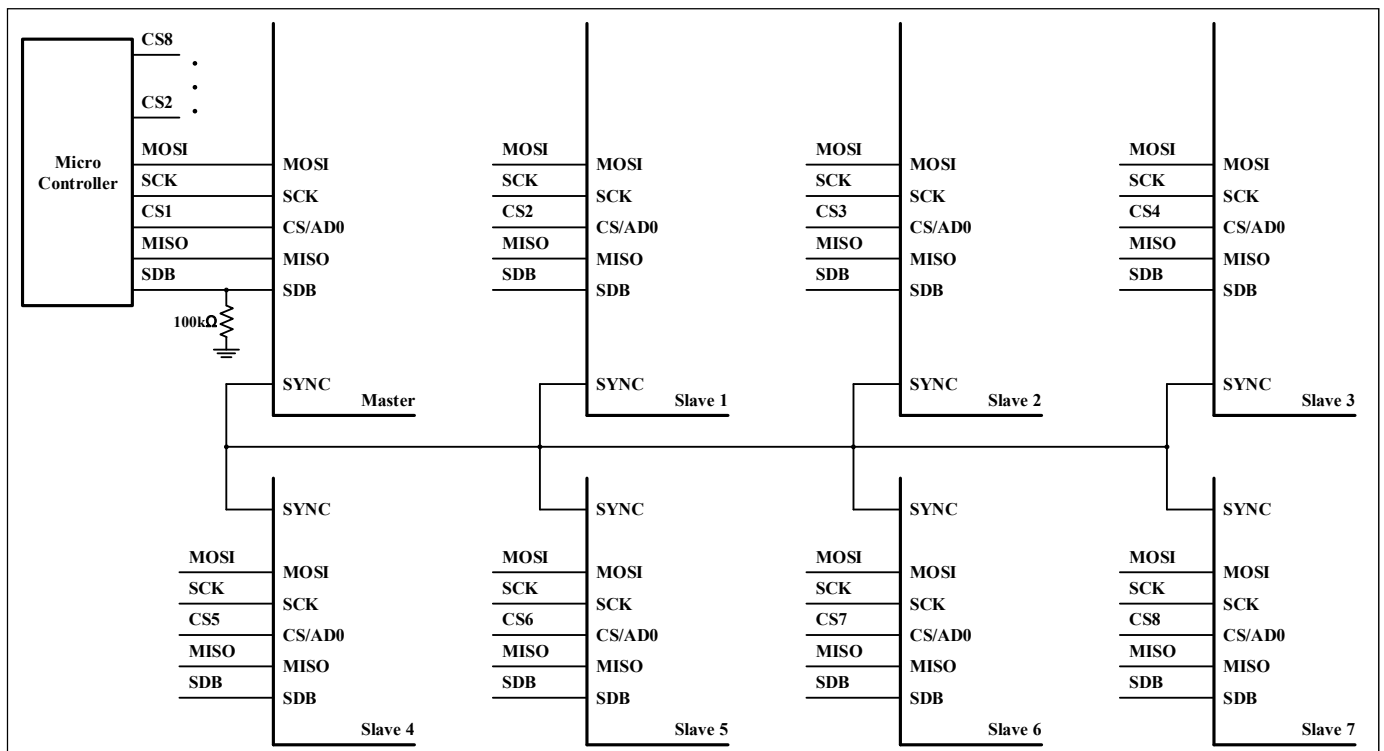


Figure 6 Typical Application Circuit: More Than One Slave in System (SPI Interface)

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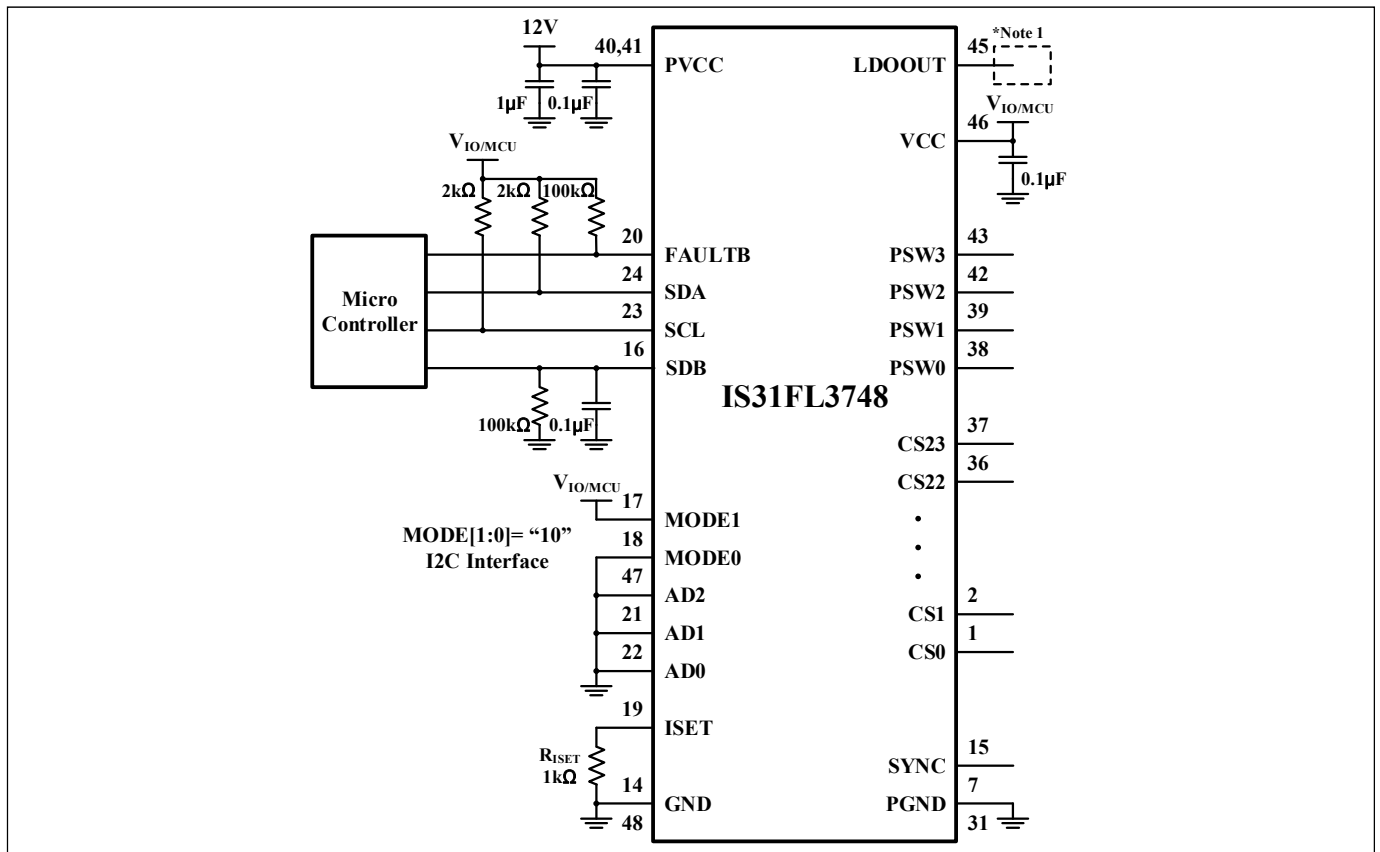


Figure 7 Typical Application Circuit (I2C Interface)

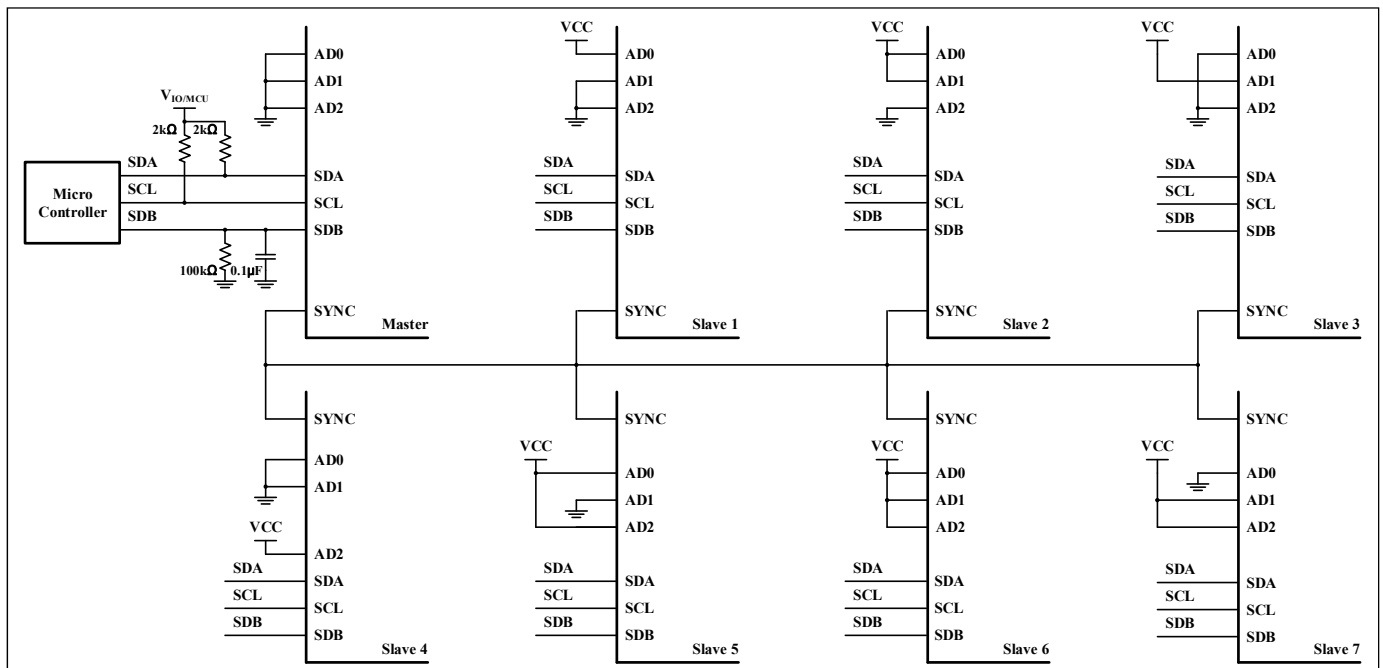


Figure 8 Typical Application Circuit: More Than One Slave in System (I2C Interface)

Note 1: LDOOUT can provide stable 4.8V power supply, which can directly supply power to VCC (LDO is short to VCC). When LDOOUT is not used, LDOOUT pin can be float/NC.

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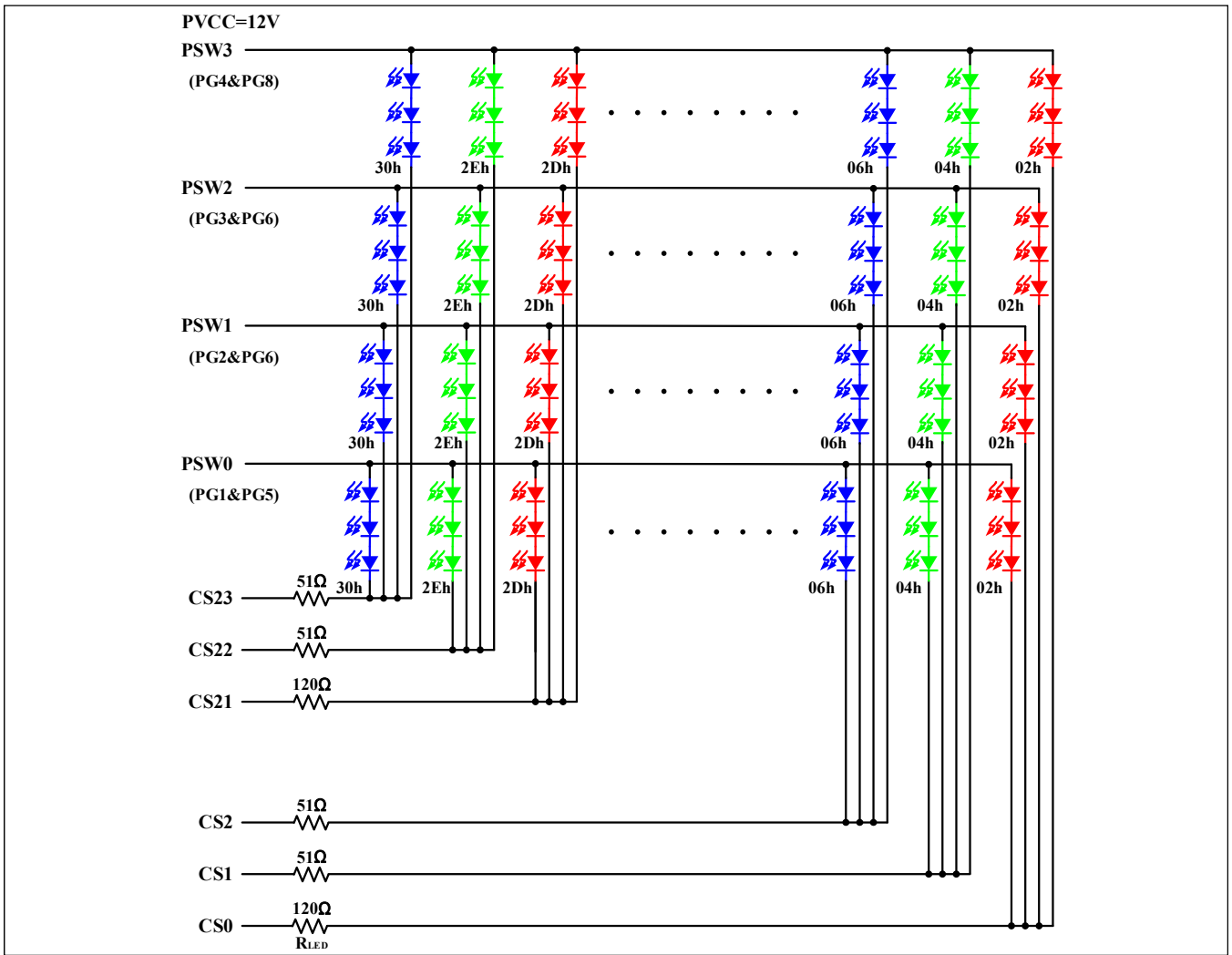


Figure 9 LED Circuit: 24x4

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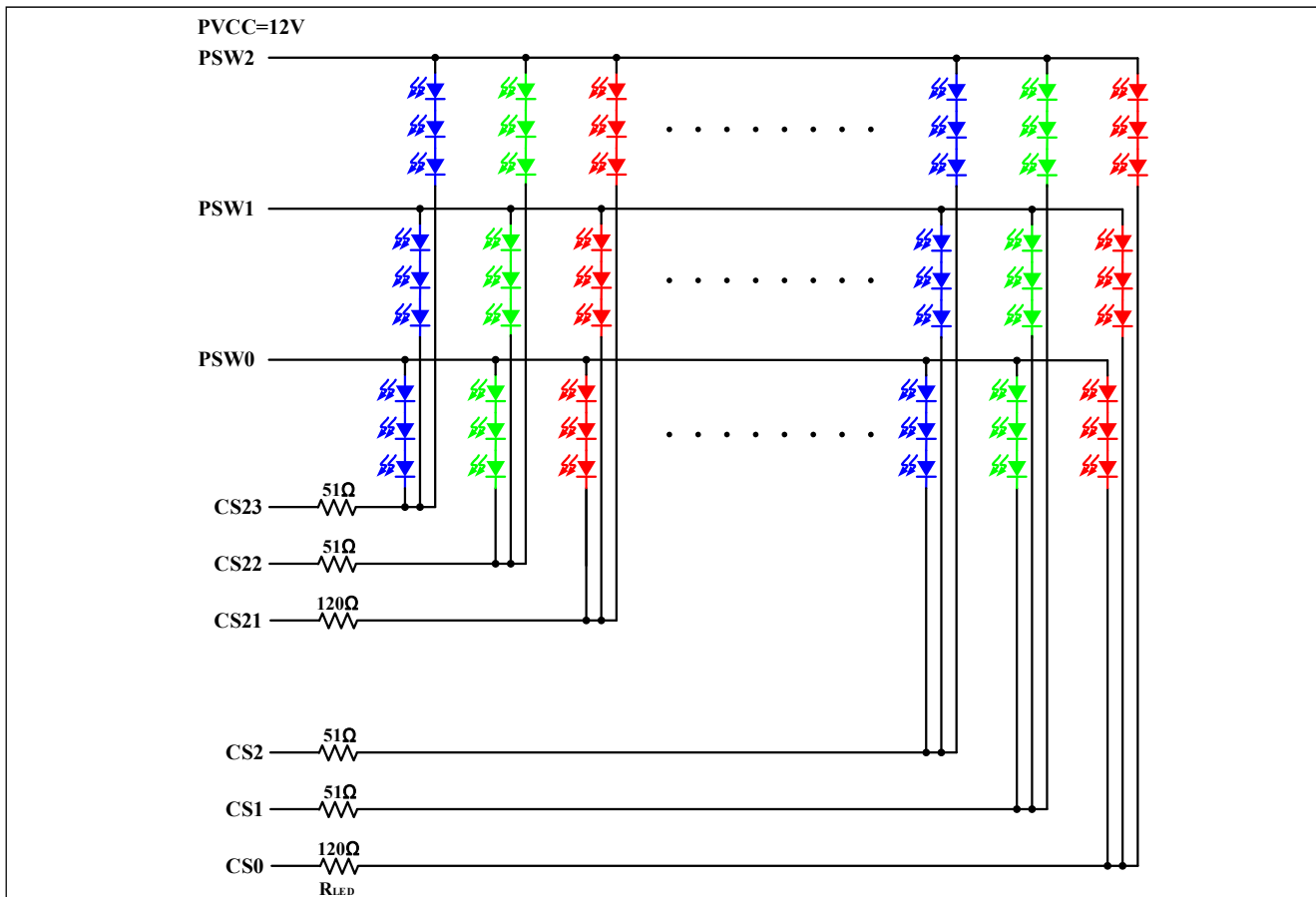


Figure 10 LED Circuit: 24x3

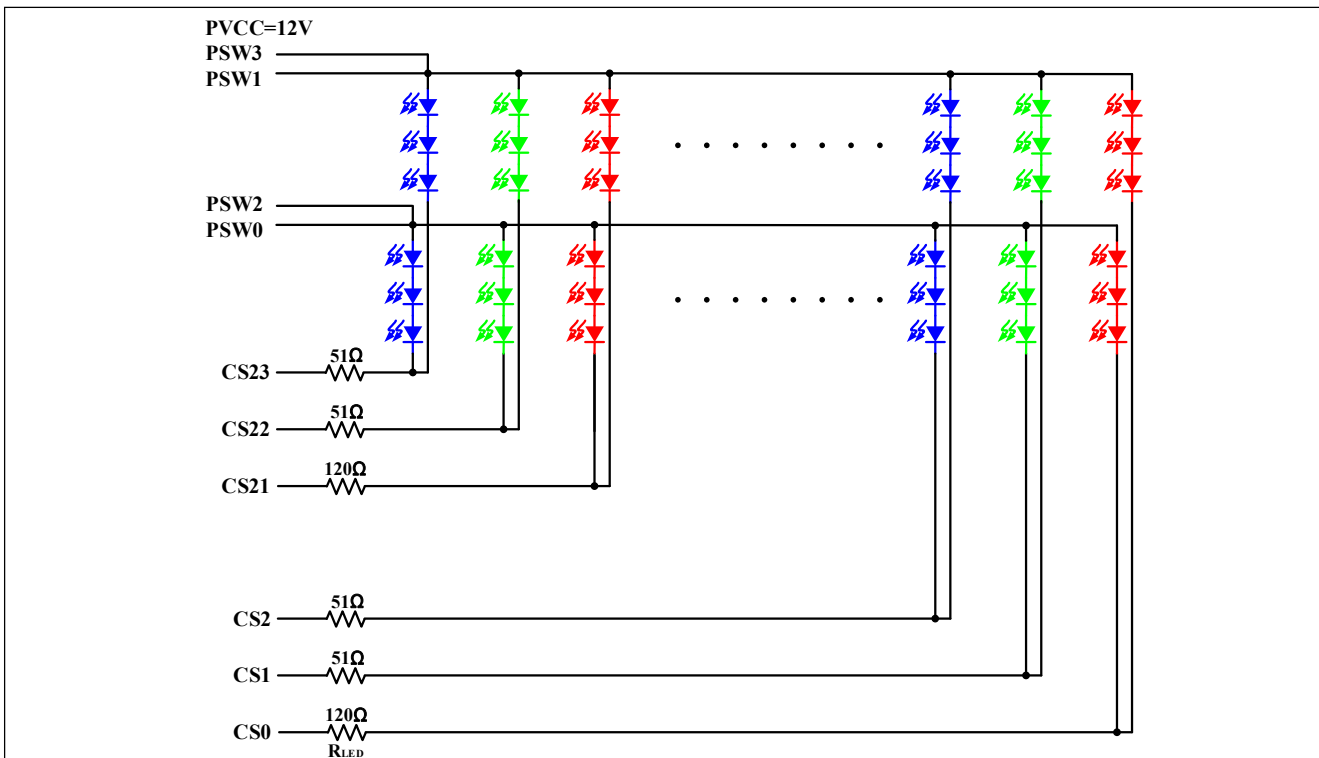


Figure 11 LED Circuit: 24x2

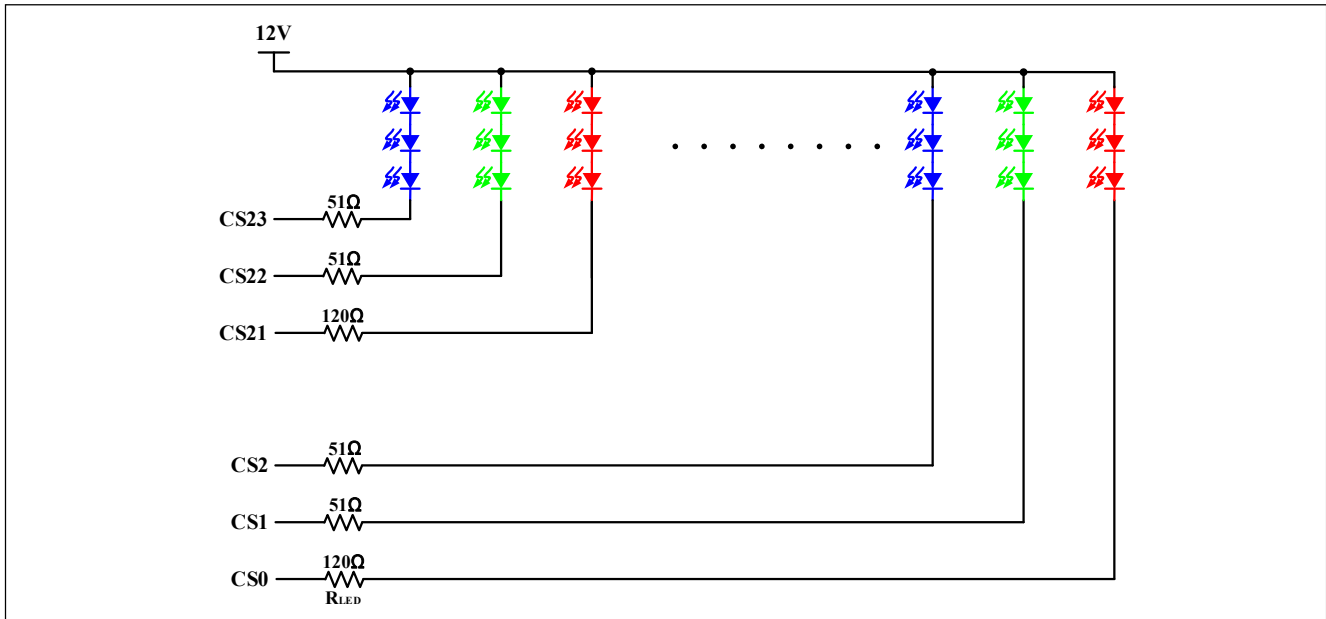
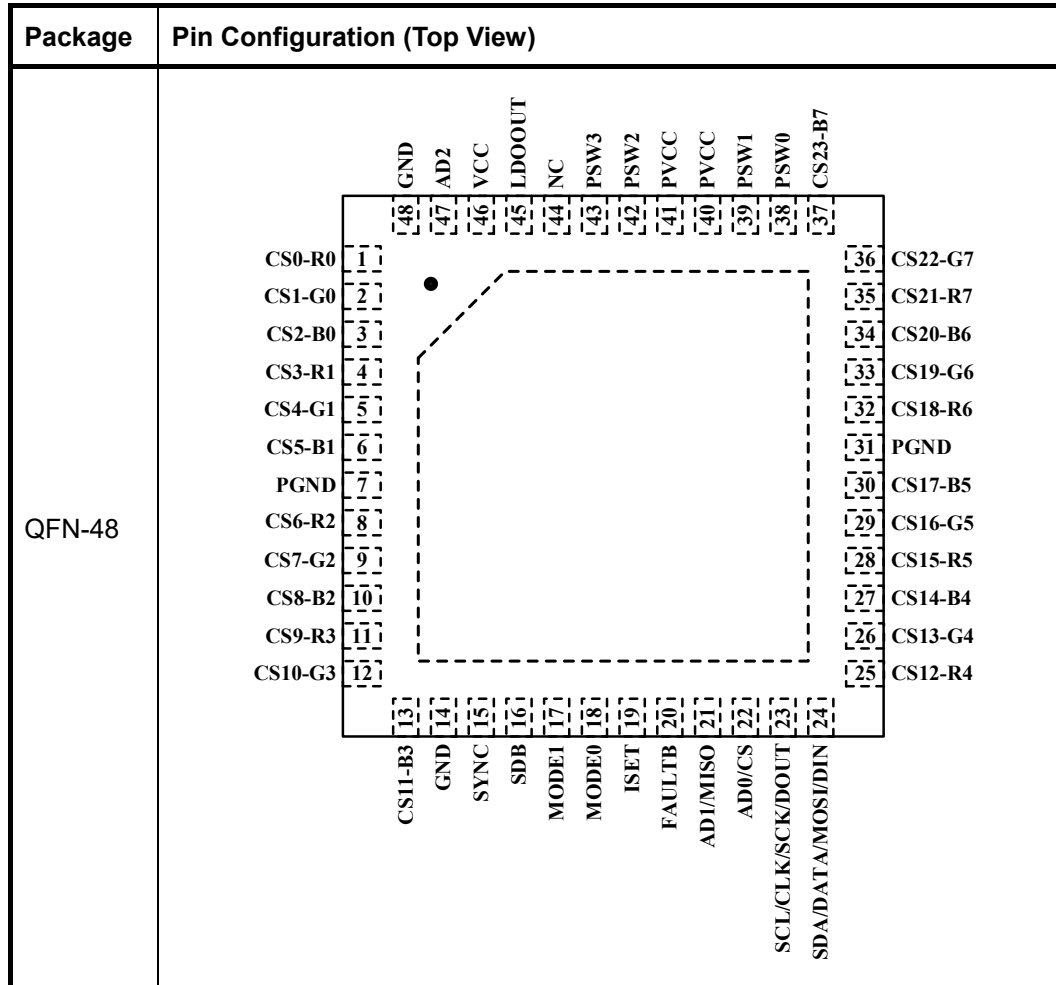


Figure 12 Typical LED Circuit: 24×1

Note 2: These resistors in series with LED are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3748 (values are for $PV_{CC}=12V$).

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PIN CONFIGURATION



IS31FL3748

PIN DESCRIPTION

| No. | Pin | Description |
|--------------------------|-----------------------|--|
| 1~6,8~13, 25~30,32~37 | CS[23:0]-Xx | X=R, G or B, x=0, 1, 2, current sink pin for LED matrix. |
| 7,31 | PGND | Power GND. |
| 14,48 | GND | Analog GND. |
| 15 | SYNC | Synchronization. |
| 16 | SDB | Shutdown pin. |
| 17,18 | MODE [1:0] | Interface selects. |
| 19 | ISET | Set the maximum IOOUT current. |
| 20 | FAULTB | Interrupt output pin. Register 78h can read the function of the FAULTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function is not used. |
| 21 | AD1/MISO | Address select pin/SPI output data. |
| 22 | AD0/CS | Address select pin/CS signal of SPI. |
| 23 | SCL/ CLK/SCK/DOUT | I2C clock/ HSB clock/ SPI clock /DSB Data out. |
| 24 | SDA/ DATA/MOSI/DIN | I2C input data /HSB input data / SPI input data/ DSB input data. |
| 38,39,42,43 | PSW[3:0] | Power SW. |
| 40, 41 | PVCC | Power for current source PSWx. |
| 44 | NC | Not connect. |
| 45 | LDOOUT | LDO output, 4.8V typical. |
| 46 | VCC | Analog and digital circuits. |
| 47 | AD2 | Address select pin. |
| | Thermal Pad | Connect to GND. |

IS31FL3748

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY/Reel |
|---------------------|-------------------|----------|
| IS31FL3748-QFLS4-TR | QFN-48, Lead-free | 2500 |

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

IS31FL3748

ABSOLUTE MAXIMUM RATINGS

| | |
|--|------------------------|
| Supply voltage, V_{CC} | -0.3V ~ +6.0V |
| Supply voltage, PV_{CC} | -0.3V ~ +30V |
| Voltage at CSx pin | -0.3V ~ +30V |
| Voltage at any input pin | -0.3V ~ $PV_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | +150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, $T_A=T_J$ | -40°C ~ +125°C |
| Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA} | 37.3°C/W |
| ESD (HBM) | ±7kV |
| ESD (CDM) | ±750V |

Note 3: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $PV_{CC}=12V$, $V_{CC}=5V$, $T_A=25^\circ C$, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|--|------|------|------|---------|
| PV_{CC} | Power supply voltage | | 4.5 | | 28 | V |
| V_{CC} | Supply voltage | | 3.0 | | 5.5 | V |
| $I_{CC}(PV_{CC})$ | Quiescent power supply current | $R_{ISET}=1.0k\Omega$, $V_{SDB}=V_{CC}=5V$, all LEDs off | | 2.2 | 3 | mA |
| $I_{CC}(V_{CC})$ | | $R_{ISET}=1.0k\Omega$, $V_{SDB}=V_{CC}=5V$, all LEDs off | | 11.6 | 15 | mA |
| $I_{SD}(PV_{CC})$ | Shutdown current | $V_{SDB}=0V$ | | 10 | 12 | μA |
| $I_{SD}(V_{CC})$ | | | | 2.6 | 3.5 | |
| $I_{SD}(PV_{CC})$ | | $V_{SDB}=V_{CC}=5V$, Configuration Register written “0000 0000” | | 1.0 | 1.5 | mA |
| $I_{SD}(V_{CC})$ | | | | 7.2 | 10 | |
| I_{OUT} | Maximum constant current of CSx | $R_{ISET}=1k\Omega$, $GCCR=GCCG=GCCB=0xFE$ | 37 | 39.6 | 43 | mA |
| ΔI_{MAT} | Output current error between outputs (Note 4) | $R_{ISET}=1k\Omega$, $GCCR=GCCG=GCCB=0xFE$ | -5 | | 5 | % |
| ΔI_{ACC} | Output current error between devices (Note 5) | $R_{ISET}=1k\Omega$, $GCCR=GCCG=GCCB=0xFE$ | -8 | | 8 | % |
| V_{HR} | Current switch headroom voltage PSWx | $R_{ISET}=1k\Omega$, $I_{SWITCH}=800mA$ | | 700 | 1100 | mV |
| | Current sink headroom voltage CSx | $R_{ISET}=1k\Omega$, $I_{SINK}=40mA$ | | 350 | 550 | |
| t_{SCAN} | Turn on time of single PSWy | PWMF=32kHz | 27 | 31 | 35 | μs |
| t_{NOL1} | Non-overlap blanking time during scan, the PSWx and CSy are all off during this time | PWMF=32kHz | | 0.75 | | μs |
| t_{NOL2} | Delay total time for CS0 to CS23, during this time, the PSWx is on but CSx is not all turned on | PWMF=32kHz (Note 6) | | 0.37 | | μs |

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ELECTRICAL CHARACTERISTICS (CONTINUED)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--|-------------------------|---------------|------|--------------|------|
| Logic Electrical Characteristics (DATA/DIN/MOSI, CLK/DOUT/MISO, CS, MODE[1:0], AD[2:0]) | | | | | | |
| V_{IL} | Logic "0" input voltage (not include SDB pin) | $V_{CC}= 3.0V$ | | | $0.3V_{CC}$ | V |
| V_{IH} | Logic "1" input voltage (not include SDB pin) | $V_{CC}= 5.5V$ | $0.7V_{CC}$ | | | V |
| V_{HYS} | Input Schmitt trigger hysteresis (not include SDB pin) | $V_{CC}= 3.6V$ | | 0.2 | | V |
| V_{AD} | Input for AD[2:0], AD= VCC | $V_{CC}= 3.0V\sim 5.5V$ | $V_{CC}-0.3$ | | V_{CC} | V |
| | Input for AD[2:0], AD= Open | $V_{CC}= 3.0V\sim 5.5V$ | $GND+1.6$ | | $V_{CC}-0.6$ | V |
| | Input for AD[2:0], AD= ISET | $V_{CC}= 3.0V\sim 5.5V$ | $ISET-0.3$ | | $ISET+0.3$ | V |
| | Input for AD[2:0], AD= GND | $V_{CC}= 3.0V\sim 5.5V$ | GND | | $GND+0.3$ | V |
| V_{OH} | H level MISO pin output voltage | $I_{OH}= -8mA$ | $V_{CC}-0.4V$ | | V_{CC} | V |
| V_{OL} | L level MISO pin output voltage | $I_{OL}= 8mA$ | 0 | | 0.4 | V |
| V_{IL_SDB} | Logic "0" input voltage | $V_{CC}= 3.0V$ | | | 0.6 | V |
| V_{IH_SDB} | Logic "1" input voltage | $V_{CC}= 5.5V$ | 2 | | | V |
| V_{HYS_SDB} | Input schmitt trigger hysteresis | $V_{CC}= 3.6V$ | | 0.2 | | V |
| I_{IL} | Logic "0" input current | $V_{INPUT}= L$ (Note 6) | | 5 | | nA |
| I_{IH} | Logic "1" input current | $V_{INPUT}= H$ (Note 6) | | 5 | | nA |

DIGITAL INPUT HSB SWITCHING CHARACTERISTICS (NOTE 6)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|------------|---------------------|------|------|------|-------|
| f_C | Clock frequency | - | | 10 | MHz |
| t_{DVCH} | Data in set-up time | 10 | | - | ns |
| t_{CHDX} | Data in hold time | 10 | | - | ns |
| t_{CH} | Clock high time | 50 | | - | ns |
| t_{CL} | Clock low time | 50 | | - | ns |

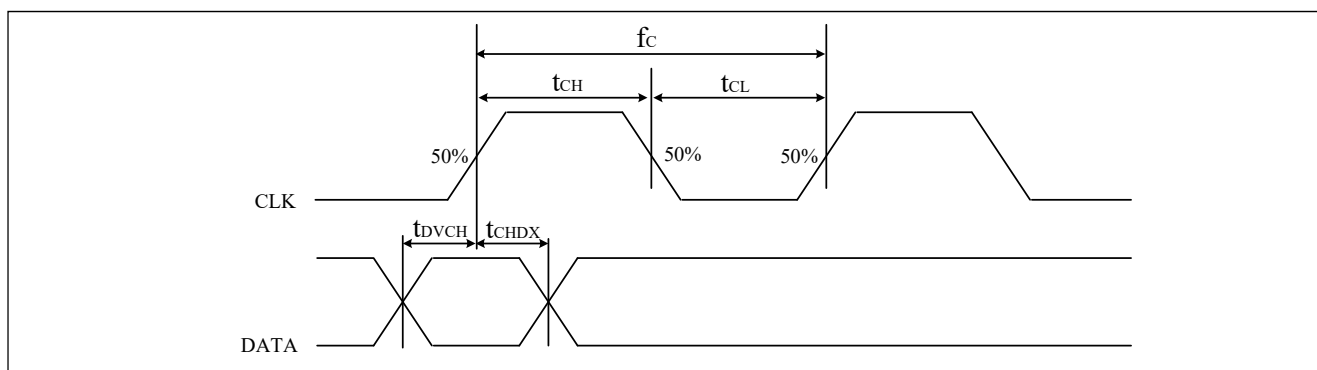


Figure 13 HSB Input Timing

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DIGITAL INPUT DSB SWITCHING CHARACTERISTICS (NOTE 6)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------|---|------|------|------|-------|
| t_{pLH} | DATAIN-DATAOUT propagation delay time $C_L=15pF, t_r = t_f=15ns$ | - | | 20 | ns |
| t_{pHL} | DATAIN-DATAOUT propagation delay time $C_L=15pF, t_r = t_f=15ns$ | - | | 20 | ns |

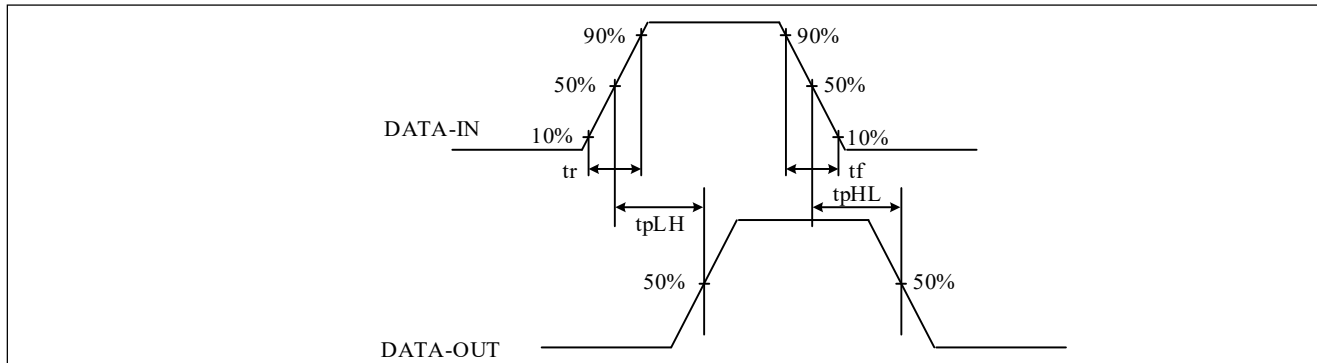


Figure 14 t_{pHL}/t_{pLH} for DSB

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 6)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|------------|---------------------------|------|------|------|-------|
| f_C | Clock frequency | - | | 12 | MHz |
| t_{SLCH} | CS active set-up time | 34 | | | ns |
| t_{SHCH} | CS not active set-up time | 17 | | | ns |
| t_{SHSL} | CS detect time | 167 | | | ns |
| t_{CHSH} | CS active hold time | 34 | | | ns |
| t_{CHSL} | CS not active hold time | 17 | | | ns |
| t_{CH} | Clock high time | 34 | | | ns |
| t_{CL} | Clock low time | 34 | | | ns |
| t_{CLCH} | Clock rise time | | | 9 | ns |
| t_{CHCL} | Clock fall time | | | 9 | ns |
| t_{DVCH} | Data in set-up time | 7 | | | ns |
| t_{CHDX} | Data in hold time | 9 | | | ns |
| t_{SHQZ} | Output disable time | | | 34 | ns |
| t_{CLQV} | Clock low to output valid | | | 39 | ns |
| t_{CLQX} | Output hold time | 0 | | | ns |
| t_{QLQH} | Output rise time | | | 17 | ns |
| t_{QLQH} | Output fall time | | | 17 | ns |

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DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 6)

| Symbol | Parameter | Fast Mode | | | Fast Mode Plus | | | Units |
|----------------------|--|-----------|------|------|----------------|------|------|-------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| f _{SCL} | Serial-clock frequency | - | | 400 | - | | 1000 | kHz |
| t _{BUF} | Bus free time between a STOP and a START condition | 1.3 | | - | 0.5 | | - | µs |
| t _{HD, STA} | Hold time (repeated) START condition | 0.6 | | - | 0.26 | | - | µs |
| t _{SU, STA} | Repeated START condition setup time | 0.6 | | - | 0.26 | | - | µs |
| t _{SU, STO} | STOP condition setup time | 0.6 | | - | 0.26 | | - | µs |
| t _{HD, DAT} | Data hold time | - | | - | - | | - | µs |
| t _{SU, DAT} | Data setup time | 100 | | - | 50 | | - | ns |
| t _{LOW} | SCL clock low period | 1.3 | | - | 0.5 | | - | µs |
| t _{HIGH} | SCL clock high period | 0.7 | | - | 0.26 | | - | µs |
| t _R | Rise time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |
| t _F | Fall time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |

Note 4: I_{OUT} mismatch (bit to bit) ΔI_{MAT} is calculated:

$$\Delta I_{MAT} = \pm \left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0} + I_{OUT1} + \dots + I_{OUT23}}{24} \times 2 \right)} \right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) ΔI_{ACC} is calculated:

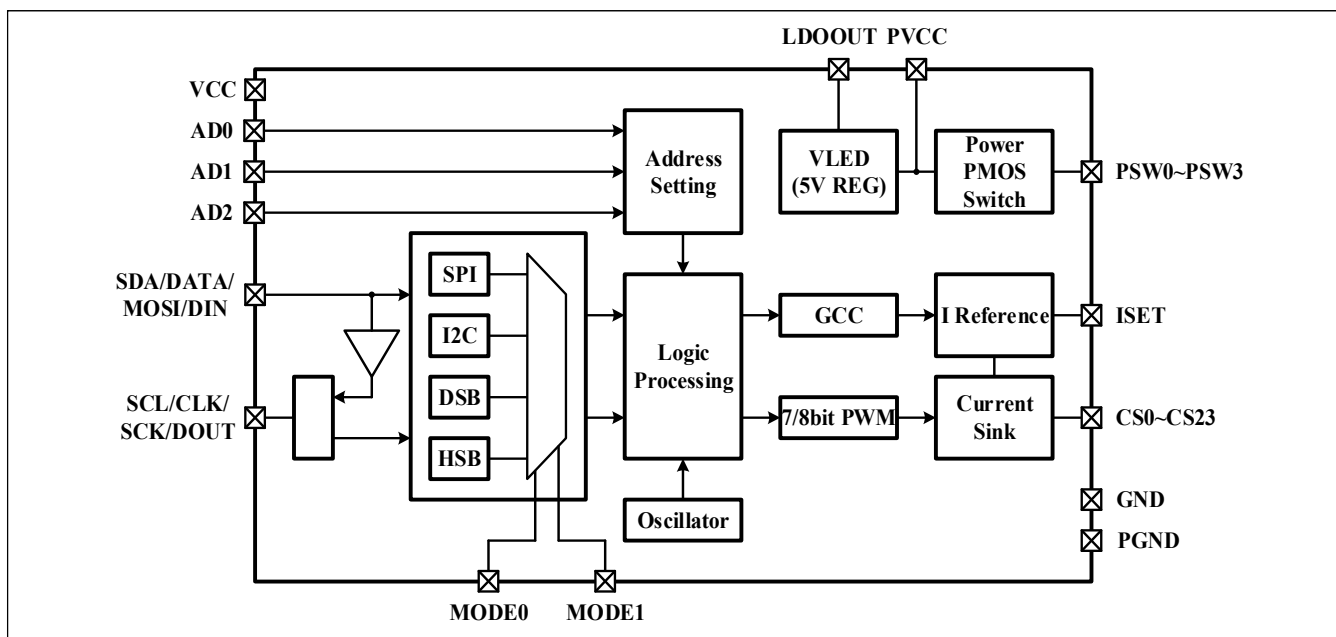
$$\Delta I_{ACC} = \pm \text{MAX} \left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where I_{OUT(IDEAL)} = 39.6mA when R_{ISSET} = 1kΩ.

Note 6: Guaranteed by design.

IS31FL3748

FUNCTIONAL BLOCK DIAGRAM



IS31FL3748

DETAILED DESCRIPTION

IS31FL3748 has two MODE pins which can select the interface of IS31FL3748.

Table 1 Interface Setting

| MODE[1:0] | Interface |
|-----------|-----------------------------|
| 00 | HSB, high speed serial bus |
| 01 | DSB, daisy chain serial bus |
| 10 | I2C |
| 11 | SPI |

HSB INTERFACE (HIGH SPEED SERIAL BUS)

When MODEx pins are connected as MODE[1:0]= "00", the device will be programmed in HSB, high speed serial bus, the IS31FL3748 should be programmed using the following format:

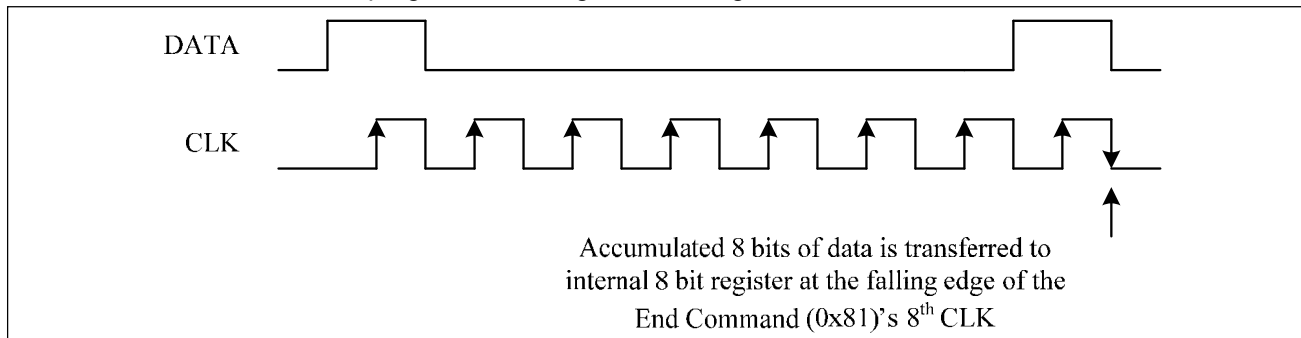


Figure 15 Data State To The Transition State

About data setting of the registers please refer to DATA SETTING MODE section.

DSB INTERFACE (DAISY CHAIN SERIAL BUS)

When MODEx pins are connected as MODE[1:0]= "01", the device will be programmed in DSB, daisy chain serial bus.

The IS31FL3748 uses DIN signal. As compared with 2 wires data signal synchronous with the clock signal in conventional products, this product assigns each data state to the transition state (H to L or L to H) as shown below.

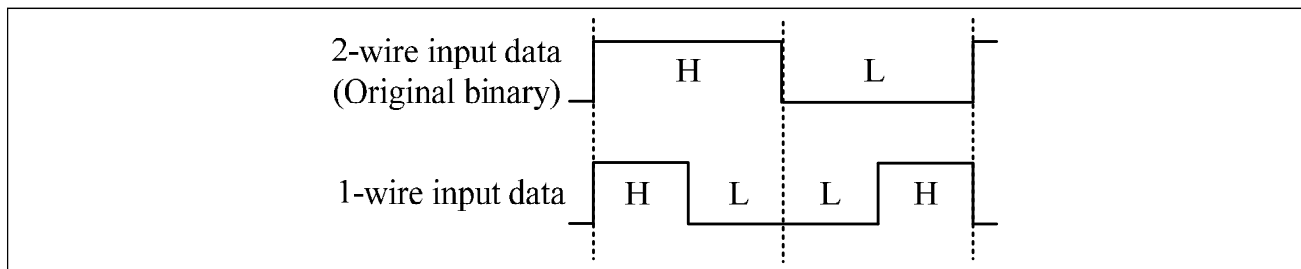


Figure 16 Data state to the transition state

About data setting of the registers please refer to DATA SETTING MODE section.

DATA SETTING MODE (For HSB AND DSB)

For setting data, select from (1) Normal Programming Mode, (2) Special Programming Mode, if all outputs are controlled, Special Programming Mode is recommended.

(1) Normal Programming Mode

| | | | | |
|-----------------------------|-------------------------|----------------------------|---------------------|---------------------------|
| Start Command [11111111] | Slave Address 8 bits | Register Address 8 bits | Data byte 8 bits | End Command [10000001] |
|-----------------------------|-------------------------|----------------------------|---------------------|---------------------------|

Figure 17 Programming One Register

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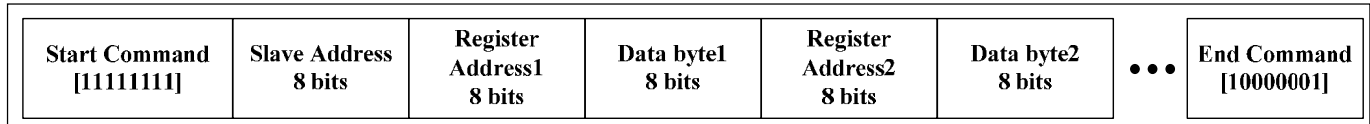


Figure 18 Programming More Than One Register

Normal Programming Mode should be set as the following flow:

“Start Command (11111111)”->“Slave address(8 bits)” -> “Register(8 bits)” -> “Data byte(8 bits)” -> “End Command (10000001)” or

“Start Command (11111111)”->“Slave address(8 bits)” -> “Register 1 (8 bits)” -> “Data byte1 (8 bits)” -> “Register 2 (8 bits)” -> “Data byte2 (8 bits)” -> ...-> “End Command (10000001)”

Input data from DATA signal is written to the shift register at the rising edge of CLK every 8 bit.

This data is transferred at the falling edge of the End Command (0x81)’s eighth CLK.

(2) Special Programming Mode

When data of 01100000 is input to the sub address, the operation moves to the special mode where all channels are selected in order. Data of 24 channels should be input.

(If data of more than 24 channels are provided, the 25th and subsequent data are treated as invalid. If data of less than 24 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.)

To return to the normal mode, input data from the start command (ALL “H” 8-bit). In case of using this mode configuration, volume of data can be omitted.

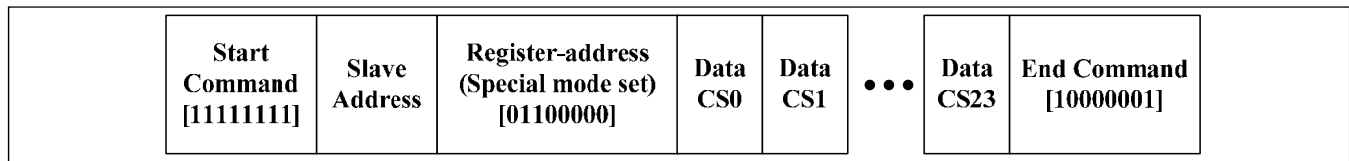


Figure 19 Programming in Special Programming Mode

SLAVE ADDRESSES (For HSB and DSB)

Input voltages and logic states of the AD2, AD1 and AD0 pins are determined as follows.

(High order bit = 0. Low order bit = 0 (Except of all selection))

VCC= “11”, ISET= “01”, Open= “10”, GND= “00”

Table 2 Slave Address (For HSB and DSB)

| A7 | A6:A5 | A4:A3 | A2:A1 | A0 | Remark |
|----|-------|-------|-------|----|---|
| 0 | AD2 | AD1 | AD0 | 0 | ADx=VCC, ISET, Open or GND, “00000000” ~ “01111110” |
| 0 | xx | xx | xx | 1 | All Select, 4 PWM pages will be included. |

Total support “00000000” ~ “01111110”, 64 addresses

When A7:A0= “0xxx xxx1” all slave device are selected, include 4 PWM pages in each single part.

The All Select slave address allows every device and even every 4 PWM pages to be addressed at the same time. This special slave address is to facilitate a system broadcast mode.

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SPI INTERFACE

When MODEx pins are connected as MODE[1:0]= “11”, the device will be programmed SPI bus.

IS31FL3748 uses a SPI protocol to control the chip’s function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3748 latches data when clock rising.

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first, and is followed by register address byte then the register data. If the R/W bit is “0”, it will be written operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS31FL3748 is 12MHz.

Table 3 SPI Command Byte

| Name | R/W | ID bit | Page No. |
|-------|---------------------|--------|---|
| Bit | D7 | D6:D4 | D3:D0 |
| Value | 0: Write 1: Read | 101 | 0110: Point to Page 1 1000: Point to Page 2 1010: Point to Page 3 1100: Point to Page 4 |
| | | 110 | 0110: Point to Page 5 1000: Point to Page 6 1010: Point to Page 7 1100: Point to Page 8 1110: Point to Page 9 |

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3748, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3748 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3748 (Figure 23).

READING OPERATION

Page1~Page 9 registers can be read by SPI.

To read the registers of Page 1 thru Page 9, The D7 of the Command Byte need to be set to “1” and select the page number. If read one register, as shown in Figure 24, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 25, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

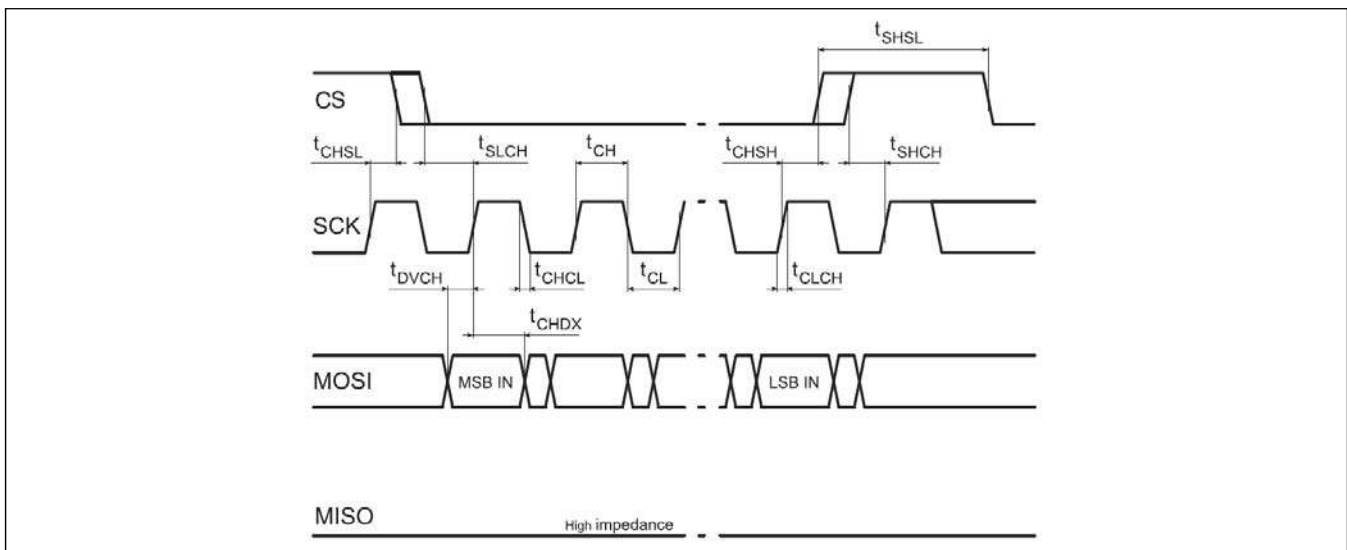


Figure 20 SPI Input Timing

IS31FL3748

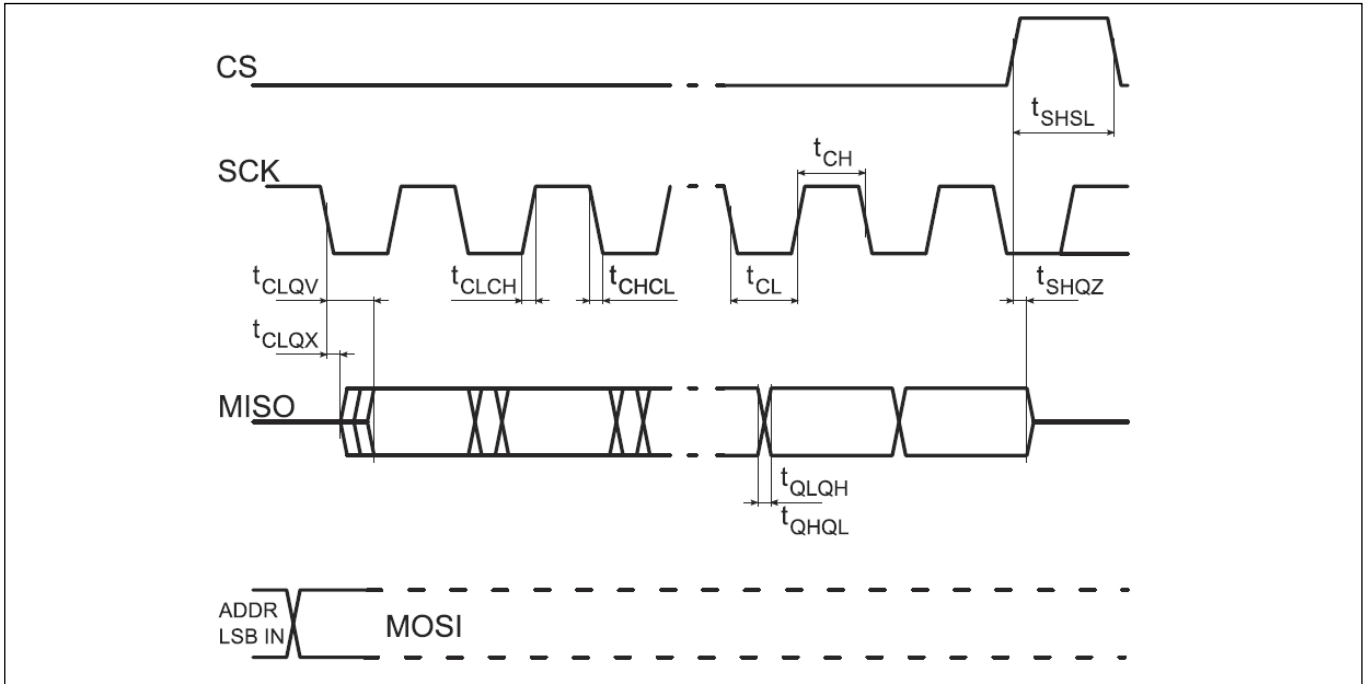


Figure 21 SPI Input Timing

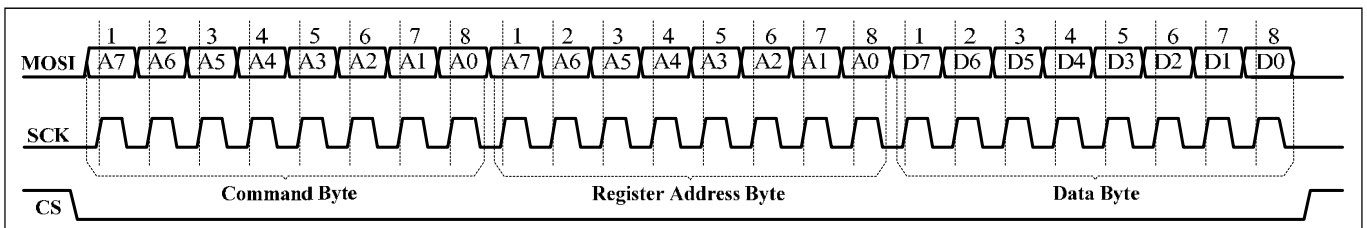


Figure 22 SPI writing to IS31FL3748 (Typical)

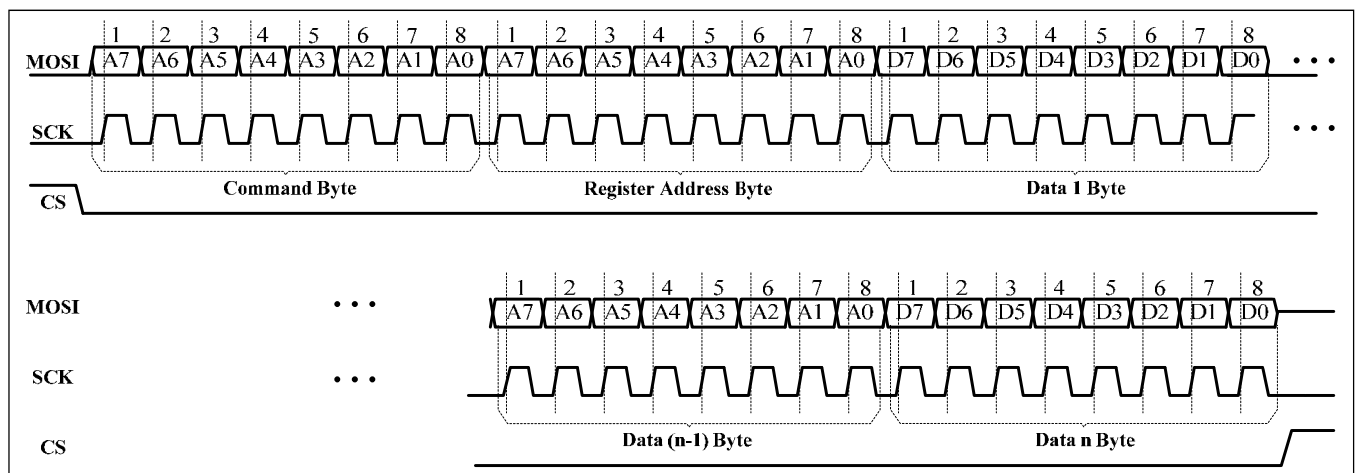


Figure 23 SPI Writing to IS31FL3748 (Automatic Address Increment)

IS31FL3748

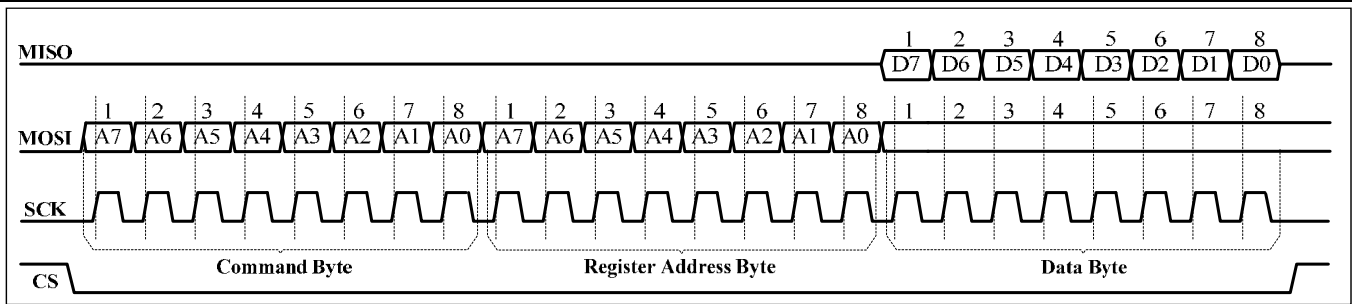


Figure 24 SPI Reading From IS31FL3748 (Typical)

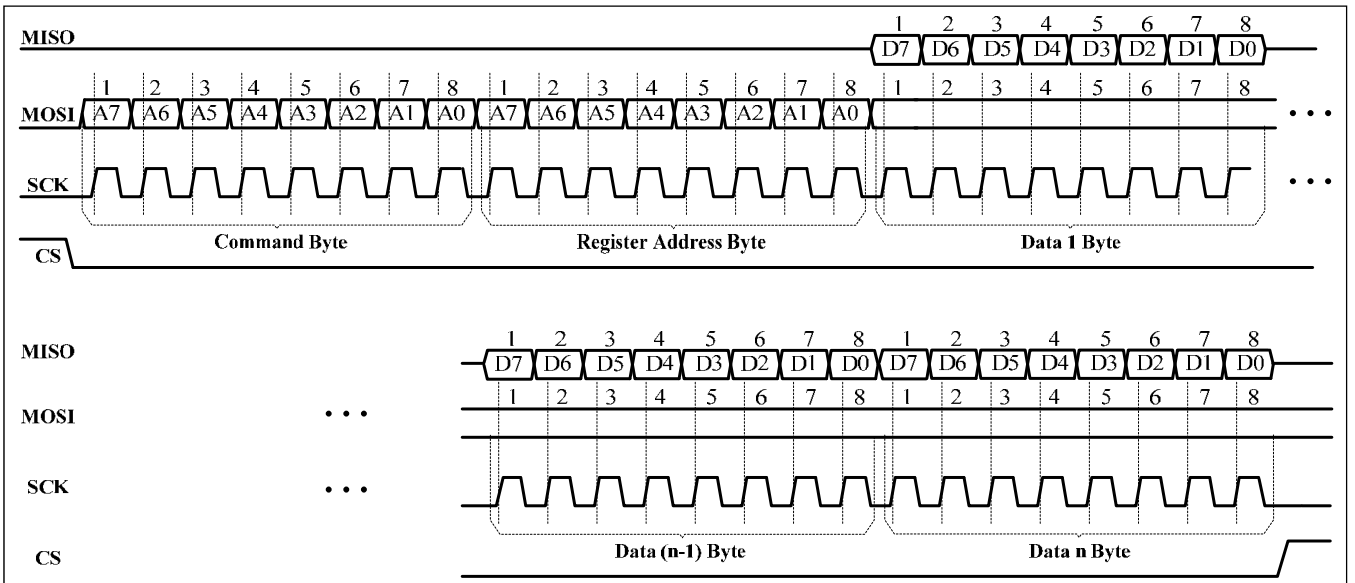


Figure 25 SPI Reading From IS31FL3748 (Automatic Address Increment)

I2C INTERFACE

When MODEx pins are connected as MODE[1:0]= “10”, the device will be programmed I2C bus.

IS31FL3748 uses a serial bus, which conforms to the I2C protocol, to control the chip’s functions with two wires: SCL and SDA. The IS31FL3748 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to “0” for a write command and set A0 to “1” for a read command. The value of bits from A6 to A1 is decided by the connection of the ADx pins.

Input voltages and logic states of the AD2, AD1 and AD0 pins are determined as follows.

Table 4 Slave Address

| A7 | A6:A5 | A4:A3 | A2:A1 | A0 | Remark |
|----|-------|-------|-------|----|---|
| 1 | AD2 | AD1 | AD0 | 0 | ADx=VCC, ISET, Open or GND, “10000000” ~ “11111100” AD[2:0] must not all connect to VCC |
| 1 | AD2 | AD1 | AD0 | 1 | Read address |
| 1 | 1 | 1 | 1 | 0 | Broadcast address, all slaves will ack |

ADx connected to VCC, ADx = 11;

ADx connected to ISET, ADx = 01;

ADx is open, ADx = 10;

ADx connected to GND, ADx = 00;

Total support “10000000”~“11111100”, 63 addresses.

When A7:A0= “1111 1110” all slave devices are

selected, include 4 PWM pages in each single part.

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3748.

IS31FL3748

The timing diagram for the I2C is shown in Figure 26. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The “START” signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3748’s acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3748 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a “STOP” signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3748, the register address byte is sent, most significant bit first. IS31FL3748 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3748 must generate another acknowledge to indicate that the data was received.

The “STOP” signal ends the transfer. To signal “STOP”, the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3748, load the address of the data register that the first data byte is intended for. During the IS31FL3748 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3748 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3748 (Figure 29).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3748 device address with the R/\bar{W} bit set to “0”, followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3748 device address with the R/\bar{W} bit set to “1”. Data from the register defined by the command byte is then sent from the IS31FL3748 to the master (Figure 30).

To read the registers of Page 1 thru Page 9, the 7Ah should write with xxh (56h,58h...6Eh) before follow the Figure 31 sequence to read the data. For example, when you want to read registers of Page 9, first the 7Eh should write with C6h (unlock command when you change page before), second FDh should write with 6Eh, third you can read the Page 9 data.

IS31FL3748

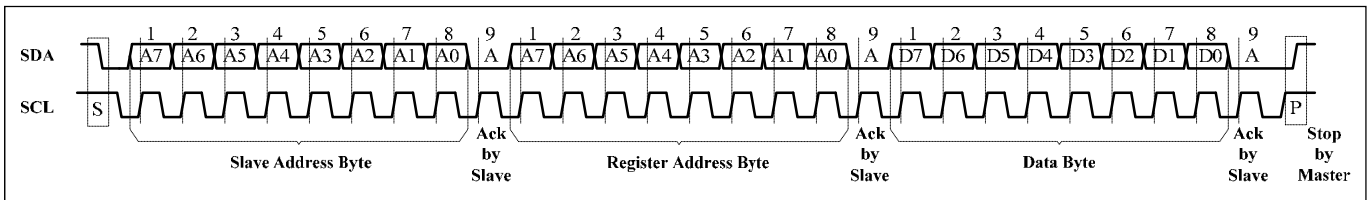
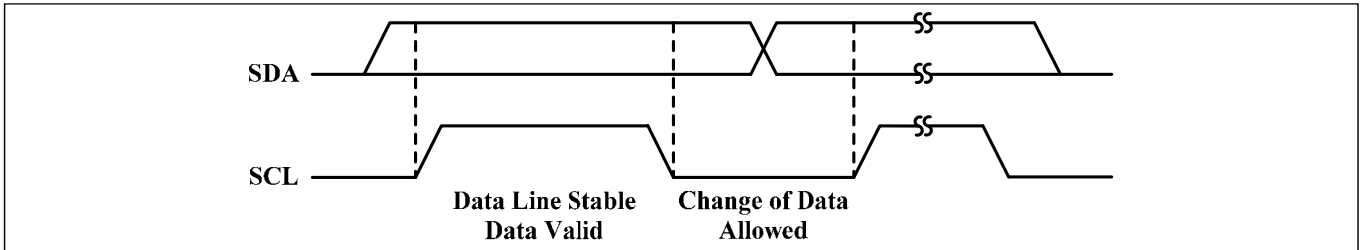
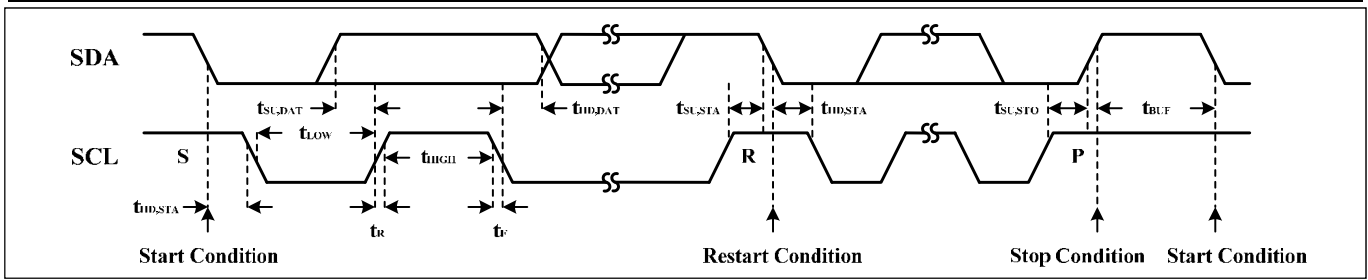


Figure 28 I2C Writing to IS31FL3748 (Typical)

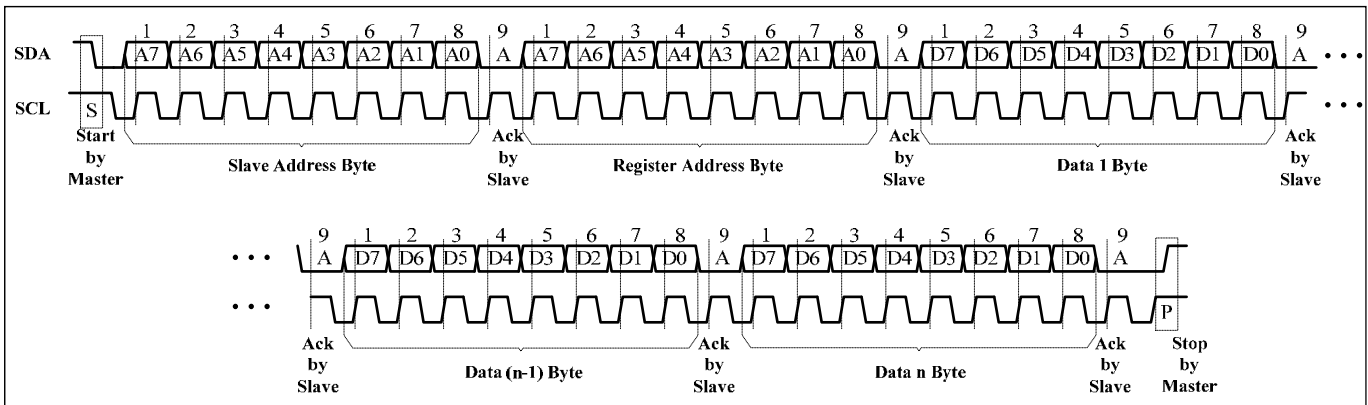


Figure 29 I2C Writing to IS31FL3748 (Automatic Address Increment)

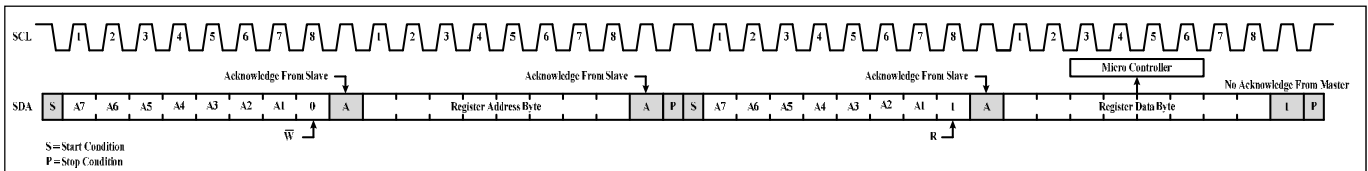


Figure 30 I2C Reading from IS31FL3748

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REGISTER DEFINITIONS

Table 5 Command Register Definition

| Address | Name | Function | Table | R/W | Default |
|---------|-----------------------------|--------------------------------------|-------|-----|-----------|
| 7Eh | Command Register Write Lock | To unlock Command Register | - | W | 0000 0000 |
| 7Ah | Command Register | Available Page 1 to Page 9 Registers | 6 | W | 0101 0110 |

Note 7: For SPI mode only, the command already include the page information and it does not need to unlock the command register.

REGISTER PAGE CONTROL

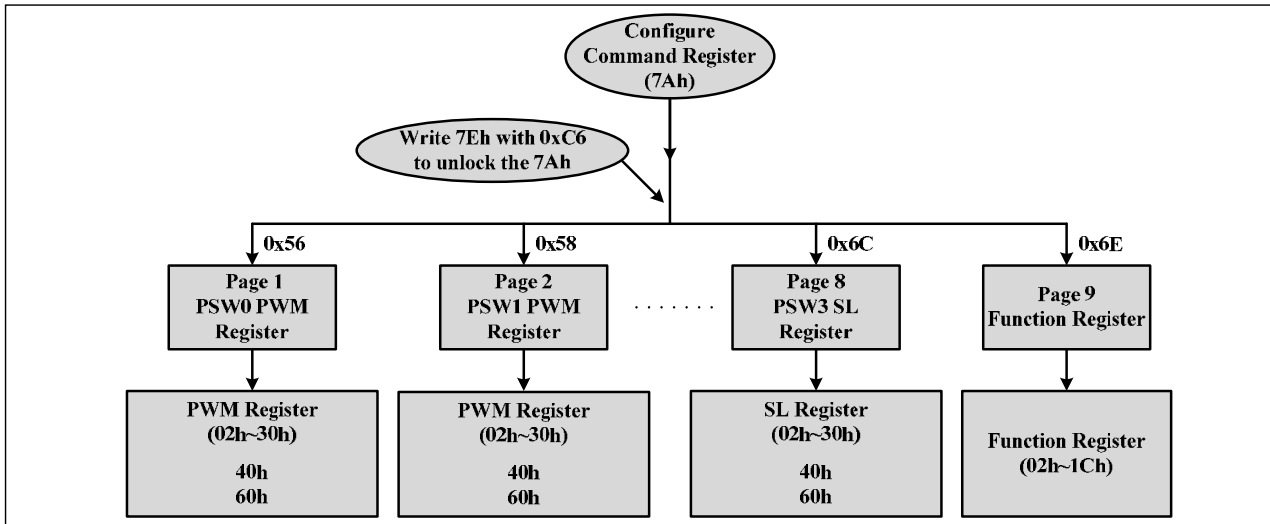


Figure 31 Register Pages (For HSB, DSB and I2C Mode Only)

Table 6 7Ah Command Register

| Data | Hex | Function |
|-----------|------|---|
| 0101 0110 | 0x56 | Point to Page 1(PG1): PSW0-PWM (PSW0 page PWM Register is available) |
| 0101 1000 | 0x58 | Point to Page 2(PG2): PSW1-PWM (PSW1 page PWM Register is available) |
| 0101 1010 | 0x5A | Point to Page 3(PG3): PSW2-PWM (PSW2 page PWM Register is available) |
| 0101 1100 | 0x5C | Point to Page 4(PG4): PSW3-PWM (PSW3 page PWM Register is available) |
| 0110 0110 | 0x66 | Point to Page 5(PG5): PSW0-SL (PSW0 page Current Scaling Register is available) |
| 0110 1000 | 0x68 | Point to Page 6(PG6): PSW1-SL (PSW1 page Current Scaling Register is available) |
| 0110 1010 | 0x6A | Point to Page 7(PG7): PSW2-SL (PSW2 page Current Scaling Register is available) |
| 0110 1100 | 0x6C | Point to Page 8(PG8): PSW3-SL (PSW3 page Current Scaling Register is available) |
| 0110 1110 | 0x6E | Point to Page 9(PG9): Function Register Page |
| 1000 0001 | 0x81 | PWM update register, for SPI only. |
| Others | - | Not allowed |

Note 8: Register 7Ah is not in any of above pages and it can swap the pages at any time, when power up, default page is page 1(7Ah=0x56), and all the writing is in page 1 if not swap to other pages. Follow the sequence can swap to new page:

HSB/DSB mode: "Start Command"->"Slave address" -> 7Eh="0xC6" ->7Ah= "Command Register Value" (page number) -> "End Command", 7Eh set to "0xC6" is to unlock the 7Ah.

SPI mode: The SPI command already includes page information, see table 3 for detail information.

For example, when write "0110 0110" (0x66) in the Command Register (7Ah), the data which writing after will be stored in page 5, PSW0-SL page, the White balance Scaling Register of PSW0.

For example, when write "0110 1110" (0x6E) in the Command Register (7Ah), the data which writing after will be stored in page 9, Function Register page.

When in SPI mode, the PWM data need to be updated with the writing 0x00 to 81h register, 81h is not belong to any pages, anytime when user writing the 81h, the PWM data will be updated.

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Table 7 Register Definition

| Address | Name | Function | Table | R/W | Default |
|---|--------------------|------------------------|-------|-----|-----------|
| PG1 (0x56): PWM Register of PSW0 | | | | | |
| 02h~30h | PWM Register | Set PWM value for PSW0 | 9 | W | 0000 0000 |
| 40h | All Channel Select | Set global channel | | W | 0000 0000 |
| 60h | Special Mode | Set special mode | | W | 0000 0000 |
| PG2 (0x58): PWM Register of PSW1 | | | | | |
| 02h~30h | PWM Register | Set PWM value for PSW1 | 9 | W | 0000 0000 |
| 40h | All Channel Select | Set global channel | | W | 0000 0000 |
| 60h | Special Mode | Set special mode | | W | 0000 0000 |
| PG3 (0x5A): PWM Register of PSW2 | | | | | |
| 02h~30h | PWM Register | Set PWM value for PSW2 | 9 | W | 0000 0000 |
| 40h | All Channel Select | Set global channel | | W | 0000 0000 |
| 60h | Special Mode | Set special mode | | W | 0000 0000 |
| PG4 (0x5C): PWM Register of PSW3 | | | | | |
| 02h~30h | PWM Register | Set PWM value for PSW3 | 9 | W | 0000 0000 |
| 40h | All Channel Select | Set global channel | | W | 0000 0000 |
| 60h | Special Mode | Set special mode | | W | 0000 0000 |
| PG5 (0x66): SL Register of PSW0 | | | | | |
| 02h~30h | SL Register | Set SL value for PSW0 | 11 | W | 1111 1110 |
| 40h | All Channel Select | Set global channel | | W | 1111 1110 |
| 60h | Special Mode | Set special mode | | W | 1111 1110 |
| PG6 (0x68): SL Register of PSW1 | | | | | |
| 02h~30h | SL Register | Set SL value for PSW1 | 11 | W | 1111 1110 |
| 40h | All Channel Select | Set global channel | | W | 1111 1110 |
| 60h | Special Mode | Set special mode | | W | 1111 1110 |
| PG7 (0x6A): SL Register of PSW2 | | | | | |
| 02h~30h | SL Register | Set SL value for PSW2 | 11 | W | 1111 1110 |
| 40h | All Channel Select | Set global channel | | W | 1111 1110 |
| 60h | Special Mode | Set special mode | | W | 1111 1110 |
| PG8 (0x6C): SL Register of PSW3 | | | | | |
| 02h~30h | SL Register | Set SL value for PSW3 | 11 | W | 1111 1110 |
| 40h | All Channel Select | Set global channel | | W | 1111 1110 |
| 60h | Special Mode | Set special mode | | W | 1111 1110 |

Table 8 Register Definition (Continued)

| Address | Name | Function | Table | R/W | Default |
|--------------------------------------|--|---|-------|-----|-----------|
| PG9 (0x6E): Function Register | | | | | |
| 02h | Configuration Register | Set operating mode | 13 | W | 0000 0010 |
| 04h | Global Current Control Register | Set global current for R channels | 14 | W | 1111 1110 |
| 06h | | Set global current for G channels | | W | |
| 08h | | Set global current for B channels | | W | |
| 0Ah | Spread Spectrum Register | Set spread spectrum and SYNC function | 15 | W | 0000 0000 |
| 0Eh | Power Noise Reduction (PNR) Register | Power noise reduction setting | 16 | W | 1001 0000 |
| 10h | Temperature Status Register | Temperature thermal roll off setting | 17 | W | 0000 0000 |
| 12h~28h | Open Detect Register | Store the open information of LED | 18~20 | R | 0000 0000 |
| 30h | Pull Down Voltage Selection Register 1 | Set de-ghost option: pull down voltage for PSW0 and PSW1 | 21 | W | 0000 0000 |
| 32h | Pull Down Voltage Selection Register 2 | Set de-ghost option: pull down voltage for PSW2 and PSW3 | 22 | W | 0000 0000 |
| 34h | Pull Up Voltage Selection Register 1 | CSx pull up voltage selection | 23 | W | 0000 0000 |
| 36h | Pull Up Voltage Selection Register 2 | CSx pull up voltage selection and PSW pull 1.5x mode enable | 24 | W | 0000 0000 |
| 3Eh | Software Reset Register | Enable software reset function | - | W | 0000 0000 |
| 78h | Fault State Register | For reading the fault state | 25 | R | 0000 0000 |

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Table 9 PWM Register: PG1~PG4 (7Ah=0x56~0x5C): PWM Register of PSW0~PSW3
Data bytes set PWM value.

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register | Remark |
|-----|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------------|
| 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | /CS00 | |
| 04h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | /CS01 | |
| 06h | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | /CS02 | |
| ... | | | | | | | | | ... | |
| 30h | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | /CS23 | |
| 40h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Global | Default Local |
| 60h | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Special | Default Normal |

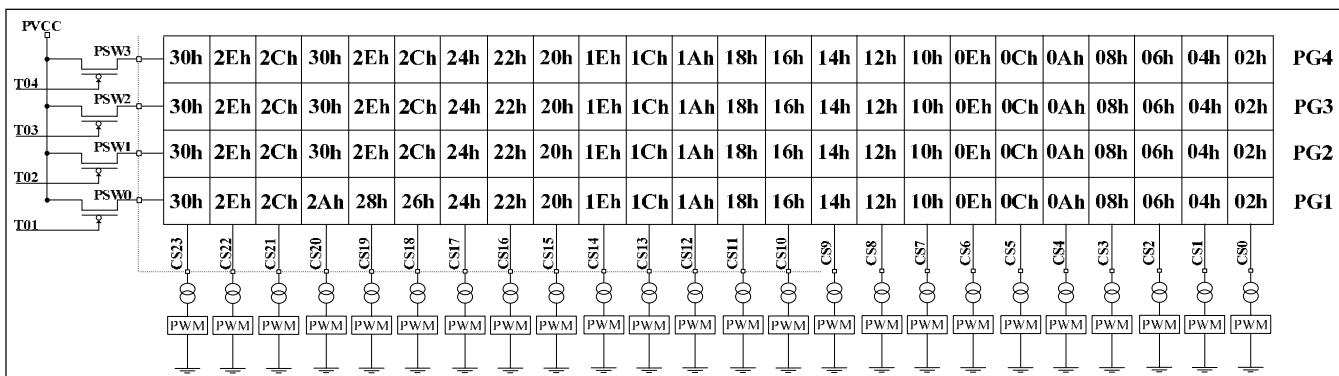


Figure 32 PWM Register

60h is for HSB and DSB interface only. Data bytes set PWM value. (Bit 0 must be “0” for HSB and DSB mode.)

Table 10 Data Bytes: PWM Value

Data bytes set PWM value. (Bit 0 must be zero for HSB and DSB mode)

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | PWM Dimming (for reference only) |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------------------|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/128, OFF (Default) |
| 02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1/128 |
| 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2/128 |
| | | | | | | | | | |
| FC | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 126/128 |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 127/128 |

Data bytes set PWM value. (For SPI and I2C mode, Bit 0 can be “1”)

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | PWM Dimming (for reference only) |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------------------|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/256, OFF (Default) |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/256 |
| 02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2/256 |
| | | | | | | | | | |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254/256 |
| FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255/256 |

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Table 11 Register: PG5~PG8 (7Ah= 0x66~0x6C): SL Register of PSW0~PSW3
Data bytes set dot correction (SL) value.

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register | Remark |
|-----|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------------|
| 02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | /CS00 | |
| 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | /CS01 | |
| 06 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | /CS02 | |
| ... | | | | | | | | | ... | |
| 30 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | /CS23 | |
| 40 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Global | Default Local |
| 60 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Special | Default Normal |

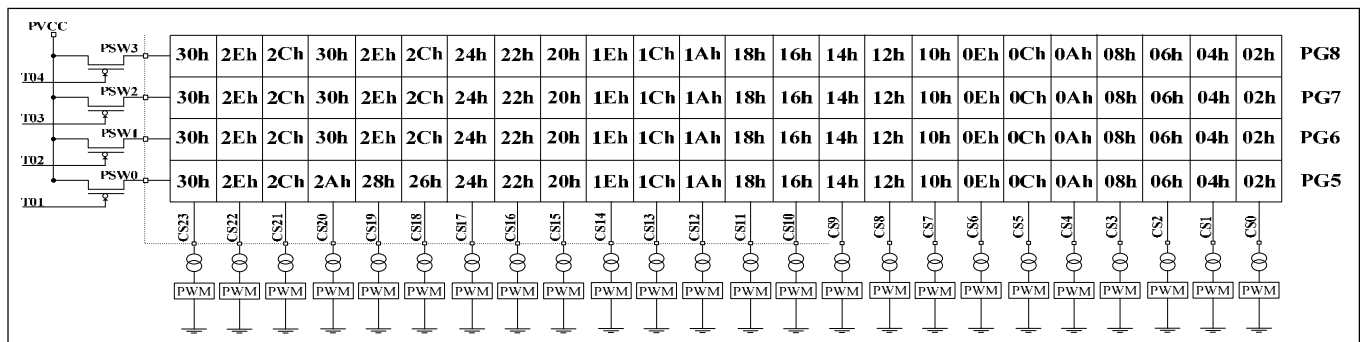


Figure 33 SL Register

60h is also for HSB and DSB interface only. Data bytes set dot correction (SL) value. (Bit 0 must be “0” for HSB and DSB mode.)

Table 12 Data bytes: SL Current Scaling Value

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | SL Current (of maximum, for reference only) |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|---|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/128, OFF(Default) |
| 02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1/128 |
| 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2/128 |
| 06 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3/128 |
| | | | | | | | | | |
| FC | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 126/128 |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 127/128 |

Data bytes set current scale value. (For SPI and I2C mode, Bit 0 can be “1”)

| HEX | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | SL current (of maximum, for reference only) |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|---|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/256, OFF(Default) |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/256 |
| 02 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2/256 |
| 03 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3/256 |
| | | | | | | | | | |
| FE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254/256 |
| FF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255/256 |

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Function Register: PG9 (7Ah= 0x6E)

Table 13 02h Configuration Register

| Bit | D7 | D6:D4 | D3:D2 | D1 | D0 |
|---------|----|-------|-------|-----|----|
| Name | - | SWS | PWMF | SSD | - |
| Default | - | 000 | 00 | 1 | 0 |

The Configuration Register sets operating mode of IS31FL3748. When SSD is “0”, IS31FL3748 works in software shutdown mode. When SSD is set to “1”, IS31FL3748 works in normal operate mode.

SWS control the duty cycle of the PSWx, default mode is 1/4.

| | |
|------------|---|
| SWS | PSWx Scan Setting |
| 000 | PSW0~PSW3 scan, 1/4 |
| 001 | PSW0~PSW2 scan, PSW3 no-active |
| 010 | PSW0~PSW1 scan, PSW2 and PSW3 no-active |
| 011 | Only PSW0 scan, PSW1~PSW3 no-active |
| 100 | PSW0~PSW1 scan, PSW2=PSW0, PSW3=PSW1 |

| | |
|-------------|-----------------|
| PWMF | PWM Frequency |
| 00 | 32kHz (default) |
| 01 | 64kHz |
| 10 | 1kHz |
| 11 | 500Hz |

| | |
|------------|---------------------------|
| SSD | Software Shutdown Control |
| 0 | Software shutdown |
| 1 | Normal operation |

Table 14 04h/06h/08h Global Current Control Register

| Bit | D7:D1 | D0 |
|---------|----------|----|
| Name | GCCx | - |
| Default | 1111 111 | 0 |

The Global Current Control Registers modulate all CSy (x=0~23) SL current which is noted as IO_{UT} in 128 steps.

04h is for R channels, GCCR, CS0, CS3, CS6 ... CS21

06h is for G channels, GCCG, CS1, CS4, CS7 ... CS22

08h is for B channels, GCCB, CS2, CS5, CS8 ... CS23

For HSB and DSB mode, IO_{UT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = \frac{40}{R_{ISET}} \times \frac{GCC}{128} \times \frac{SL}{128} \quad (1)$$

$$GCC = \sum_{n=1}^7 D[n] \cdot 2^n$$

$$SL = \sum_{n=1}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For SPI and I2C mode, IO_{UT} is computed by the Formula (2):

$$I_{OUT(PEAK)} = \frac{40}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (2)$$

$$GCC = \sum_{n=0}^7 D[n] \cdot 2^n$$

$$SL = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 15 0Ah Spread Spectrum Register

| Bit | D7:D6 | D5:D4 | D3:D2 | D1 | D0 |
|---------|-------|-------|-------|-----|----|
| Name | - | CLT | SYNC | SSP | - |
| Default | 00 | 00 | 00 | 0 | 0 |

Spread Spectrum Register set the spread spectrum (SSP) and synchronization function of IS31FL3748. The spread spectrum range is ±5%. When SSP enable, the spread spectrum function will be enabled and the CLT bits will adjust the cycle time of spread spectrum function.

| | |
|------------|----------------------------|
| CLT | Spread Spectrum Cycle Time |
| 00 | 1980µs |
| 01 | 1200µs |
| 10 | 820µs |
| 11 | 660µs |

| | |
|-------------|--------------------------------------|
| SYNC | Enable of SYNC Function |
| 0x | Disable SYNC function, 30kΩ pull-low |
| 10 | Slave, clock input |
| 11 | Master, clock output |

| | |
|------------|---------------------------------|
| SSP | Spread Spectrum Function Enable |
| 0 | Disable |
| 1 | Enable |

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Table 16 0Eh Power Noise Reduction (PNR) Register

| Bit | D7:D6 | D5:D4 | D3:D2 | D1:D0 |
|---------|-------|-------|-------|-------|
| Name | PNR_B | PNR_G | PNR_R | - |
| Default | 10 | 01 | 00 | 00 |

IS31FL3748 implemented a proprietary PWM algorithm which is to spread PWM rising and falling edges of each channel to minimize power line disturbance, hence to minimize power rail noise. Traditionally, all channels start PWM cycle at the same time, creating a large LED current switching transient on the power bus. Using this Power Noise Reduction (PNR) method, some LED rising and falling edges can be cancelled, some are spread at different time point, minimizing simultaneously switching power transient noise. The timing and definition are shown in the following figure.

Between each adjacent channel with the same starting PWM cycles, an internal clock delay is inserted to further spread the edges.

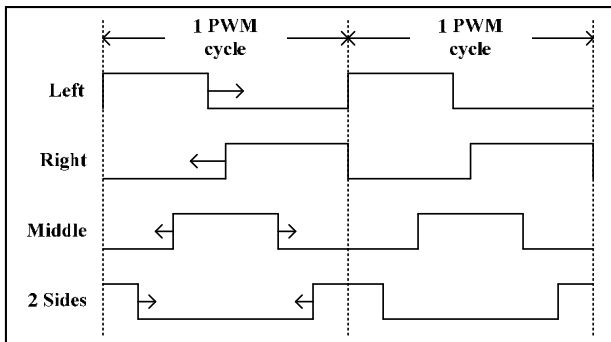


Figure 34 PWM Counting Position Definition

The PWM counting direction is programmable for each color group, for all R channel, G channel and B channel, defined by PNR[7:0]. Select different direction for R, G and B can minimize the power rail noise.

The default value of PNR_B is “10”, default value of PNR_G is “01”, but before writing any value to 0Eh, if read out the 0Eh, the read result is always 0x00. After writing 0Eh with correct value, the reading result will be same as 0Eh is written.

| | |
|--------------|-----------------------|
| PNR_B | PNR for blue channels |
| 00 | Left |
| 01 | Right |
| 10 | Middle (default) |
| 11 | Two sides |

| | |
|--------------|------------------------|
| PNR_G | PNR for green channels |
| 00 | Left |
| 01 | Right (default) |
| 10 | Middle |
| 11 | Two sides |

| | |
|--------------|----------------------|
| PNR_R | PNR for red channels |
| 00 | Left (default) |
| 01 | Right |
| 10 | Middle |
| 11 | Two sides |

Table 17 10h Temperature Status Register

| Bit | D7:D6 | D5:D4 | D3 | D2 | D1 | D0 |
|---------|-------|-------|-----|------|-----|----|
| Name | TS | TROF | ODE | GOFF | GON | - |
| Default | 00 | 00 | 0 | 0 | 0 | 0 |

TS store the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

| | |
|-----------|---|
| TS | Temperature Point, Thermal Roll Off start point |
| 00 | 140°C |
| 01 | 120°C |
| 10 | 100°C |
| 11 | 90°C |

| | |
|-------------|------------------------------|
| TROF | Percentage Of Output Current |
| 00 | 100% |
| 01 | 75% |
| 10 | 55% |
| 11 | 30% |

| | |
|------------|--------------------|
| ODE | Open Detect Enable |
| 0 | Disable |
| 1 | Enable |

| | |
|-------------|---|
| GOFF | All PWM off, if GON= “1”, GOFF will reset GON to “0” |
| 0 | Function off (default) |
| 1 | All channel’s PWM= 0x00 (HSB & DSB: 0/128) (SPI & I2C: 0/256) |

| | |
|------------|--|
| GON | All PWM On |
| 0 | Function off (default) |
| 1 | DC Mode (HSB & DSB:128/128) (SPI & I2C: 256/256) |

Table 18 12h/18h/1Eh/24h R Open Status Register of PSW0/PSW1/PSW2/PSW3

| Bit | D7:D0 |
|---------|------------|
| Name | OPR7: OPR0 |
| Default | 0000 0000 |

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Table 19 14h/1Ah/20h/26h G Open Status Register of PSW0/PSW1/PSW2/PSW3

| Bit | D7:D0 |
|---------|------------|
| Name | OPG7: OPG0 |
| Default | 0000 0000 |

Table 20 16h/1Ch/22h/28h B Open Status Register of PSW0/PSW1/PSW2/PSW3

| Bit | D7:D0 |
|---------|------------|
| Name | OPB7: OPB0 |
| Default | 0000 0000 |

The open status register stores the open information of LED string. PSW0 is 12h, 14h, 16h; PSW1 is 18h 1Ah 1Ch; PSW2 is 1Eh 20h 22h; PSW3 is 24h 26h 28h.

To get the correct open information, several configurations are recommended to set before setting the ODE bit (D3 of 10h):

- 1 SL=0xFF. LSB of SL register should be set to "1". For example, if set SL= "0xFE", can't read correct open information. If set SL= "0xFF", can read correct open information. Recommend to set SL registers to 0xFF. Notice the default value of SL is 0xFE.
- 2 GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open information.
- 3 PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open information.
- 4 Disable PSWx Pull Down Voltage and CSy Pull Up Voltage. 30h=0x00, 32h=0x00, 34h=0x00, 36h=0x00.

Table 21 30h Pull Down Voltage Selection Register 1

| Bit | D7 | D6:D4 | D3:D1 | D0 |
|---------|----|--------|--------|----|
| Name | - | PSW0PD | PSW1PD | - |
| Default | 0 | 000 | 000 | 0 |

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3748 has integrated Pull down voltage for each PSWx (x=0~3) and Pull up voltage for each CSy (y=0~23). Select the right PSWx Pull down voltage (30h, 32h) and CSy Pull up voltage (34h, 36h) which eliminates the ghost LED for a particular matrix layout configuration.

The PSWx pull down voltage and CSy pull up voltage are active only when the CSy/PSWx output working

the OFF state and therefore no power is lost through these voltages setting.

When IS31FL3748 works in hardware shutdown mode, the de-ghost function should be disabled.

PSWxPD PSWx Pull Down Voltage Selection Bit, 1x Mode, PSWVS= "0" in 36h

| | |
|-----|-----------------|
| 000 | No pull down |
| 001 | 0V (PVCC≤6V) |
| 010 | 1.4V (PVCC≤10V) |
| 011 | 2.8V (PVCC≤13V) |
| 100 | 4.2V |
| 101 | 5.6V |
| 110 | 7.0V |
| 111 | 8.4V |

PSWxPD PSWx Pull Down Voltage Selection Bit, 1.5x Mode, PSWVS= "1" in 36h

| | |
|-----|-----------------|
| 000 | No pull down |
| 001 | 0V (PVCC≤6V) |
| 010 | 2.1V (PVCC≤10V) |
| 011 | 4.2V (PVCC≤13V) |
| 100 | 6.3V |
| 101 | 8.4V |
| 110 | 10.5V |
| 111 | 12.6V |

Table 22 32h Pull Down Voltage Selection Register 2

| Bit | D7 | D6:D4 | D3:D1 | D0 |
|---------|----|--------|--------|----|
| Name | - | PSW2PD | PSW3PD | - |
| Default | 0 | 000 | 000 | 0 |

PSWxPD PSWx Pull Down Voltage Selection Bit, 1x Mode, PSWVS= "0" in 36h

| | |
|-----|-----------------|
| 000 | No pull down |
| 001 | 0V (PVCC≤6V) |
| 010 | 1.4V (PVCC≤10V) |
| 011 | 2.8V (PVCC≤13V) |
| 100 | 4.2V |
| 101 | 5.6V |
| 110 | 7.0V |
| 111 | 8.4V |

PSWxPD PSWx Pull Down Voltage Selection Bit, 1.5x Mode, PSWVS= "1" in 36h

| | |
|-----|-----------------|
| 000 | No pull down |
| 001 | 0V (PVCC≤6V) |
| 010 | 2.1V (PVCC≤10V) |
| 011 | 4.2V (PVCC≤13V) |
| 100 | 6.3V |
| 101 | 8.4V |
| 110 | 10.5V |
| 111 | 12.6V |

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Table 23 34h Pull Up Voltage Selection Register 1

| Bit | D7 | D6:D4 | D3:D1 | D0 |
|---------|----|--------|--------|----|
| Name | - | CSRPUV | CSGPUV | - |
| Default | 0 | 000 | 000 | 0 |

| | |
|---------------|-----------------------------------|
| CSxPUV | CSx Pull up Voltage Selection Bit |
| 000 | No pull up |
| 001 | PVCC |
| 010 | PVCC-7.0V |
| 011 | PVCC-5.6V |
| 100 | PVCC-4.2V |
| 101 | PVCC-2.8V |
| 110 | PVCC-1.4V |
| 111 | PVCC-1.0V |

Table 24 36h Pull Up Voltage Selection Register 2

| Bit | D7 | D6:D4 | D3 | D2 | D1 | D0 |
|---------|----|--------|----|-------|-------|----|
| Name | - | CSBPUV | - | PSWVS | PSWTS | - |
| Default | 0 | 000 | 0 | 0 | 0 | 0 |

| | |
|---------------|-----------------------------------|
| CSxPUV | CSx Pull up Voltage Selection Bit |
| 000 | No pull up |
| 001 | PVCC |
| 010 | PVCC-7.0V |
| 011 | PVCC-5.6V |
| 100 | PVCC-4.2V |
| 101 | PVCC-2.8V |
| 110 | PVCC-1.4V |
| 111 | PVCC-1.0V |

| | |
|--------------|--|
| PSWVS | PSW Pull Down Voltage 1.5x Selection Bit |
| 0 | Disable |
| 1 | Enable |

| | |
|--------------|---|
| PSWTS | PSW Pull Down Only During the Interval Time |
| 0 | SW pull down in PSWx off time |
| 1 | SW pull down in tNOL |

3Eh Software Reset Register

Write Software Reset Register with 0x00 will reset all the register to default value.

Table 25 78h Fault State Register

| Bit | D7:D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-------|----|------|------|----|----|----|
| Name | - | OF | TSDf | PSWS | | | |
| Default | 00 | 0 | 0 | 0000 | | | |

Fault State Register stores the PSW_y pins short to ground fault information, thermal shutdown flag and LED open flag.

To get the correct open information, several configurations are recommended to set before setting the ODE bit (D3 of 10h):

- 1 SL=0xFF. LSB of SL register should be set to "1". For example, if set SL="0xFE", can't read correct open information. If set SL="0xFF", can read correct open information. Recommend to set SL registers to 0xFF. Notice the default value of SL is 0xFE.
- 2 GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open information.
- 3 PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open information.
- 4 Disable PSW_x Pull Down Voltage and CS_y Pull Up Voltage. 30h=0x00, 32h=0x00, 34h=0x00, 36h=0x00.

After ODE bit enable, if LED open is detected, the OF bit will be set to 1.

| | |
|-------------|---|
| PSWS | PSW_y Short to Ground Fault Flag |
| 0000 | PSW3:PSW0 are normal, no short to ground happens |
| xxx1 | PSW0 short to ground fault happens |
| xx1x | PSW1 short to ground fault happens |
| x1xx | PSW2 short to ground fault happens |
| 1xxx | PSW3 short to ground fault happens |

| | |
|-------------|-------------------------------|
| TSDf | Thermal Shutdown Flag. |
| 0 | No thermal shutdown happens |
| 1 | Thermal shutdown happens |

| | |
|-----------|-------------------------|
| OF | Open Fault Flag. |
| 0 | No LED open happens |
| 1 | LED open happens |

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APPLICATION INFORMATION

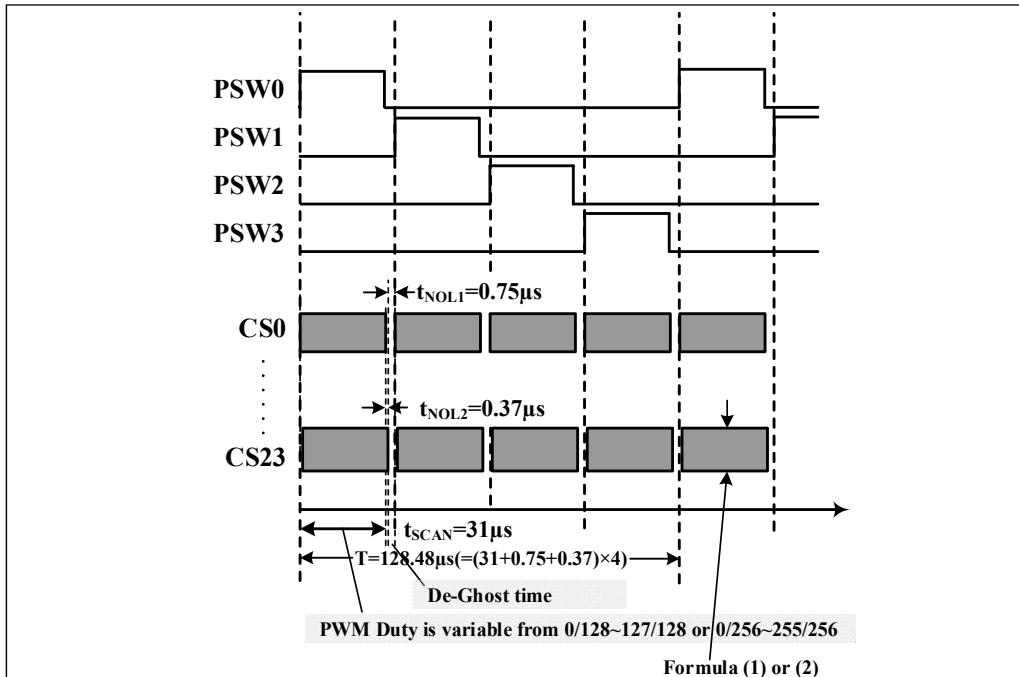


Figure 35 Scanning Timing (PWMF=32kHz)

SCANNING TIMING

As shown in Figure 35, the PSW0~PSW3 is turned on by serial, LED is driven 4 by 4 within the PSW_x (x= 0~3) on time (PSW_x, x= 0~3 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of PSW_x (active high, x= 0~3, SWS= "000") is:

$$Duty = \frac{31\mu s}{(31\mu s + 0.75\mu s + 0.37\mu s)} \times \frac{1}{4} = \frac{1}{4.12} \quad (3)$$

Where 31μs is t_{SCAN}, the period of scanning, 0.75μs is t_{NOL1}, 0.37μs is t_{NOL2}, the non-overlap time and CS_y (y= 0~23) delay time.

If SWS= "001", the duty cycle is:

$$Duty = \frac{31\mu s}{(31\mu s + 0.75\mu s + 0.37\mu s)} \times \frac{1}{3} = \frac{1}{3.09} \quad (3)$$

PWM CONTROL

After setting the I_{OUT}, GCC_x and SL, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula below.

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For HSB and DSB mode, I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = \frac{40}{R_{ISET}} \times \frac{GCC}{128} \times \frac{SL}{128} \quad (1)$$

$$GCC = \sum_{n=1}^7 D[n] \cdot 2^n$$

$$SL = \sum_{n=1}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For SPI and I2C mode, I_{OUT} is computed by the Formula (2):

$$I_{OUT(PEAK)} = \frac{40}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (2)$$

$$GCC = \sum_{n=0}^7 D[n] \cdot 2^n$$

$$SL = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For HSB and DSB mode, the final average current of LED, I_{LED} is computed as Formula (4):

$$I_{LED} = \frac{PWM}{128} \times I_{OUT(PEAK)} \times Duty \quad (4)$$

$$PWM = \sum_{n=1}^7 D[n] \cdot 2^n$$

Where PWM is PWM Registers (PG1~PG4, 02h~30h) data showing in Table 10.

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For SPI and I2C mode, the final average current of LED, I_{LED} is computed as Formula (5).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (5)$$

$$PWM = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where PWM is PWM Registers (PG1~PG4, 02h~30h) data showing in Table 10.

For example, for SPI and I2C mode, if $R_{ISET} = 1k\Omega$, $PWM = 255$, and $GCC = 255$, $SL = 255$, then

$$I_{OUT(PEAK)} = \frac{40}{1k\Omega} \times \frac{255}{256} \times \frac{255}{256} = 39.68mA$$

$$I_{LED} = I_{OUT(PEAK)} \times \frac{1}{4.12} \times \frac{PWM}{256}$$

OPERATING MODE

IS32FL3748 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth (SPI and I2C mode) or second step (HSB and DSB mode).

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN DETECT FUNCTION

IS32FL3748 has open detect bit for each LED.

The open status register stores the open information of LED string. PSW0 is 12h, 14h, 16h; PSW1 is 18h 1Ah 1Ch; PSW2 is 1Eh 20h 22h; PSW3 is 24h 26h 28h.

To get the correct open information, several configurations are recommended to set before setting the ODEN bit (D3 of 10h):

1. $SL = 0xFF$. LSB of SL register should be set to "1". For example, if set $SL = "0xFE"$, can't read correct open information. If set $SL = "0xFF"$, can read correct open information. Recommend to set SL registers to 0xFF. Notice the default value of SL is 0xFE.
2. $GCCx = 0x10$, too low or too high $GCCx$, like $GCCx = 0x01$, may read out incorrect open information.
3. $PWM = 0xFE$, too low PWM, like $PWM = 0x01$, may read out incorrect open information.
4. Disable PSWx Pull Down Voltage and CSy Pull Up Voltage. 30h=0x00, 32h=0x00, 34h=0x00, 36h=0x00.

DE-GHOST FUNCTION

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS32FL3748 has integrated Pull down voltage setting for each PSWx ($x=0\sim3$) and Pull up voltage setting for each CSy ($y=0\sim23$). Select the right PSWx Pull down voltage (PG9, 30h and 32h) and CSy Pull up voltage (PG9, 34 and 36h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, need to depending on how many LED is connect in series in one LED dot position, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon.

One LED: PSWxPD=2.8V, CSxPU=PVCC-2.8V

Two LEDs: PSWxPD=4.2V, CSxPU=PVCC-4.2V

Three LEDs: PSWxPD=7.0V, CSxPU=PVCC-7.0V

Four LEDs: PSWxPD=8.4V, CSxPU=PVCC-7.0V

Five LEDs: PSWxPD=10.5V, CSxPU=PVCC-7.0V

Six LEDs: PSWxPD=12.6V, CSxPU=PVCC-7.0V

More than six LEDs: PSWxPD=12.6V, CSxPU = PVCC-7.0V

When IS32FL3748 works in hardware shutdown mode, the de-ghost function should be disabled.

INTERFACE RESET

The HSB/DSB/SPI/I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the interface operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG9, 02h) to "0", the IS32FL3748 will operate in software shutdown mode. When the IS32FL3748 is in software shutdown, all current sources are switched off, so that the matrix is blanked.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown.

IS31FL3748

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS32FL3748 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1 μ F capacitor, if possible with a 0.47 μ F or 1 μ F capacitor is recommended to connected to the ground at each power supply pins of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

R_{ISSET}

R_{ISSET} should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. IS32FL3748 has thermal pad but the chip could be very hot if power is very large. So do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad thru 9 or 16 vias to be maximized the area size of ground plane.

The package thermal resistance, θ_{JA} , determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt ($^{\circ}\text{C}/\text{W}$).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (6)$$

So,

$$P_{D(MAX)} = \frac{125^{\circ}\text{C} - 25^{\circ}\text{C}}{37.3^{\circ}\text{C}/\text{W}} \approx 2.68\text{W}$$

Figure 36, shows the power derating of the IS31FL3748 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

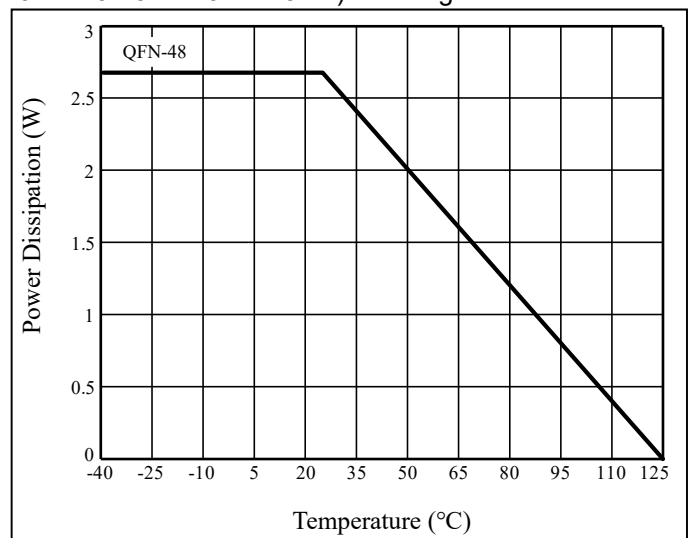


Figure 36 Dissipation Curve

Current Rating Example

For a R_{ISSET}= 1k Ω application, the current rating for each net is as follows:

- VCC and SWx pins= 39.6mA \times 24=950.4mA, recommend trace width: 0.3mm~0.5mm.
- CSy pins= 39.4mA, recommend trace width: 0.1016mm~0.254mm.
- All other pins < 15mA, recommend trace width: 0.1016mm~0.254mm.

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CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s) | 150°C 200°C 60-120 seconds |
| Average ramp-up rate (T _{smax} to T _p) | 3°C/second max. |
| Liquidous temperature (T _L) Time at liquidous (t _L) | 217°C 60-150 seconds |
| Peak package body temperature (T _p)* | Max 260°C |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | Max 30 seconds |
| Average ramp-down rate (T _p to T _{smax}) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

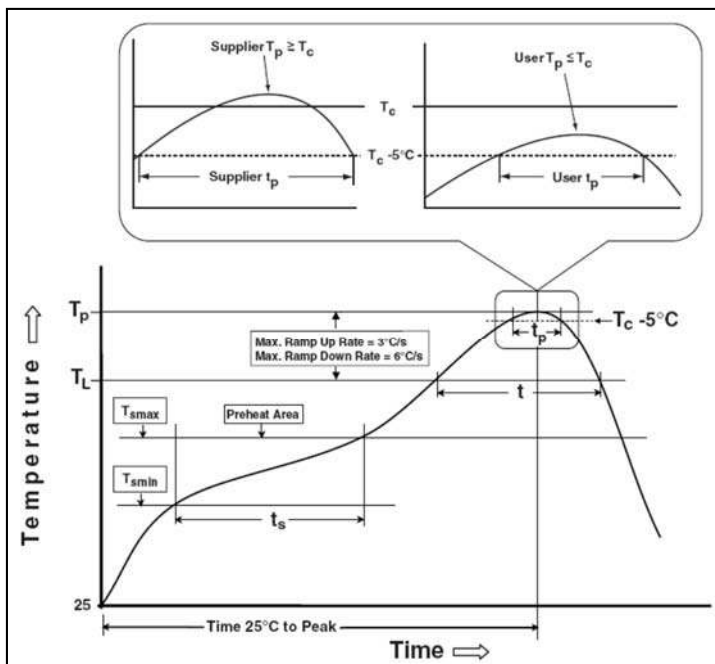
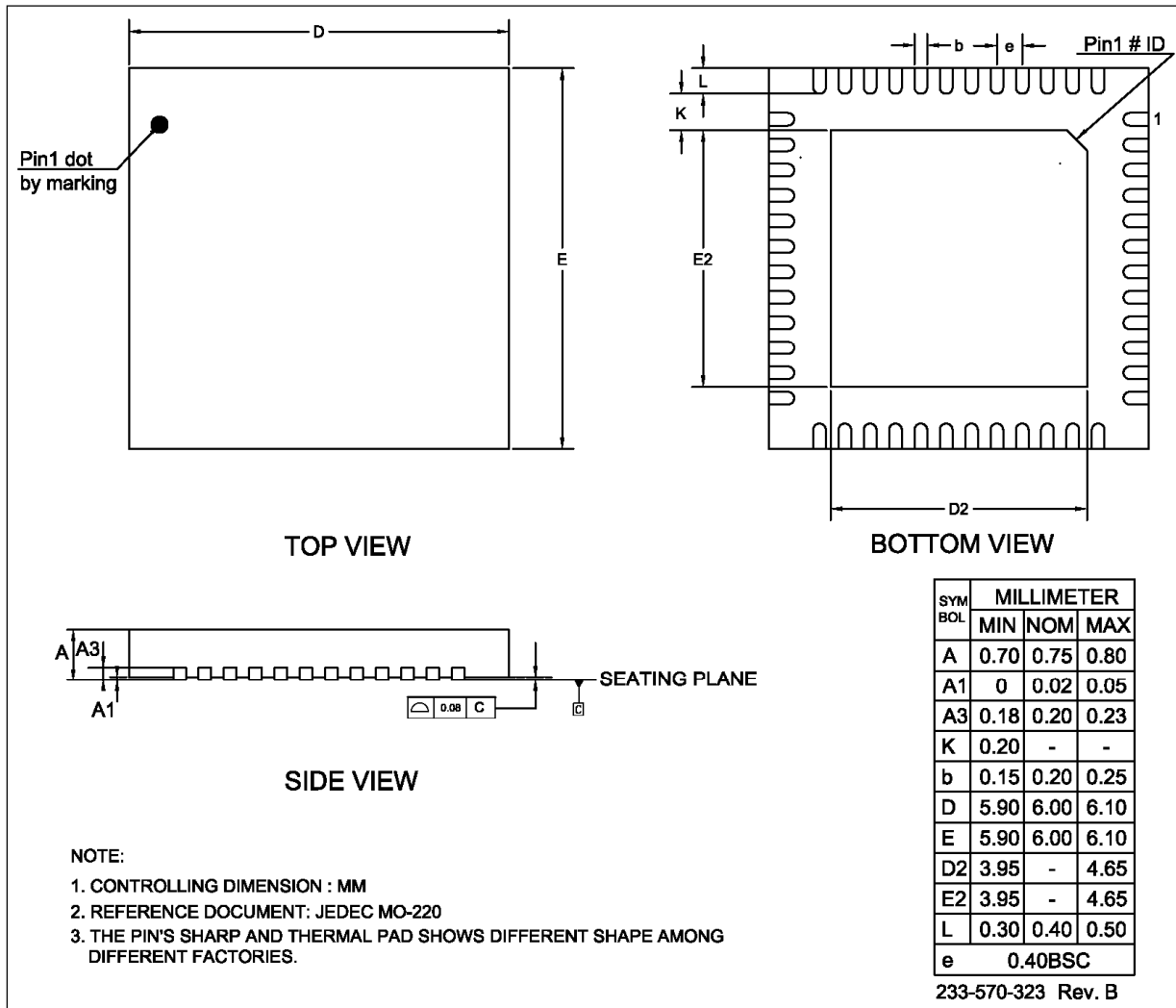


Figure 37 Classification profile

IS31FL3748

PACKAGE INFORMATION

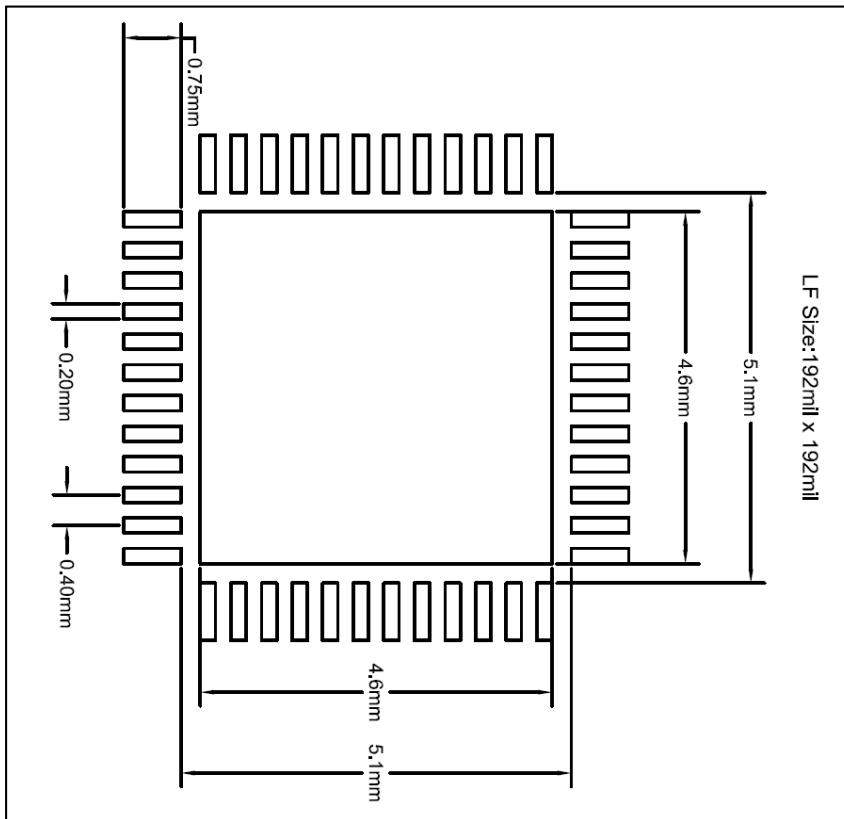
QFN-48



IS31FL3748

RECOMMENDED LAND PATTERN

QFN-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

| Revision | Detail Information | Date |
|----------|---|------------|
| A | Initial release | 2020.11.03 |
| B | 1. Update t_{ONL2} in EC table 2. Spread Spectrum range to $\pm 5\%$ 3. Update POD and land pattern | 2021.07.29 |
| C | 1. Add I2C interface 2. Correct the PWM frequency number(25.6kHz->32kHz) 3. Correct T, t_{NOL1} in Scanning timing figure and update t_{NOL2} value in EC table | 2021.09.15 |
| D | 1. Update POD and land pattern 2. Add I2C/SPI/HSB/DSB Switching characteristics 3. Add FAULTB pin and Fault State Register definition | 2021.12.22 |
| E | 1. Update HSB Switching Characteristics 2. Update SW pull-down register definition | 2022.02.24 |