Features

- **3.3V and 5V power supply options**
- **>2.5Gbps maximum throughput**
- **Fast output transitions <160ps t_r / t_f**
- **100k compatible PECL/ECL I/O**
- **Functionally equivalent to SY88927V and SY100EP16VS**
- **Variable output swing from 100mV to 700mV**
- **Guaranteed operation over –40°C to +85°C temperature range**
- **Available in ultra-small 8-pin MLF® (2mm x 2mm) package**

Applications

- **Multimode optical transceiver**
- **VCSEL driver**
- **Backplane receiver**

Precision Edge®

General Description

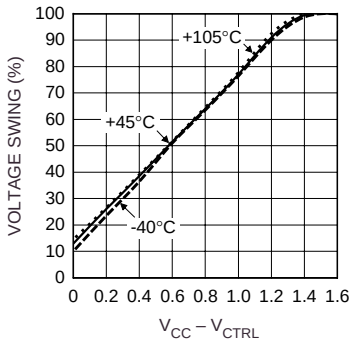
The SY89307V is a differential receiver with a variable output swing. It is functionally equivalent to the SY100EP16VS but in an ultra-small 8-lead MLF® package that features a 70% smaller footprint. Like the EP16VS its variable output swing makes it ideal for use as a VCSEL laser driver.

The operational range of the SY89307V control input is from V_{BB} (maximum output swing) to V_{CC} (minimum output swing). The output swing can be controlled by a variable resistor between the V_{BB} pin and V_{CC} with the wiper driving V_{CTRL}.

The SY89307V provides a V_{BB} output for either single-ended use or as a DC bias for AC-coupling to the device. The V_{BB} pin should be used only as a bias for this device as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01µF capacitor.

Under open input conditions the Q output will be LOW.

Typical Operating Characteristics



Typical Voltage Output Swing
V_{CC} = 3.3V or 5V

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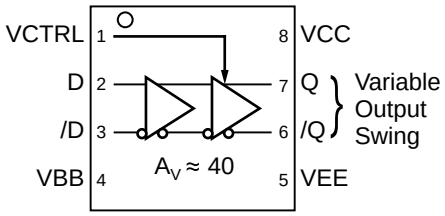


TOP VIEW
8-Pin MLF®
Ultra-Small Outline
(2mm x 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89307VMITR	MLF-8	Industrial	P16S	Sn-Pb
SY89307VMGTR(1)	MLF-8	Industrial	P16S with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

Pin Number	Pin Name	Type	Pin Function
2, 3	D, /D	100K ECL Input	Differential PECL/ECL Inputs: If inputs are left open, Q output will default to LOW. See “Input Interface Applications” section for single-ended inputs.
7, 6	Q, /Q	100K PECL/ECL Output	Differential Outputs: Variable swing PECL/ECL output pair defaults to LOW if D inputs left open. See “Application Implementation” section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: V_{EE} and Exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V_{CC}–1.3V. Used as reference voltage when AC-coupling to the D, /D inputs. Bypass with 0.01µF capacitor to V_{CC}.
1	VCTRL	Control Voltage	Voltage Input: Variable voltage input to control output swings.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on D, /D ..... ±50mA
Current (V_{BB})
  Source or sink current on V_{BB}, **Note 3** ..... ±1.5mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage ($|V_{CC}–V_{EE}|$) ..... 3.0V to 3.6V
  ..... 4.5V to 5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance, (**Note 4**)
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB})
  Junction-to-Board ..... 56°C/W

V_{CC} = +3.3V ±10% or +5V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –3.3V ±10% or –5V ±10%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} –2V unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{EE}	Power Supply Current	Max V_{CC}, no load	—	—	51	mA
V_{OH}	Output HIGH Voltage		V_{CC}–1.085	—	V_{CC}–0.88	V
V_{OL}	Output LOW Voltage	V_{CTRL} = V_{BB}	V_{CC}–1.90	—	V_{CC}–1.650	V
	Output LOW Voltage	V_{CTRL} = V_{CC}	V_{CC}–1.125	—	V_{CC}–0.975	V
V_{IH}	Input HIGH Voltage		V_{CC}–1.165	—	V_{CC}–0.88	V
V_{IL}	Input LOW Voltage		V_{CC}–1.810	—	V_{CC}–1.475	V
V_{BB}	Bias Voltage		V_{CC}–1.38	—	V_{CC}–1.26	V
I_{IH}	Input HIGH Current	D, /D	—	—	150	µA
I_{IL}	Input LOW Current		0.5	—	—	µA
		V_{CTRL} = V_{IH}			80	µA

Notes:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Due to the limited drive capability use for input of the same package only.

4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

V_{CC} = +3.3V ±10% or +5V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –3.3V ±10% or –5V ±10%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} –2V unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Throughput	NRZ Data	2.5	—	—	Gbps
t_{pd}	Propagation Delay	D (Diff) D (SE)	100 100	— 250	300 400	ps
V_{PP}	Minimum Input Swing	**Note 5**	150	—	—	mV
V_{CMR}	Common Mode Range	**Note 6**	V_{CC}–1.3	—	V_{CC}–0.4	V
t_r, t_f	Output Rise/Fall Times (20% to 80%)	Q, /Q; **Note 7**	—	95	160	ps

Notes:

5. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40 when output has a full swing.
6. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V and V_{CC} = 0V. Note for PECL operation, the V_{CMR}(min.) will be fixed at 3.3V – |V_{CMR}(min.)|.
7. Output at full swing.

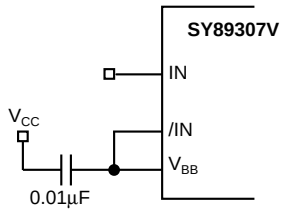


Figure 1. Single-Ended Input (Terminating Unused Input)

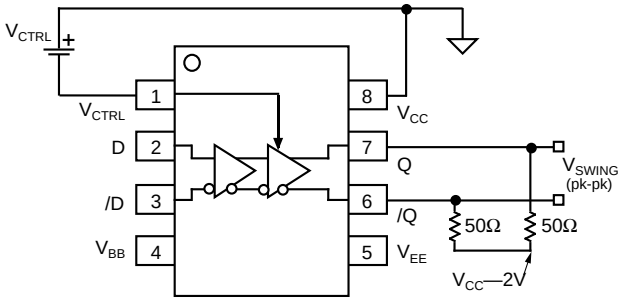


Figure 2. Voltage Source Implementation

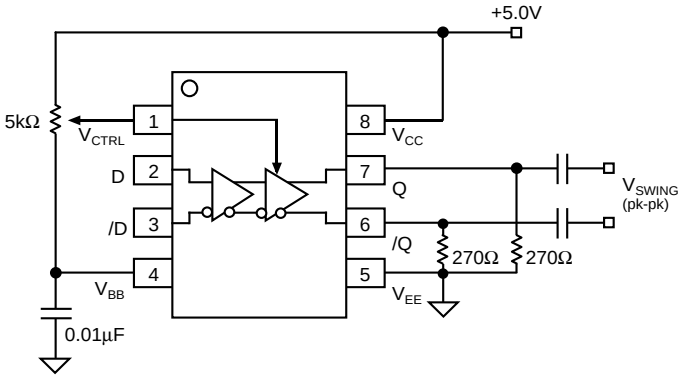
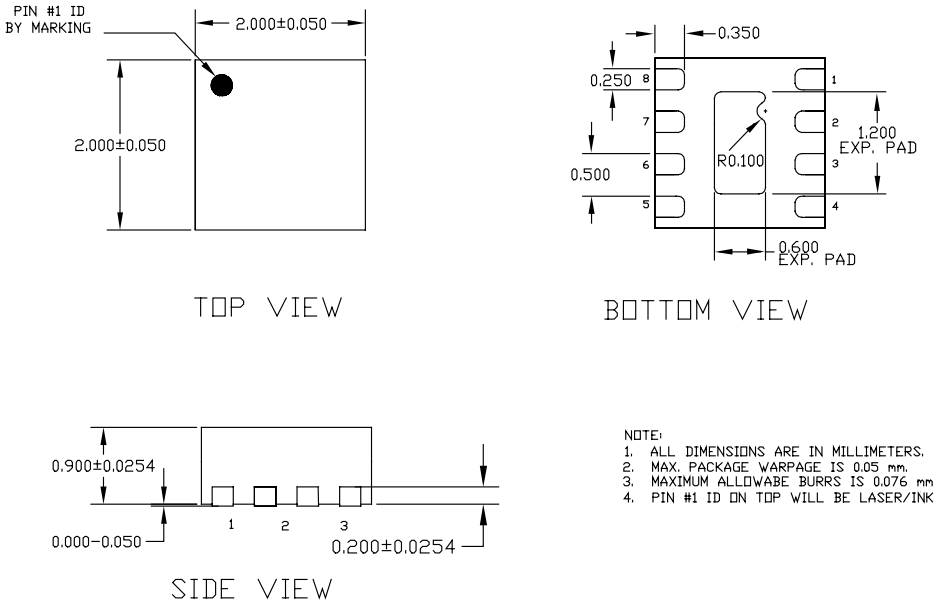
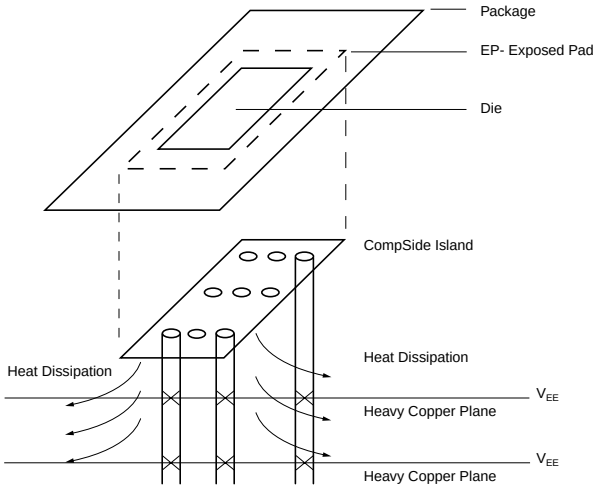


Figure 3. Alternative Implementation





PCB Thermal Consideration for 8-Pin MLF® Package

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a plane equivalent to device V_{EE} for proper thermal management.

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