HD-LINX™ GS1522
HDTV Serial Digital Serializer

DATA SHEET

FEATURES

- **SMPTE 292M compliant**
- **20:1 parallel to serial conversion**
- **NRZ(I) encoder & SMPTE scrambler with selectable bypass**
- **NRZ to NRZ(I) serial data conversion**
- **1.485Gb/s and 1.485/1.001Gb/s operation**
- **lock detect output**
- **selectable DUAL or QUAD 75Ω cable driver outputs**
- **8 bit or 10 bit input data support**
- **20 bit wide inputs**
- **Pb-free and Green**
- **3.3V and 5V CMOS/TTL compatible inputs**
- **single +5.0V power supply**

APPLICATIONS

SMPTE 292M Serial Digital Interfaces for Video Cameras, Camcorders, VTRs, Signal Generators, Portable Equipment, and NLEs.

DESCRIPTION

The GS1522 is a monolithic bipolar integrated circuit designed to serialize SMPTE 274M and SMPTE 260M bit parallel digital signals.

This device performs the following functions:

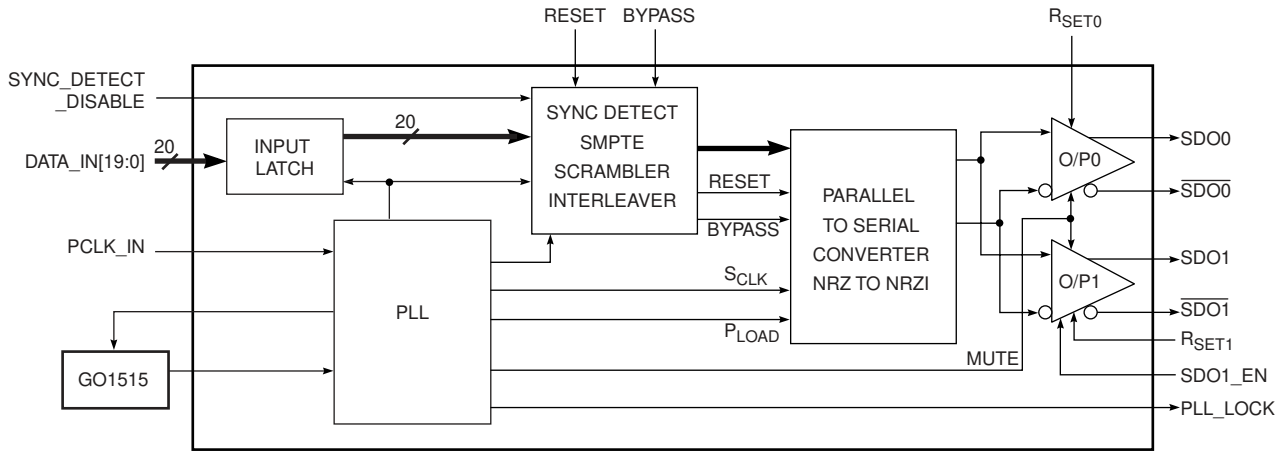
- Sync word mapping for 8-bit/10-bit operation.
- Parallel to Serial conversion of Luma & Chroma data
- Interleaving of Luma and Chroma data
- Data Scrambling (using the X^9+X^4+1 algorithm)
- Conversion of NRZ to NRZI serial data (using the (X+1) algorithm)
- Selectable DUAL or QUAD 75Ω Cable Driver outputs
- Lock Detect Output
- 1.485Gb/s or 1.485/1.001Gb/s operation

This device requires a single 5V supply and typically consumes less than 1000mW of power while driving two 75Ω cables.

The GS1522 uses the GO1515 external VCO connected to the internal PLL circuitry to achieve ultra low noise PLL performance.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS1522-CQR	128 pin MQFP	0°C to 70°C	No
GS1522-CQRE3	128 pin MQFP	0°C to 70°C	Yes



FUNCTIONAL BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	$V_{EE} - 0.5 < V_{IN} < V_{CC} + 0.5$
DC Input Current (any input)	TBD
Power Dissipation (V_{CC} = 5.25V)	TBD
Input ESD Voltage	TBD
Die Temperature	125°C
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-40°C \le T_S \le 150°C$
Lead Temperature (soldering 10 seconds)	260°C

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial data bit rate	SMPTE 292M	BR_{SDO}	-	1.485	-	Gb/s	1.485/1.001Gb/s also
Digital Serial Data Outputs	Differential outputs	V_{SDO}	750	800	850	mV p-p	With 52.3Ω 1% R_{SET} Resistor
	Rise/Fall times, 20-80%	t_r, t_f	-	150	270	ps	
	Overshoot		-	0	7	%	
	Output Return Loss @ 1.485GHz	ORL	15	17	-	dB	As per SMPTE292M (5MHz to clock frequency), using Gennum Evaluation Board, recommended layout and components.
Lock Time	Worst case	t_{LOCK}	-	200	250	ms	
Typical Loop Bandwidth	≤ 0.1dB peaking, 1.485Gb/s		-	0.200	1.5	MHz	
Intrinsic Jitter	Pseudo-random PRBS (2^{23}-1) (200kHz LBW)	t_{IJR}	-	-	100	ps p-p	
	Pathological PRBS (2^{23}-1) (200kHz LBW)	t_{IJP}	-	-	100	ps p-p	
	Pseudo-random (1.5 MHz LBW)	t_{IJR}	-	-	100	ps p-p	
	Pathological (1.5 MHz LBW)	t_{IJP}	-	-	100	ps p-p	

AC ELECTRICAL CHARACTERISTICS - PARALLEL TO SERIAL STAGE

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise specified.

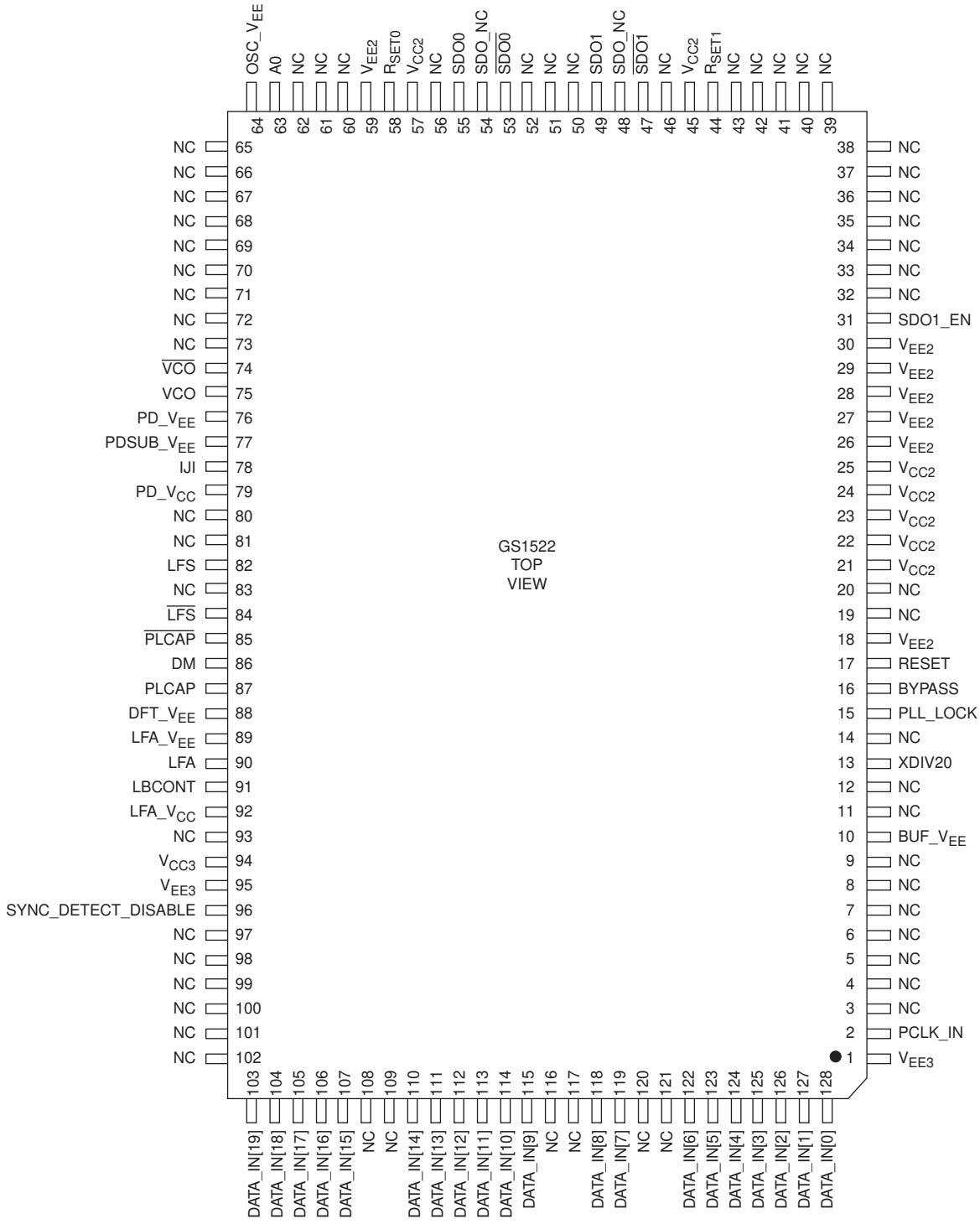
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Voltage Levels		V_{IL}	-	-	0.8	V	For compatibility with TTL voltage levels
		V_{IH}	2.0	-	-	V	For compatibility with TTL voltage levels
Input Capacitance		C_{IN}	-	1	2	pF	
Output Voltage Levels		V_{OL}	-	-	0.4	V	For compatibility with TTL voltage levels
		V_{OH}	2.4	-	-	V	For compatibility with TTL voltage levels
Parallel Input Clock Frequency		P_{CLK_IN}	-	74.25	-	MHz	74.25/1.001MHz also
Input Clock Pulse Width LOW		t_{PWL}	5	-	-	ns	
Input Clock Pulse Width HIGH		t_{PWH}	5	-	-	ns	
Input Clock Rise/Fall time		t_r, t_f	-	500	1000	ps	20% to 80%
Input Clock Rise/Fall time Matching		t_{rfm}	-	200	-	ps	
Input Setup Time		t_{SU}	1.0	-	-	ns	
Input Hold Time		t_{IH}	0	-	-	ns	

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	Operating Range	V_{CC}	4.75	5.00	5.25	V	
Power (system power)	V_{CC} = 5.00V, T=25°C	P_D	-	950	-	mW	(Driving two 75Ω outputs)
	V_{CC} = 5.00V, T=25°C	P_D	-	1170	-	mW	(Driving four 75Ω outputs)
Supply Current	V_{CC} = 5.25V, T=70°C		-	-	300	mA	(Driving four 75Ω outputs)
	V_{CC} = 5.00V, T=25°C		-	234	-	mA	(Driving four 75Ω outputs)
	SDO1 disabled V_{CC} = 5.25V, 70°C		-	-	240	mA	(Driving two 75Ω outputs)
	SDO1 disabled V_{CC} = 5.0V, 25°C		-	190	-	mA	(Driving two 75Ω outputs)

PIN CONNECTIONS



NOTE: No Heat Sink Required

PIN DESCRIPTIONS

NUMBER	SYMBOL	LEVEL	TYPE	DESCRIPTION
1, 95	V_{EE3}	Power	Input	**Negative Supply.** Most negative power supply connection, for input stage.
2	PCLK_IN	TTL	Input	**Parallel Data Clock**. 74.25 or 74.25/1.001MHz
3, 4, 5, 6, 7, 8, 9, 11, 12, 14, 19, 20, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43,46, 50, 51, 52, 56, 60, 61, 62, 65, 66, 67, 68, 69, 70, 71, 72, 73, 80, 81, 83, 93, 97, 98, 99, 100, 101, 102, 108, 109, 116, 117, 120, 121	NC			**No Connect**. These pins are not used internally. These pins should be floating.
10	BUF_V_{EE}	Power	TEST	**Negative Supply/Test Pin**. Most negative power supply connection. For buffer for oscillator/divider for test purposes only. Leave floating for normal operation.
13	XDIV20	TTL	TEST	**Test Pin**. Test block output. Leave floating for normal operation.
15	PLL_LOCK	TTL	Output	**Status Signal Output**. Indicates when the GS1522 is phase locked to the incoming PCLK_IN clock signal. LOGIC HIGH indicates PLL is in Lock. LOGIC LOW indicates PLL is out of Lock.
16	BYPASS	TTL	Input	**Control Signal Input**. Used to bypass the scrambling function if data is already scrambled by GS1501 or if non-SMPTE encoded data stream such as 8b/10b is to be transmitted. When BYPASS is LOW, the SMPTE scrambler and NRZ(I) encoder are enabled. When BYPASS is HIGH, the SMPTE scrambler and NRZ(I) encoder are bypassed.
17	RESET	TTL	Input	**Control Signal Input**. Used to reset the SMPTE scrambler. For logic HIGH; Resets the SMPTE scrambler and NRZ(I) encoder. For logic LOW: normal SMPTE scrambler and NRZ(I) encoder operation.
18, 26, 27, 28, 29, 30, 59	V_{EE2}	Power	Input	**Negative Supply**. Most negative power supply connection. For Cable Driver outputs and all other digital circuitry excluding input stage and PLL stage.
21, 22, 23, 24, 25, 45, 57	V_{CC2}	Power	Input	**Positive Supply**. Most positive power supply connection. For Cable Driver outputs and all other digital circuitry excluding input stage and PLL stage.
31	SDO1_EN	Power	Input	**Control Signal Input**. Used to enable or disable the second serial data output stage. This signal must be tied to GND to enable this stage. Do not connect to a logic LOW.
44	R_{SET1}		Input	**Control Signal Input**. External resistor is used to set the data output amplitude for SDO1 and $\overline{SDO1}$. Use a ±1% resistor.
47, 49	$\overline{SDO1}$, SDO1	Analog	Output	**Serial Data Output Signal**. Current mode serial data output #1. Use 75Ω ±1% pull up resistors to V_{CC2}.
48, 54	SDO_NC			**No Connect**. Not used internally. This pin must be left floating.
53, 55	$\overline{SDO0}$, SDO0	Analog	Output	**Serial Data Output Signal**. Current mode serial data output #0. Use 75Ω ± 1% pull up resistors to V_{CC2}.
58	R_{SET0}	Analog	Input	**Control Signal Input**. External resistor is used to set the data output amplitude for SDO0 and $\overline{SDO0}$. Use a ±1% resistor.

PIN DESCRIPTIONS (Continued)

NUMBER	SYMBOL	LEVEL	TYPE	DESCRIPTION
63	A0	TTL	TEST	**Test Signal**. Used for manufacturing test purposes only. This pin must be tied low for normal operation.
64	OSC_V_{EE}	Power	Input	**Negative Supply**. Ground for ring oscillator. This pin must be floating for normal operation.
74	$\overline{VCO}$	Analog	Input	**Control Signal Input**. Input pin is AC coupled to ground using a 50Ω transmission line.
75	VCO	Analog	Input	**Control Signal Input**. Voltage controlled oscillator input. This pin is connected to the output pin of the GO1515 VCO. This pin must be connected to the GO1515 VCO output pin via a 50Ω transmission line.
76	PD_V_{EE}	Power	Input	**Negative Supply**. Most negative power supply connection. For phase detector stage.
77	PDSUB_V_{EE}	Power	Input	**Guard Ring**. Ground guard ring connection to isolate phase detector in PLL stage.
78	IJI	Analog	Output	**Status Signal Output**. Indicates the amount of excessive jitter on the incoming SDI and $\overline{SDI}$ input.
79	PD_V_{CC}	Power	Input	**Positive Supply**. Most positive power supply connection. For phase detector stage.
82, 84	LFS, $\overline{LFS}$	Analog	Input	**Loop Filter Connections**.
85, 87	PLCAP, $\overline{PLCAP}$	Analog	Input	**Control Signal Input**. Phase lock detect time constant capacitor.
86	DM			**Test Signal**. Used for manufacturing test only. This pin must be left floating in normal operation.
88	DFT_V_{EE}	Power	Input	**Most Negative Power Supply Connection** . Enables the jitter demodulator functionality. This pin should be connected to ground. If left floating, the DM function is disabled resulting in a current saving of 340µA.
89	LFA_V_{EE}	Power	Input	**Negative Supply**. Most negative power supply connection. For loop filter stage.
90	LFA	Analog	Output	**Control Signal Output**. Control voltage for GO1515 VCO.
91	LBCONT	Analog	Input	**Control Signal Input**. Used to provide electronic control of Loop Bandwidth.
92	LFA_V_{CC}	Power	Input	**Positive Supply**. Most positive power supply connection. For loop filter stage.
94	V_{CC3}	Power	Input	**Positive Supply**. Most positive power supply connection. For input stage.
96	SYNC_DETECT_DISABLE	TTL	Input	**Control Signal Input**. Used to disable the sync detection function. Logic HIGH disables sync detection. Logic LOW: 000-003 is mapped into 000 and 3FC-3FF is mapped into 3FF for 8-bit operation.
103, 104, 105, 106, 107, 110, 111, 112, 113, 114, 115, 118, 119, 122, 123, 124, 125, 126, 127, 128	DATA_IN[19:0]	TTL	Input	**Input Data Bus**. The device receives a 20 bits data stream running at 74.25 or 74.25/1.001 MHz from the GS1501 HDTV Formatter or GS1511 HDTV Formatter. Input data can be in SMPTE292M scrambled or unscrambled format. DATA_IN[19] is the MSB (pin 103). DATA_IN[0] is the LSB (pin 128).

INPUT/OUTPUT CIRCUITS

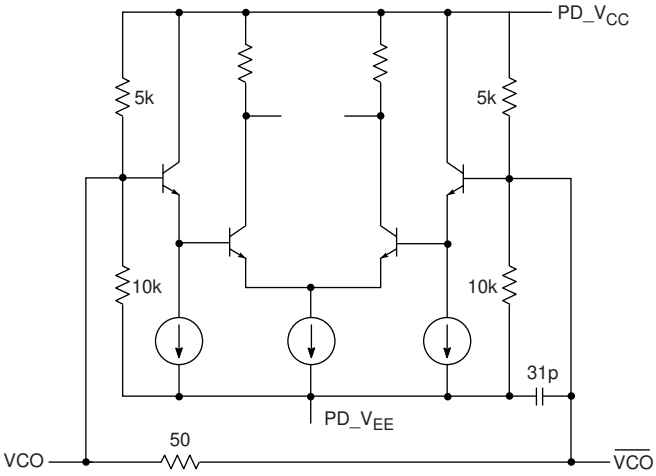


Fig. 1 VCO/$\overline{\text{VCO}}$ Input Circuit

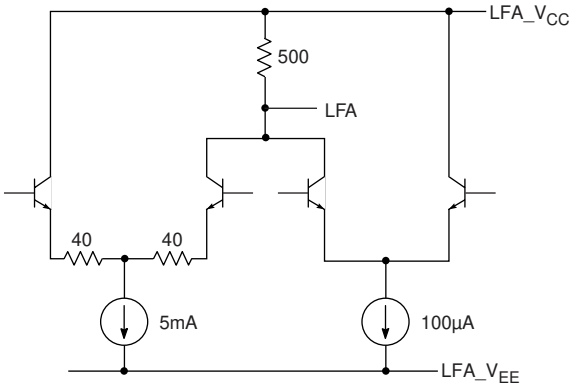


Fig. 4 LFA Circuit

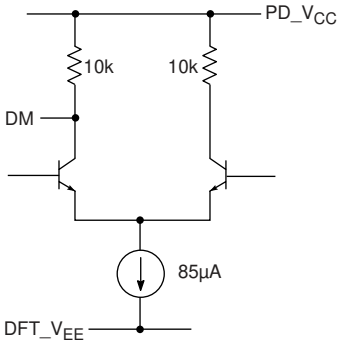


Fig. 2 DM Output Circuit

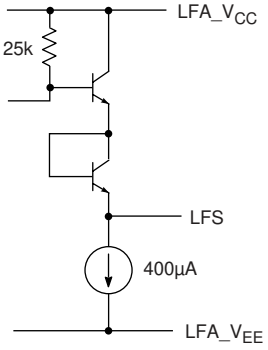


Fig. 5 LFS Output Circuit

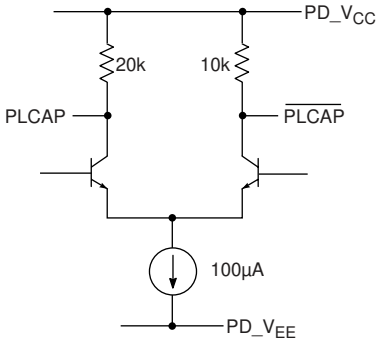


Fig. 3 PLCAP/$\overline{\text{PLCAP}}$ Output Circuit

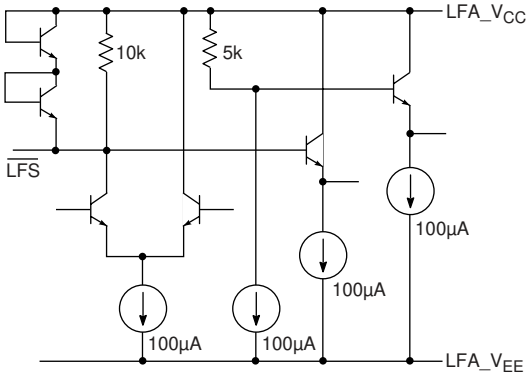
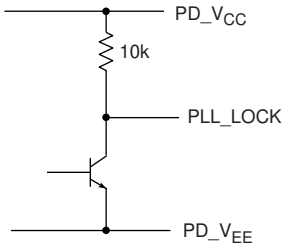


Fig. 6 $\overline{\text{LFS}}$ Input Circuit



All on-chip resistors have ±20% tolerance at room temperature.

Fig. 7 PLL_LOCK Output Circuit

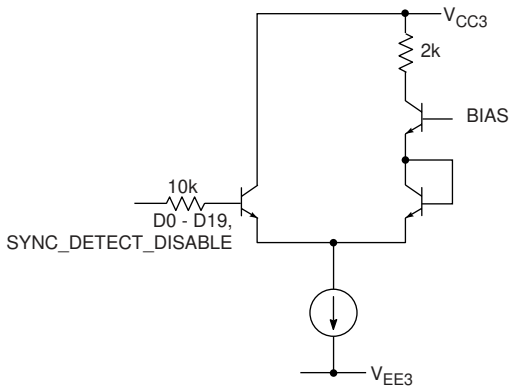


Fig. 10 Data Input and SYNC_DETECT_DISABLE Circuit

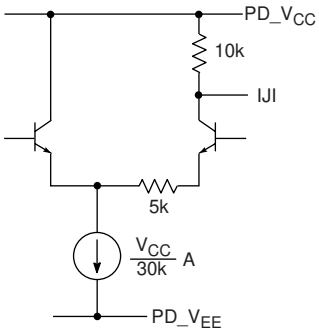


Fig. 8 IJI Output Circuit

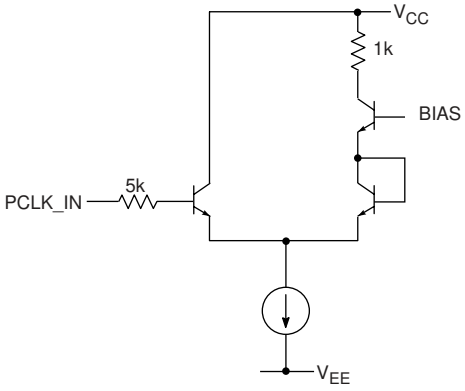


Fig. 11 PCLK_IN Circuit

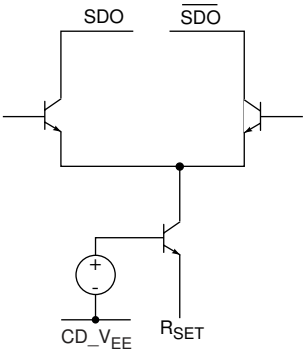


Fig. 9 SDO/$\overline{\text{SDO}}$ Output Circuit

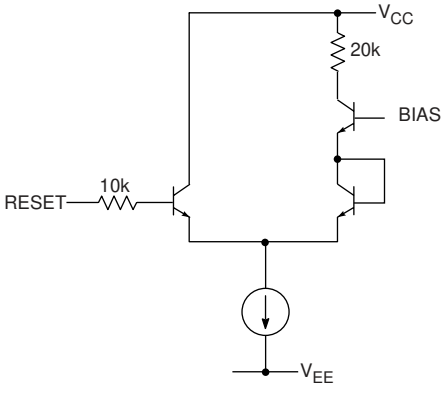


Fig. 12 RESET Circuit

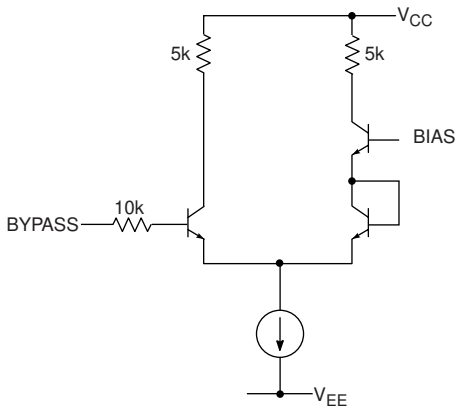


Fig. 13 BYPASS Circuit

DETAILED DESCRIPTION

The GS1522 HDTV Serializer is a bipolar integrated circuit used to convert parallel data into serial format according to the SMPTE 292M standard. The device encodes both 8-bit and 10-bit TTL compatible parallel signals producing a serial data rate of 1.485Gb/s. The device operates from a single 5V supply and is available in a 128 pin MQFP package.

The functional blocks within the device include the input latches, interleaver, sync detector, parallel to serial converter, SMPTE scrambler, NRZ to NRZ(I) converter, two internal cable drivers, PLL for 20x parallel clock multiplication and lock detect circuitry.

1. INPUT LATCHES

The 20-bit input latch accepts either 3.3V or 5V CMOS/TTL inputs. The input data is buffered and then latched on the rising edge of the PCLK_IN pin (2). The output of the latch is a differential signal for increased noise immunity. Further noise isolation is provided by the use of separate power supplies.

2. INTERLEAVER

The interleaver takes the 20-bit wide parallel data (Y and C) and reduces it internally to a 10-bit wide word by alternating the Y and C data words according to SMPTE 292M, section 6.1.

3. SYNC DETECTOR

The sync detector looks for the reserved words 000-003 and 3FC-3FF in 10-bit hexadecimal, or 00-03 and FC-FF in 8-bit hexadecimal used in the TRS-ID sync word. When there is an occurrence of all zeros or all ones in the eight higher order bits, the lower two bits are forced to zeros or ones respectively. This allows the system to be compatible with 8-bit and 10-bit data. For non-SMPTE standard parallel data, a logic input Sync Detect Disable pin (96) is available to disable this feature.

4. SCRAMBLER

The scrambler is a linear feedback shift register used to pseudo-randomize the incoming data according to the fixed polynomial (X^9+X^4+1). This minimizes the DC component in the output serial stream. The NRZ to NRZ(I) converter uses another polynomial (X+1) to convert a long sequence of ones to a series of transitions, minimizing polarity effects. To disable these features, set the BYPASS pin (16) HIGH.

5. SLEW PHASE LOCK LOOP (S-PLL)

An innovative feature of the GS1522 is the slew phase lock loop (S-PLL). When a step phase change is applied to the PLL, the output phase gains constant rate of change with respect to time. This behavior is termed slew. Figure 14 shows an example of input and output phase variation over time for slew and linear (conventional) PLLs. Since the slewing is a non-linear behavior, the small signal analysis cannot be done in the same way as it is for the standard PLL. However, it is still possible to plot input jitter transfer characteristics at a constant input jitter modulation.

Slew PLLs offer several advantages such as excellent noise immunity. The loop corrects small input jitter modulation immediately because of the infinite bandwidth. Therefore, the small signal noise of the VCO is cancelled immediately. The GS1522 uses a very clean, external VCO called the GO1515 *(refer to the GO1515 Data Sheet for details)*.

Another advantage is the bi-level digital phase detector which provides constant loop bandwidth that is predominantly independent of the data transition density. The loop bandwidth of a conventional tri-stable charge

pump drops with reducing data transitions. During pathological signals, the data transition density reduces from 0.5 to 0.05 but the slew PLL's performance does not change significantly.

Because most of the PLL circuitry is digital, it is very robust as digital systems are generally more robust than their analog counterparts. Signals which represent the internal functionality, like DM (86), can be generated without adding additional artifacts. Thus, system debugging is possible with these features.

The complete slew PLL is made up of several blocks including the phase detector, the charge pump and an external Voltage Controlled Oscillator (VCO) which are described in the following sections. Phase lock loop frequency synthesis and lock logic are also described.

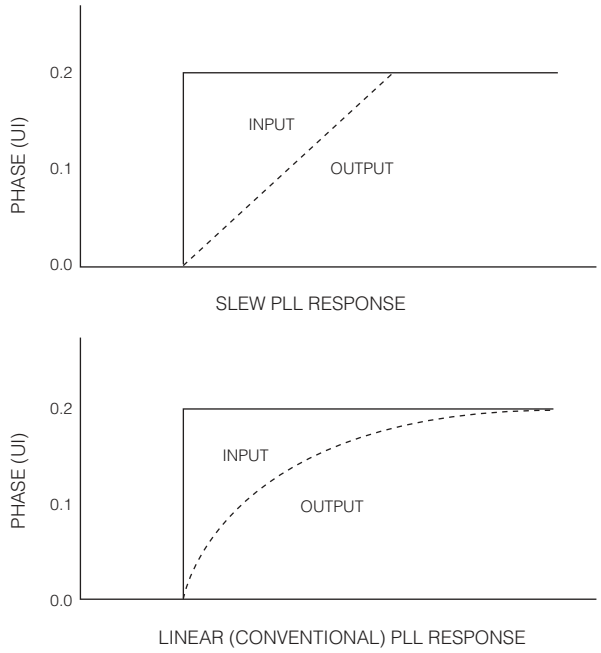


Fig. 14 PLL Characteristics

5.1. Phase Detector

The phase detector portion of the slew PLL used in the GS1522 is a bi-level digital phase detector. It indicates whether the data transition occurred before or after with respect to the falling edge of the internal clock. When the phase detector is locked, the data transition edges are aligned to the falling edge of the clock. The input data is then sampled by the rising edge of the clock, as shown in Figure 15. In this manner, the allowed input jitter is 1UI p-p in an ideal situation. However, due to setup and hold time, the GS1522 typically achieves 0.8UI p-p input jitter tolerance without causing any errors in this block. When the signal is locked to the internal clock, the control output from the phase detector is refreshed at the transition of each rising edge of the data input. During this time, the phase of the clock drifts in one direction.

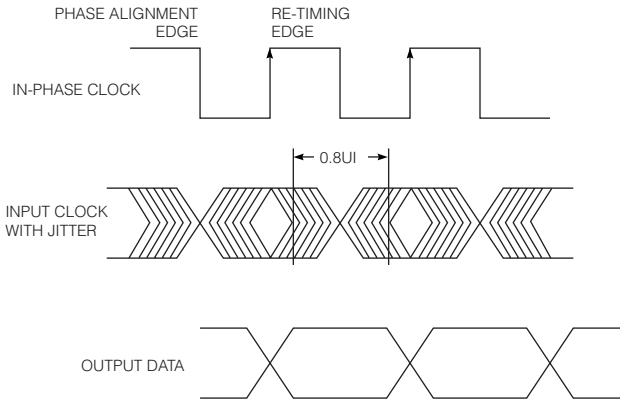


Fig. 15 Phase Detector Characteristics

During pathological signals, the amount of jitter that the phase detector will add can be calculated. By choosing the proper loop bandwidth, the amount of phase detector induced jitter can also be limited. Typically, for a 1.41MHz loop bandwidth at 0.2UI input jitter modulation, the phase detector induced jitter is about 0.015UIp-p. This is not significant, even in the presence of pathological signals.

5.2. Charge Pump

The charge pump in a slew PLL is different from the charge pump in a linear PLL. There are two main functions of the charge pump: to hold the frequency information of the input data and to provide a binary control voltage to the VCO.

The charge pump holds the frequency information of the input data. This information is held by C_{CP1} which is connected between LFS (82) and $\overline{LFS}$ (84). C_{CP2}, which is connected between $\overline{LFS}$ and LFA_V_{EE} (89), is used to remove common mode noise. Both C_{CP1} and C_{CP2} should have the same value.

The charge pump provides a binary control voltage to the VCO depending upon the phase detector output. The output pin LFA (90) controls the VCO. Internally there is a 500Ω pull-up resistor which is driven with a 100µA current called I_P. Another analog current I_F, with 5mA maximum drive proportional to the voltage across the C_{CP1}, is applied at the same node. The voltage at the LFA node is V_{LFA_VCC} - 500(I_P+I_F) at any time.

Because of the integrator, I_F changes very slowly whereas I_P can change at the positive edge of the data transition as often as a clock period. In the locked position, the average voltage at LFA (V_{LFA_VCC} – 500(I_P/2+I_F) is such that VCO generates frequency f equal to the data rate clock frequency. Since I_P is changing all the time between 0A and 100µA, there are two levels generated at the LFA output.

5.3. VCO

The GO1515 is an external hybrid VCO which has a centre frequency of 1.485GHz. It is guaranteed to provide 1.485/1.001GHz within the control voltage (3.1V – 4.65V) of the GS1522 over process, power supply and temperature.

The GO1515 is a very clean frequency source and, because of the internal high Q resonator, is an order of magnitude more immune to external noise as compared to on-chip VCOs.

The VCO gain, Kf, is nominally 16MHz/V. The control voltage around the average LFA voltage is 500 x I_P/2. This produces two frequencies off from the centre by f = Kf x 500 x I_P/2.

5.4. Phase Lock Loop Frequency Synthesis

The GS1522 requires the HDTV parallel clock (74.25 or 74.25/1.001MHz) to synthesize a serial clock which is 20 times the parallel clock frequency (1.485MHz) using a phase locked loop (PLL). This serial clock is then used to strobe the output serial data. Figure 16 illustrates this operation. The VCO is normally free-running at a frequency close to the serial data rate. A divide-by-20 circuit converts the free running serial clock frequency to approximately that of the parallel clock. Within the phase detector, the divided-by-20 serial clock is then compared to the reference parallel clock from the PCLK_IN pin (2). Based on the leading or lagging alignment of the divided clock to the input reference clock, the serial data output is synchronized to the incoming parallel clock.

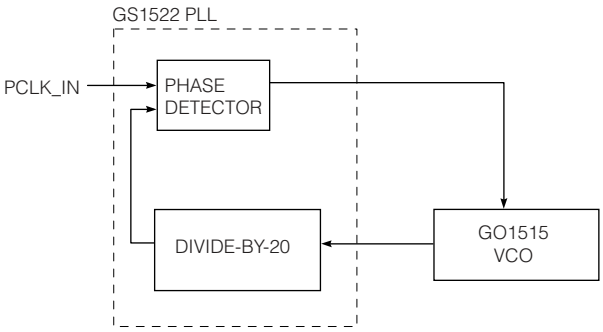


Fig. 16 Phase Lock Loop Frequency Synthesis

5.5. Lock Logic

Logic is used to produce the PLL_LOCK (15) signal which is based on the LFS signal and phase lock signal. When there is no data input, the integrator charges and eventually saturates at either end. By sensing the saturation of the integrator, it is determined that no data is present. If there is no data present or phase lock is low, the lock signal is made LOW. Logic signals are used to acquire the frequency by sweeping the integrator. Injecting a current into the summing node of the integrator achieves the sweep. The sweep is disabled when phase lock is asserted. The direction of the sweep is changed when LFS saturates at either end.

6. LBCONT

The LBCONT pin (91) is used to adjust the loop bandwidth by externally changing the internal charge pump current. For maximum loop bandwidth, connect LBCONT to the most positive power supply. For medium loop bandwidth, connect LBCONT through a pull-up resistor ($R_{PULL-UP}$). For low loop bandwidth, leave LBCONT floating. The formula below shows the change in the loop bandwidth using $R_{PULL-UP}$.

$$LBW = LBW_{NOMINAL} \times \frac{(25k\Omega + R_{PULL-UP})}{(5k\Omega + R_{PULL-UP})}$$

where $LBW_{NOMINAL}$ is the loop bandwidth when LBCONT is left floating.

7. LOOP BANDWIDTH OPTIMIZATION

Since the feed back loop has only digital circuits, the small signal analysis does not apply to the system. The effective loop bandwidth scales with the amount of input jitter modulation index. The following table summarizes the relationship between input jitter modulation index and bandwidth when R_{CP1} and C_{CP3} are not used. *See the Typical Application Circuit for the location of R_{CP1} and C_{CP3}.*

TABLE 1: Relationship Between Input Jitter Modulation Index and Bandwidth

INPUT JITTER MODULATION INDEX	BANDWIDTH	BW JITTER FACTOR (jitter modulation x BW)
0.05	5.657MHz	282.9kHzUI
0.10	2.828MHz	282.9kHzUI
0.20	1.414MHz	282.9kHzUI
0.50	565.7kHz	282.9kHzUI

The product of the input jitter modulation (IJM) and the bandwidth (BW) is a constant. In this case, it is 282.9kHzUI. The loop bandwidth automatically reduces with increasing input jitter, which results in the cleanest signal possible.

Using a series combination of R_{CP1} and C_{CP3} in parallel to an on-chip resistor (*see the Typical Application Circuit*) can reduce the loop bandwidth of the GS1522. The parallel combination of the resistors is directly proportional to the bandwidth factor. For example, the on-chip 500Ω resistor yields 282.9kHzUI. If a 50Ω resistor is connected in parallel, the effective resistance will be (50:500) 45.45Ω. This resistance yields a bandwidth factor of

[282.9 x (45.45/500)] = 25.72kHzUI

The capacitance C_{CP3} in series with the R_{CP1} should be chosen such that the RC factor is 50µF. For example, R_{CP1}=50Ω requires C_{CP3}=1µF.

The synchronous lock time increases with reduced bandwidth. Nominal synchronous lock time is equal to [0.25 × $\sqrt{2}$ /Bandwidth factor]. That is, the default bandwidth factor (282.9kHzUI) yields 1.25µs. For 25.72kHzUI, the synchronous lock time is 0.3535/25.72k = 13.75µs. Since the C_{CP1}, C_{CP2} and C_{CP3} are also charged, it is measured to be about 11µs which is slightly less than the calculated value of 13.75µs.

The Kf of the VCO (GO1515) is specified with a minimum of 11MHz/V and maximum of 21MHz/V which is about ±32% variation. The 500 x I_P/2 varies about ±10%. The resulting bandwidth factor varies by approximately ±45% when no R_{CP1} and C_{CP3} are used. I_P by itself may vary by 30% so the variability for lower bandwidths increases by an additional ±30%.

The C_{CP1} and C_{CP2} capacitors should be changed with reduced bandwidths. Smaller C_{CP1} and C_{CP2} capacitors result in jitter peaking, lower stability, less probability of locking but at the same time lowering the asynchronous lock time. Therefore, there is a trade-off between asynchronous lock time and jitter peaking/stability. These capacitors should be as large as possible for the allowable lock time and should be no smaller than the allowed value. With the recommended values, jitter peaking of less than 0.1dB has been measured at the lower loop bandwidth as shown in Figure 17. At higher loop bandwidths, it is difficult to measure jitter peaking because of the limitation of the measurement unit.

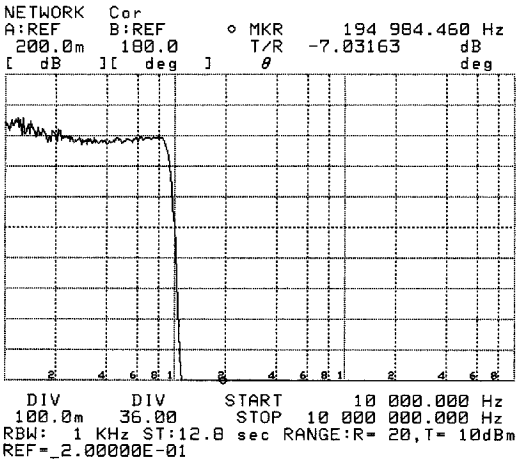


Fig. 17 Typical Jitter Peaking

However, because relatively larger C_{CP1} and C_{CP2} capacitors can be used, over-damping of the loop response occurs. An accurate jitter peaking measurement of 0.1dB for the GS1522 requires the modulation source to have a constant amount of jitter modulation index (within 0.1dB or 1.2%) over the frequency range beyond the loop bandwidth.

It has been determined that for 282.9kHzUI, the minimum value of the C_{CP1} and C_{CP2} capacitors should be no less than 0.5µF. For added margin, 1µF capacitors are recommended. The 1µF value gives a lock time of about 60ms in one attempt. For 25.72kHzUI, these capacitors should be no less than 5.6µF. This results in 340ms of lock time. If necessary, extra margin can be built by increasing these capacitors at the expense of a longer asynchronous lock time.

Bandwidths lower than 129kHz at 0.2UI modulation have not been characterized, but it is believed that the bandwidth could be further lowered (*contact Gennum's Video Products Applications for further details*). Since a lower bandwidth has less correction for noise, extra care should be taken to minimize board noise. Figures 18 and 19 show the two measured loop bandwidths at these two settings. Table 2 summarizes the two bandwidth settings.

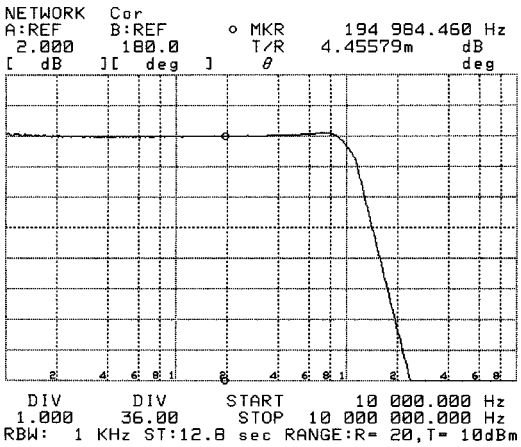


Fig. 18 Typical Jitter Transfer Curve at Setting A in Table 2

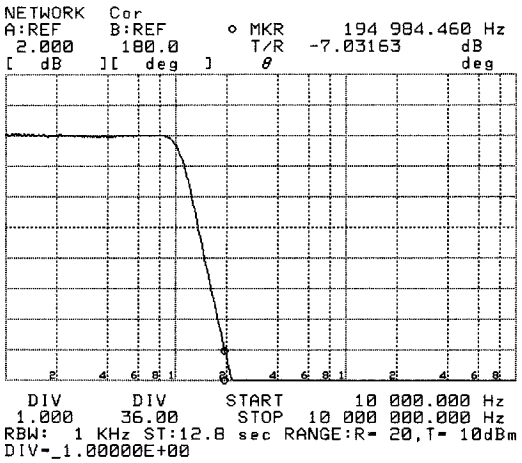


Fig. 19 Typical Jitter Transfer Curve at Setting B in Table 2

TABLE 2: Loop Bandwidth Setting Options

	RCP1	CCP3	CCP1	CCP2	BW FACTOR	BW at 0.2 UI JITTER MODULATION INDEX	ASYNCHRONOUS	SYNCHRONOUS
A	Open	Open	1.0	1.0	282.9kHz	1.41MHz	60ms	1.25µs
B	50	1.0	5.6	5.6	25.72kHz	129kHz	340ms	11.0µs

8. PHASE LOCK

The phase lock circuit is used to determine the phase locked condition. It is done by generating a quadrature clock by delaying the in-phase clock by 166ps (0.25UI at 1.5GHz) with the tolerance of 0.05UI. The in-phase clock is the clock whose falling edge is aligned to the data transition. When the PLL is locked, the falling edge of the in-phase clock is aligned with the data edges as shown in Figure 20. The quadrature clock is in a logic HIGH state in the vicinity of input data transitions. The quadrature clock is sampled and latched by positive edges of the data transitions. The generated signal is low pass filtered with an RC network. The R is an on-chip 6.67kΩ resistor and C_{PL} is an internal capacitor (31pF). The time constant is about 200ns.

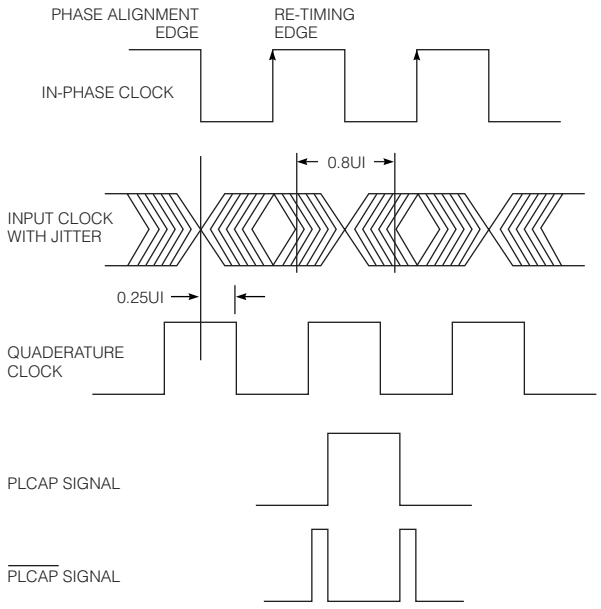


Fig. 20 PLL Circuit Principles

If the signal is not locked, the data transition phase could be anywhere with respect to the internal clock or the quadrature clock. In this case, the normalized filtered sample of the quadrature clock is 0.5. When VCO is locked to the incoming data, data will only sample the quadrature clock when it is logic HIGH. The normalized filtered sample quadrature clock is 1.0. We chose a threshold of 0.66 to generate the phase lock signal. Because the threshold is lower than 1, it allows jitter to be greater than 0.5UI before the phase lock circuit reads it as “not phase locked”.

9. INPUT JITTER INDICATOR (IJI)

This signal indicates the amount of excessive jitter which occurs beyond the quadrature clock window (greater than 0.5UI, *see Figure 19*). All the input data transitions occurring outside the quadrature clock window are captured and filtered by the low pass filter as mentioned in section 8, Phase Lock. The running time average of the ratio of the transitions inside the quadrature clock and outside the quadrature is available at the PLCAP/$\overline{\text{PLCAP}}$ pins (87 and 85). IJI, which is the buffered signal available at the PLCAP, is provided so that loading does not effect the filter circuit. The signal at IJI is referenced with the power supply such that the factor V_{IJI}/V_{CC} is a constant over process and power supply for a given input jitter modulation. The IJI signal has 10kΩ output impedance. Figure 21 shows the relationship of the IJI signal with respect to the sine wave modulated input jitter.

TABLE 3: IJI Voltage as a Function of Sinusoidal Jitter

P-P SINE WAVE JITTER IN UI	IJI VOLTAGE
0.00	4.75
0.15	4.75
0.30	4.75
0.39	4.70
0.45	4.60
0.48	4.50
0.52	4.40
0.55	4.30
0.58	4.20
0.60	4.10
0.63	3.95

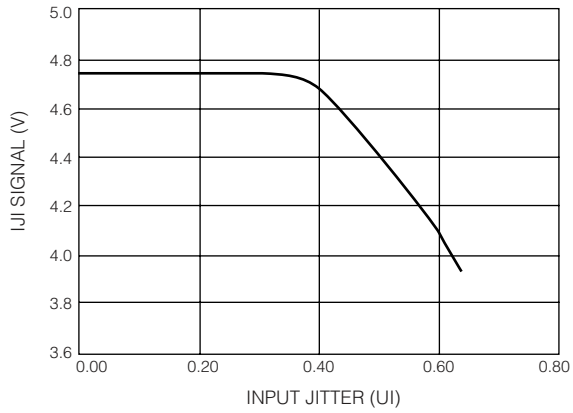


Fig. 21 Input Jitter Indicator (Typical at T_A = 25°C)

10. JITTER DEMODULATION (DM)

The differential jitter demodulation (DM) signal is available at the DM pin (86). This signal is the phase correction signal of the PLL loop, which is amplified and buffered. If the input jitter is modulated, the PLL tracks the jitter if it is within loop bandwidth. To track the input jitter, the VCO has to be adjusted by the phase detector via the charge pump. Thus, the signal which controls the VCO contains the information of the input jitter modulation. The jitter demodulation signal is only valid if the input jitter is less than 0.5UIp-p. The DM signal has a 10kΩ output impedance, which can be low pass filtered with appropriate capacitors to eliminate high frequency noise. DFT_V_{EE} (88) should be connected to GND to activate the DM signal.

The DM signal can be used as a diagnostic tool. Assume there is an HDTV SDI source which contains excessive noise during the horizontal blanking because of the transient current flowing in the power supply. To discover the source of the noise, probe around the source board with a low frequency oscilloscope (Bandwidth < 20MHz) that is triggered with an appropriately filtered DM signal. The true cause of the modulation is synchronous and appears as a stationary signal with respect to the DM signal.

Figure 22 shows an example of such a situation. An HDTV SDI signal is modulated with a signal causing about 0.2UI jitter (Channel 1). The GS1522 receives this signal and locks to it. Figure 22 (Channel 2) shows the DM signal. Notice the wave shape of the DM signal, which is synchronous to the modulating signal. The DM signal can also be used to compare the output jitter of the HDTV signal source.

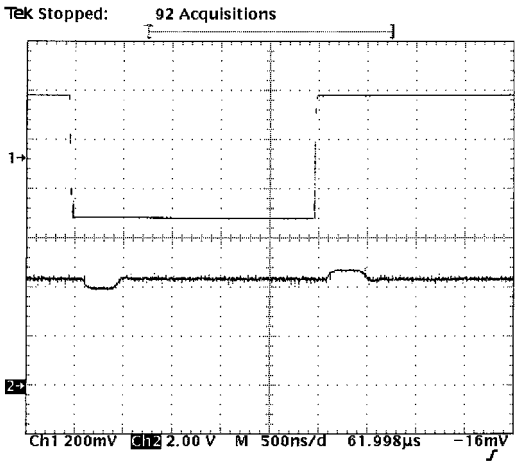


Fig. 22 Jitter Demodulation Signal

11. MUTE

The logic controls the mute block when the PLL_LOCK (15) signal has a LOW logic state. When the mute signal is asserted, the previous state of the output is latched.

12. CABLE DRIVER

The outputs of the GS1522 are complementary current mode cable driver stages. The output swing and impedance can be varied. Use Table 4 to select the R_{SET} resistor for the desired output voltage level. Linear interpolation can be used to determine the specific value of the resistor for a given output swing at the load impedance. For linear interpolation, use either Figure 23 or the information in Table 4. Find the admittance and then, by inverting the admittance, a resistor value for the R_{SET} can be found.

The output can be used as dual 0.8V 75Ω cable drivers. It can also be used as a differential transmission line driver. In this case, the pull-up resistor should match the impedance of the transmission line because the pull-up resistor acts as the source impedance. To reduce the swing and save power, use a higher value of R_{SET} resistor. There are HD-LINX™ products that can handle such low input swings.

NOTE: For reliability, the minimum R_{SET} resistor cannot be less than 50Ω because of higher current density.

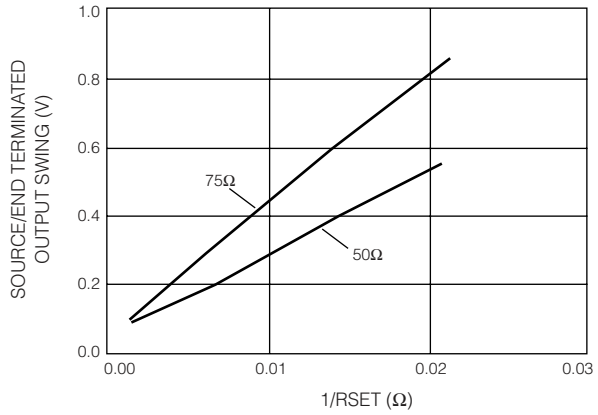


Fig. 23 Signal Swing for Various R_{SET} Admittances

When the outputs are used to differentially drive another device such as the GS1508, use 50Ω transmission lines with the smallest possible signal swing while allowing 10% variation at the output swing to select the correct R_{SET} resistor. To drive the GS1508, the recommended R_{SET} resistor is 150Ω. There is no need to compensate for the return-loss in this situation. The uncompensated waveform at the output is shown in Figure 24.

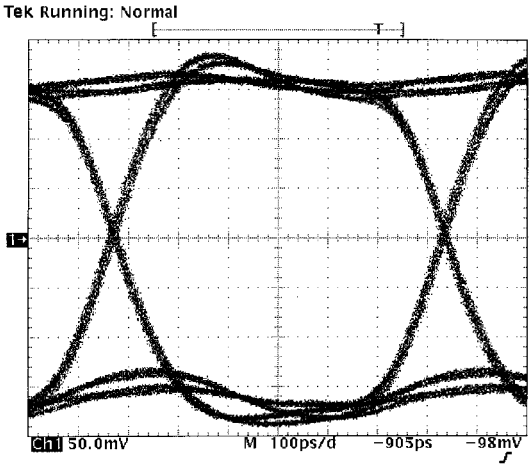


Fig. 24 Uncompensated Output Eye Waveform

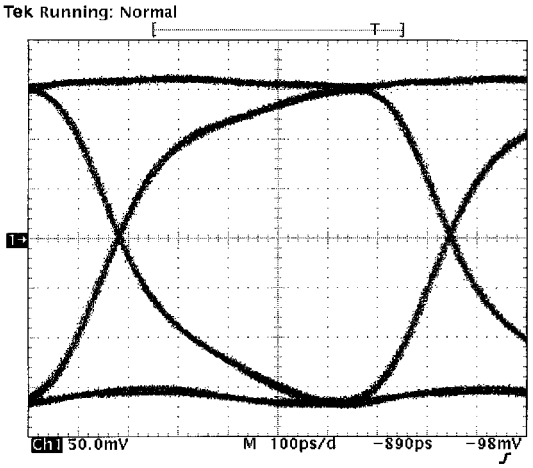


Fig. 25 Compensated Output Eye Waveform

NOTE: Figures 24 and 25 show the waveforms on an oscilloscope using a 75Ω to 50Ω pad.

TABLE 4: R_{SET} Values for Various Output Load Conditions

R_{SET} RESISTOR	ADMITTANCE (g) OF THE R_{SET} RESISTOR (= 1/R_{SET} RESISTOR)	OUTPUT CURRENT	TRANSMISSION LINE, TERMINATED AT THE END. (PULL-UP RESISTOR AT THE SOURCE = 75Ω)	TRANSMISSION LINE, TERMINATED AT THE END. (PULL-UP RESISTOR AT THE SOURCE = 50Ω)
500.0Ω	0.0020	2.506mA	0.094V	0.063V
150.0Ω	0.0067	7.896mA	0.296V	0.197V
75.0Ω	0.0133	15.161mA	0.569V	0.379V
53.6Ω	0.0187	20.702mA	0.776V	0.517V
52.3Ω	0.0192	21.216mA	0.796V	0.530V
49.9Ω	0.0200	22.032mA	0.826V	-

12. RETURN LOSS

In an application where the GS1522 directly drives a cable, it is possible to achieve an output return loss (ORL) of about 17dB to 1.485GHz. PCB layout is very important. Use the EB1522 as a reference layout (*see Figures 28 to 31*). When designing high frequency circuits, use very small '0608' surface mount components with short distances between the components. To reduce PCB parasitic capacitance, provide openings in the ground plane. For best matching, a 12nH inductor in parallel with a 75Ω resistor and a 1.5pF capacitor matches the 75Ω cable impedance. The inductor and resistor cancel the parasitic capacitance while the capacitor cancels the inductive effect of the bond wire. To verify the performance of any layout, measure the return loss by shorting the inductor with a piece of wire without the GS1522 installed.

Unless the artwork is an exact copy of the recommended layout, verify every design for output return loss. Tweak the layout until a return loss of 25dB is attained while the GS1522 is not mounted and L1 is shorted. When the device is mounted, use different inductors to match the parasitic capacitance of the IC. When the correct inductor is used, maximum return loss of 5MHz to 800MHz is achievable. To increase the return loss 800MHz to 1.5GHz, use a shunt capacitor of 0.5pF to 1.5pF. The larger inductor causes slower rise/fall time. The larger shunt capacitor causes a kink in the output waveform. Therefore, the waveform must be verified to meet SMPTE 292M specifications.

There are two levels at the output depending upon the output state (logic HIGH or LOW). When taking measurements, latch the outputs in both states. An interpolation is necessary because the actual output node voltages are different when a stream of data is passing as compared to the static situation created when measuring return loss. *See the GS1508 Preliminary Data Sheet for more information.*

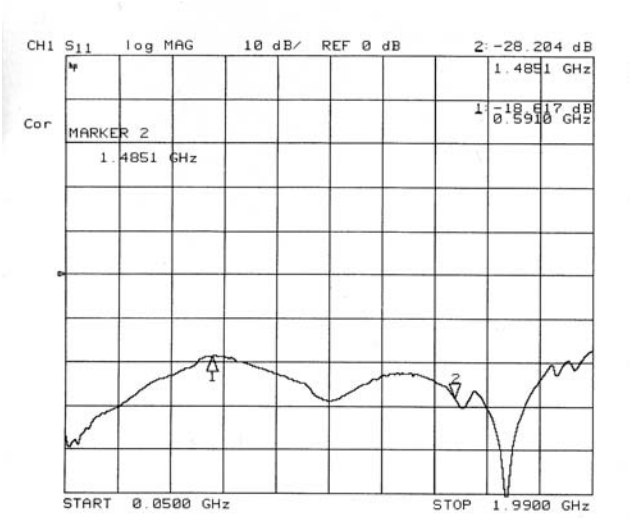


Fig. 26 Compensated Output Return Loss at Logic HIGH

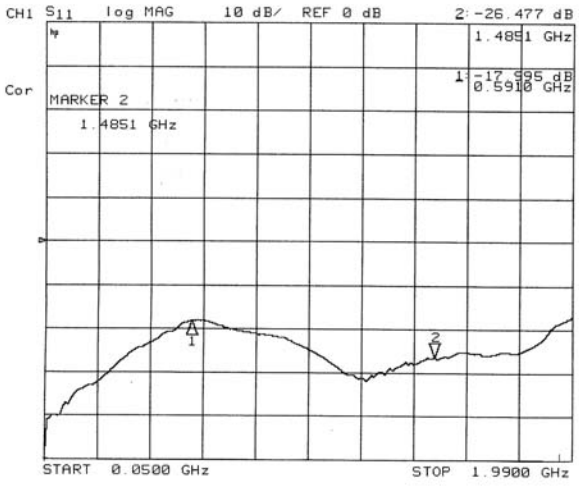
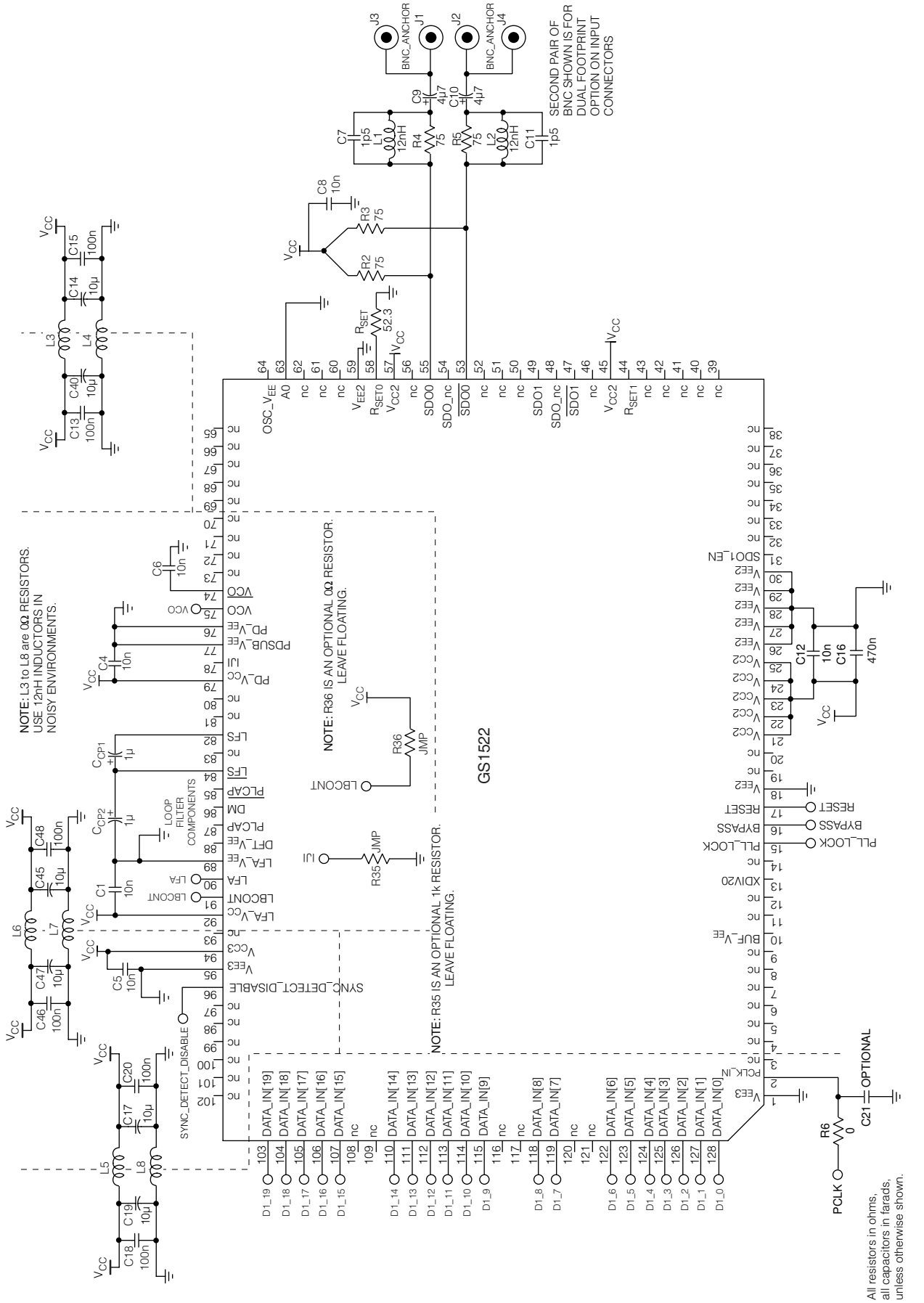


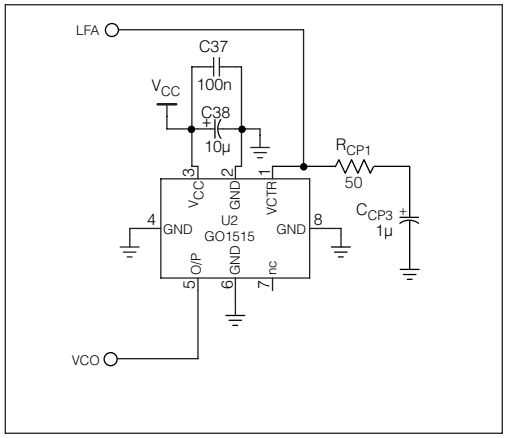
Fig. 27 Compensated Output Return Loss at Logic LOW

TYPICAL APPLICATION CIRCUIT

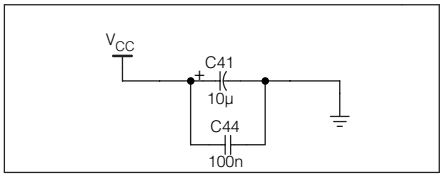


TYPICAL APPLICATION CIRCUIT (continued)

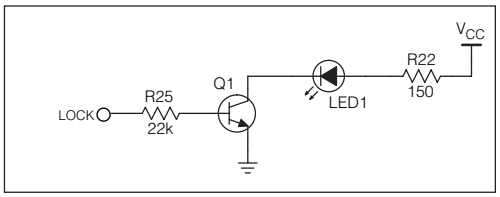
GO1515 VCO



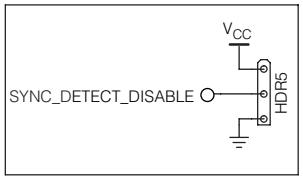
POWER CONNECT



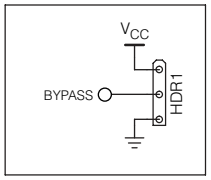
GS1522 LOCK DETECT



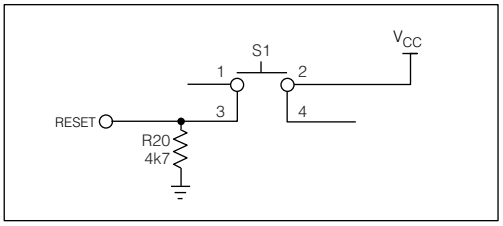
GS1522 SYNC DETECT DISABLE (10BIT/8BIT)



GS1522 SCRAMBLER BYPASS



GS1522 RESET CIRCUIT



All resistors in ohms,
all capacitors in farads,
unless otherwise shown.

The figures above show the recommended application circuit for the GS1522. The external VCO is the GO1515 and is specifically designed to be used with the GS1522. Figures 28 through 31 show an example PC board layout of the GS1522 IC and the GO1515 VCO. This application board layout does not reflect every detail of the typical application circuit. It is provided as a general guide to the location of the critical parts.

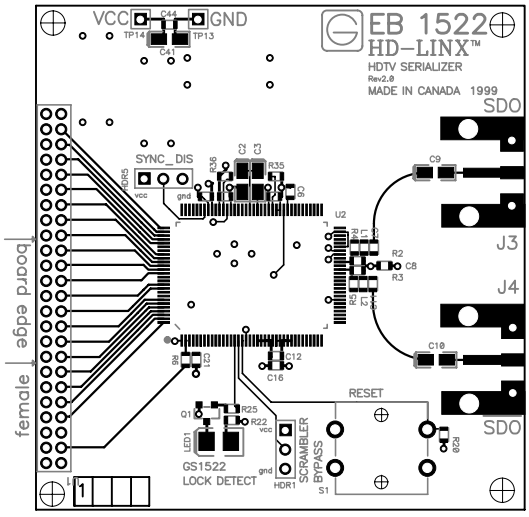


Fig. 28 Top Layer of EB1522 PCB Layout

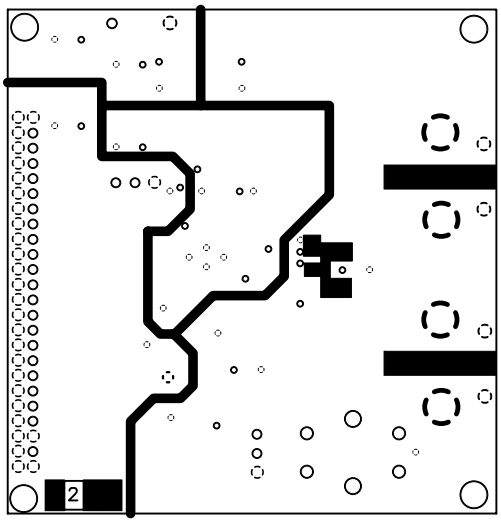


Fig. 29 Ground Layer of EB1522 PCB Layout

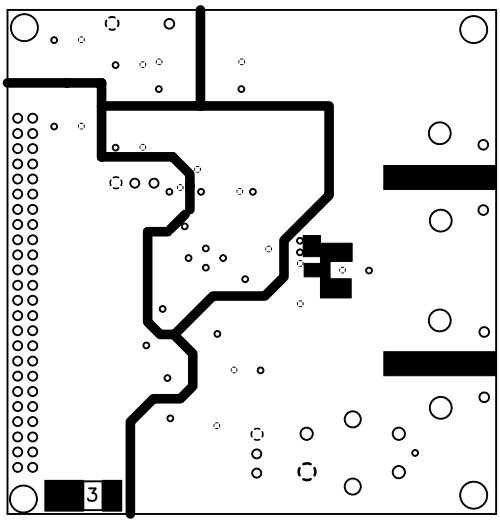


Fig. 30 Power Layer of EB1522 PCB Layout

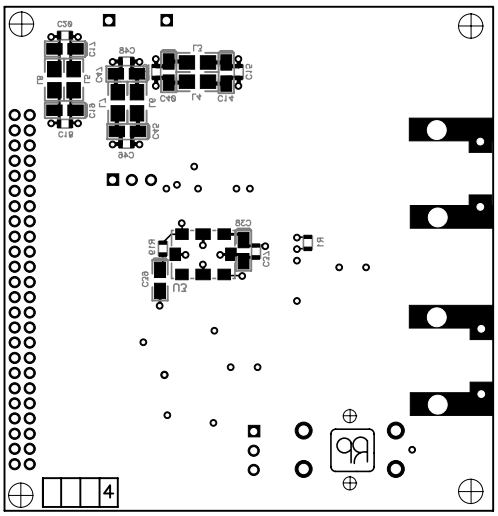
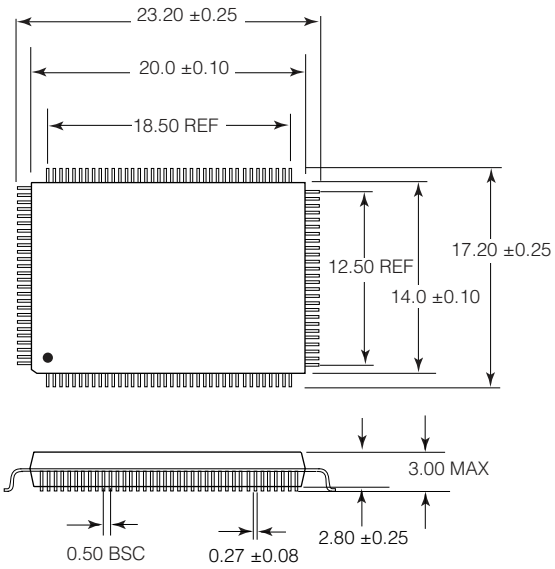


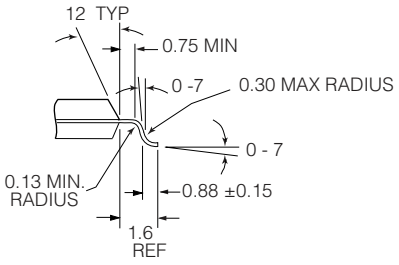
Fig. 31 Bottom Layer of EB1522 PCB Layout

APPLICATION INFORMATION

Please refer to the EBHDTX documentation for more detailed application and circuit information on using the GS1522 with the GS1501 and GS1511 Formatters.

PACKAGE DIMENSIONS





128 pin MQFP
All dimensions are in millimetres.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:
Added Pb-free and green information.
For latest product information, visit www.gennum.com

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