MPQ2124

6V, 3A, Frequency-Programmable Synchronous Buck Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2124 is a frequency-programmable (300kHz to 2.2MHz), synchronous step-down converter. It can achieve up to 3A of continuous output current using peak current control, with excellent transient response and efficiency performance. The MPQ2124 operates from a 2.7V to 6.0V input range, and generates an output voltage as low as 0.606V. It is ideal for a wide range of applications, including automotive infotainment, clusters, and telematics, as well as portable instruments.

The MPQ2124 integrates a 35mΩ high-side switch and a 25mΩ synchronous rectifier for high efficiency without an external Schottky diode. The MPQ2124 can be configured for either advanced asynchronous mode (AAM) or forced continuous conduction mode (FCCM) operation at light load. AAM provides high efficiency by reducing switching losses at light load, while FCCM has controllable frequency and a lower output ripple.

The MPQ2124 offers standard features, including soft start, an external sync clock, enable control, and a power good indicator. In addition, the MPQ2124 provides over-current protection with valley current detection, which is used to avoid current runaway. It also has short-circuit protection, reliable over-voltage protection, and auto-recovery thermal protection.

With internal compensation, the MPQ2124 requires a minimal number of readily available, standard external components, and is available in a QFN-11 (2mmx3mm) package.

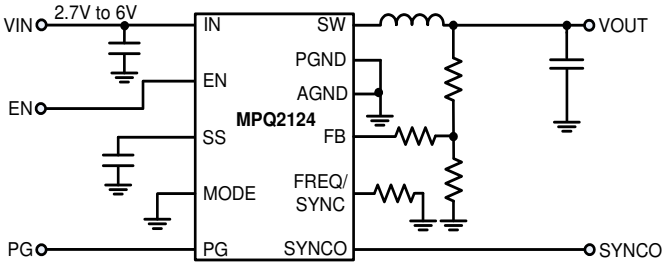
FEATURES

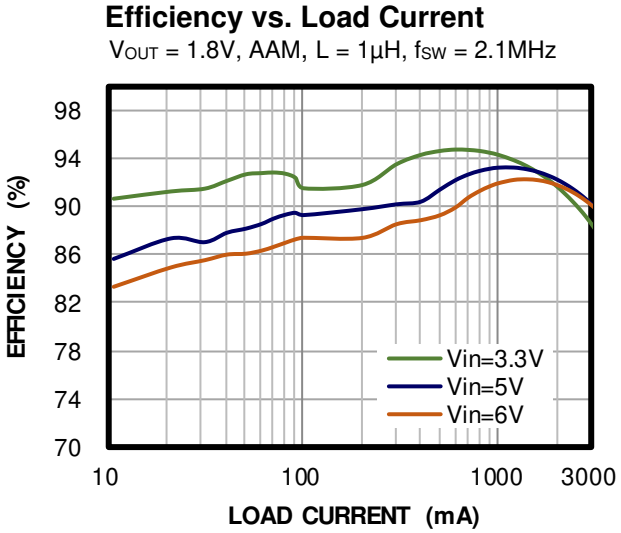
- 2.7V to 6.0V Operating Input Voltage Range
- Adjustable Output from 0.606V
- Up to 3A Continuous Output Current
- High-Efficiency Synchronous Mode Control
- 35mΩ and 25mΩ Internal Power MOSFET
- Programmable Frequency Up to 2.2MHz
- External Sync Clock Up to 2.2MHz
- 42μA Quiescent Current
- Low Shutdown Mode Current
- 100% Duty Cycle Operation
- Internal Compensation Mode
- Selectable AAM or FCCM Operation Option
- External Soft Start
- Remote EN Control
- Power Good Indicator
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection
- V_{IN} Under-Voltage Lockout
- V_{OUT} Over-Voltage Protection
- Thermal Shutdown
- Available in a QFN-11 (2mmx3mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Portable Instruments
- Industrial Supplies
- Battery-Powered Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2124GD-AEC1	QFN-11 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ2124GD-AEC1–Z).

** Moisture Sensitivity Level Rating

TOP MARKING

BGD

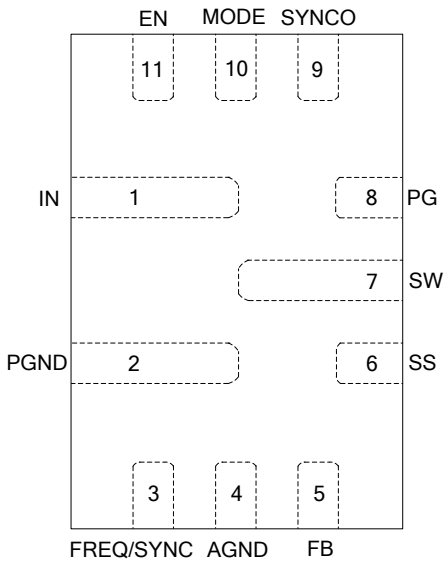
YWW

LLL

BGD: Product code of MPQ2124GD-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-11 (2mmx3mm)

PIN FUNCTIONS

PIN #	Name	Description
1	IN	**Input supply.** IN supplies all power to the converter. Place a decoupling capacitor to ground, as close as possible to the IC, to reduce switching spikes.
2	PGND	**Power ground.** Connect 2 large copper areas to the negative terminals of the input and output capacitors.
3	FREQ/SYNC	**Switching frequency programmable and synchronization input.** Connect a resistor to GND to set the switching frequency. The switching frequency can be synchronized to an external clock via this pin.
4	AGND	**Analog ground.** Ground for the internal logic and signal circuit.
5	FB	**Feedback point.** Negative input of the error amplifier. Connect to the tap of an external resistor divider between the output and GND to set the regulation voltage. In addition, the power good and under-voltage lockout circuits use FB to monitor the output voltage.
6	SS	**Soft start.** Place a capacitor from SS to GND to externally set the soft-start time. Floating this pin will activate the internal default 1ms soft-start setting.
7	SW	**Switch output.** Internally connect to the high-side and low-side power switches. Outside connect to the output inductor.
8	PG	**Power good indicator.** The PG output is an open drain that connects to VIN with an internal pull-up resistor. PG is pulled up to V_{IN} when the FB voltage is within 15% of the regulation level. If the FB voltage is out of that regulation range, it drops down.
9	SYNCO	**Synchronization output.** Outputs a 180° out-of-phase clock to the other devices.
10	MODE	**Mode selection.** Connect to logic high or the input voltage (V_{IN}) for FCCM. Connect to logic low or ground for AAM. Do not leave MODE floating.
11	EN	**Enable input.** Drive EN high to turn on the device. Leave EN floating or grounded to disable the device.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 6.5V
V_{SW} ..... -0.3V (-3V for <10ns) to 6.5V (7.0V for <10ns)
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 1.78W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}) ..... 2.7V to 6.0V
Output voltage (V_{OUT}) ..... 0.606V to V_{IN}
Load current range ..... 0A to 3A
Operating junction temp (T_J) -40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-11 (2mmx3mm)		
JESD51-7 (4)	70	15 °C/W
EV2124-D-00A (5)	42	13.5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the module will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating junction temperature above 125°C may be supported. Contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on standard EVB, 6.35cmx6.35cm, 2oz copper thick, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and UVLO						
Supply current (quiescent)	I_Q	Mode = AAM, V_{EN} = 2V, no load, R_{FREQ} = 1MΩ, T_J = 25°C		42	50	µA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	Mode = AAM, V_{EN} = 0V, T_J = 25°C		0	1	µA
		T_J = -40°C to +125°C			20	
V_{IN} UVLO rising threshold	$INUV_{Vth-R}$		2.3	2.5	2.7	V
V_{IN} UVLO falling threshold	$INUV_{Vth-F}$		2	2.15	2.3	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$			350		mV
Output and Regulation						
Regulated FB voltage	V_{FB}	T_J = 25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.591		0.621	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Switches and Frequency						
High-side switch on resistance	R_{DSON-P}	V_{IN} = 5V, I_{OUT} = 200mA		35	70	mΩ
Low-side switch on resistance	R_{DSON-N}	V_{IN} = 5V, I_{OUT} = 200mA		25	70	mΩ
High-side SW leakage current	$I_{HSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V V_{SW} = 6V, T_J = 25°C		0	1	µA
		T_J = -40°C to +125°C			30	
Low-side SW leakage current	$I_{LSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V, T_J = 25°C		0	1	µA
		T_J = -40°C to +125°C			10	
Switching frequency	f_{SW}	R_{FREQ} = 499kΩ	380	450	520	kHz
		R_{FREQ} = 75kΩ	1800	2100	2400	
SYNC frequency range	f_{SYNC}		0.3		2.2	MHz
SYNC voltage high threshold	$V_{SYNC-HIGH}$	V_{IN} = 2.7V (6)	1.5			V
		V_{IN} = 3.6V	1.8			
		V_{IN} = 6V (6)	3.2			
SYNC voltage low threshold	$V_{SYNC-LOW}$	V_{IN} = 2.7V (6)			0.8	V
		V_{IN} = 3.6V			1.1	
		V_{IN} = 6V (6)			1.6	
Maximum duty cycle	D_{MAX}			100		%
Minimum on time (6)	t_{ON-MIN}			50		ns
Minimum off time (6)	$t_{OFF-MIN}$			95		ns
PG						
PG sink current capacity	$V_{PG-SINK}$	Sink 1mA			300	mV
PG logic high voltage	$V_{PG-HIGH}$	V_{IN} = 5V	4.5			V
PG delay time	$t_{G-DELAY}$	V_{OUT} rising ddge	40	100	180	µs
		V_{OUT} falling edge	5	20	30	µs
PG upper rising threshold	PG_{UP_R}	As a percentage of V_{FB}	108	115	122	%
PG upper hysteresis	PG_{UP_HYS}	As a percentage of V_{FB}		5		%
PG lower rising threshold	PG_{LOW_R}	As a percentage of V_{FB}	80	85	90	%
PG lower hysteresis	PG_{LOW_HYS}	As a percentage of V_{FB}		5		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
EN						
EN input rising threshold	$V_{EN-RISING}$		1.2			V
EN input falling threshold	$V_{EN-FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2	5	µA
		V_{EN} = 0V		0	0.5	µA
Mode and Soft Start						
Mode pin rising threshold	$V_{MODE-FCCM}$	Into FCCM	1.2			V
Mode pin falling threshold	$V_{MODE-AAM}$	Into AAM			0.4	V
Mode input leakage current	I_{MODE}	Pulled up to 6V			1	µA
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	4	6	µA
Default soft-start time	$t_{SS-DEFAULT}$			1		ms
Protections						
Peak current limit	$I_{PEAK-LIMIT}$	Sourcing, D = 40%		6.3		A
Valley current limit	$I_{VALLEY-LIMIT}$			4		A
OCP timer (6)	t_{OCP}			100		µs
Zero cross threshold	I_{ZCD}			100		mA
Output over-voltage limit	OV_{LIMIT}	As percentage of V_{FB}		115		%
Thermal shutdown(6)	T_{SD}	Temperature rising		170		°C
Thermal shutdown hysteresis(6)	T_{SD-SYS}			25		°C

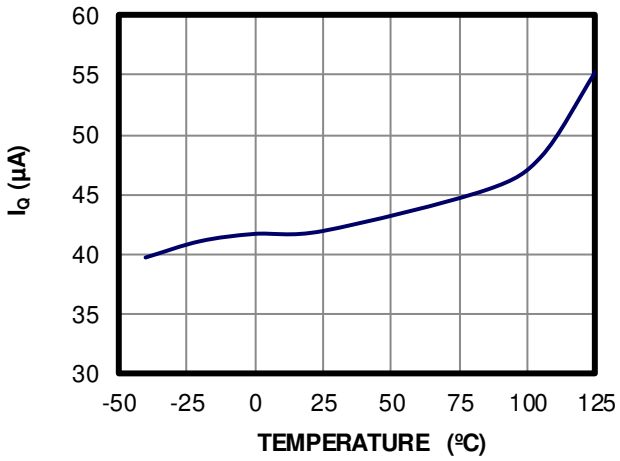
Note:

6) Not tested in production; guaranteed by design and characterization.

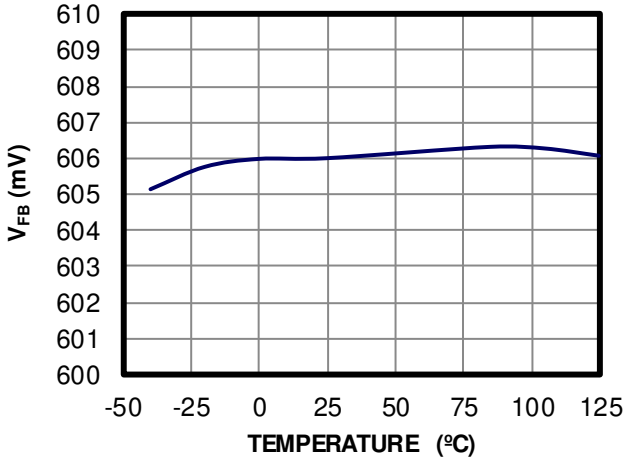
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

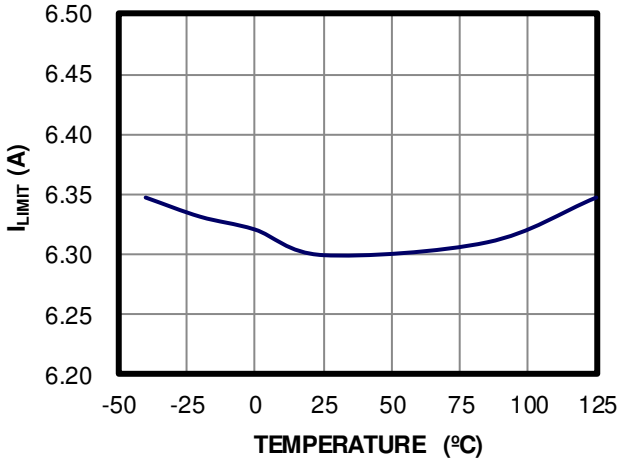
Quiescent Current vs. Temperature



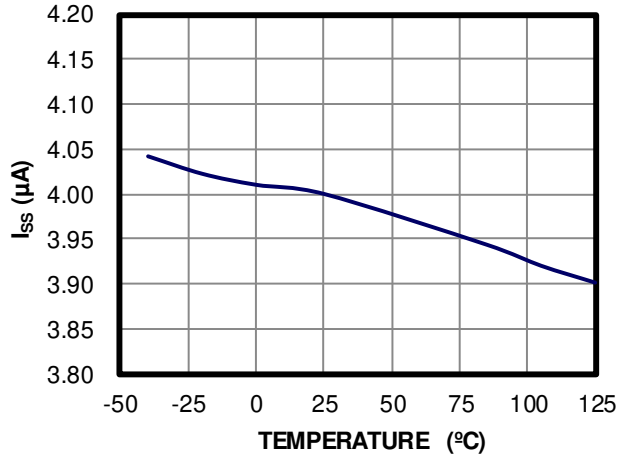
Feedback Voltage vs. Temperature



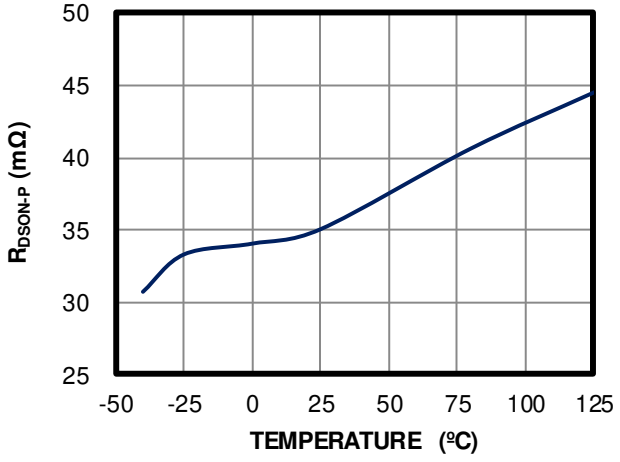
Current Limit vs. Temperature



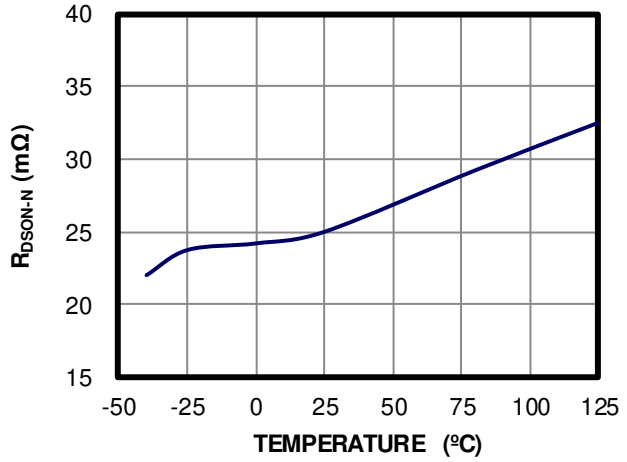
Soft-Start Current vs. Temperature



High-Side Switch On Resistance vs. Temperature



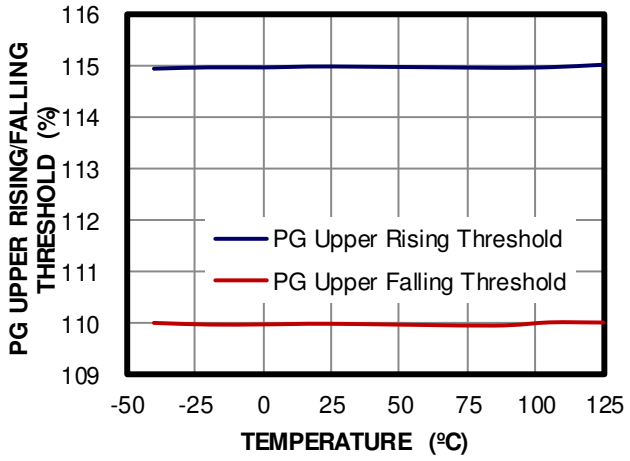
Low-Side Switch On Resistance vs. Temperature



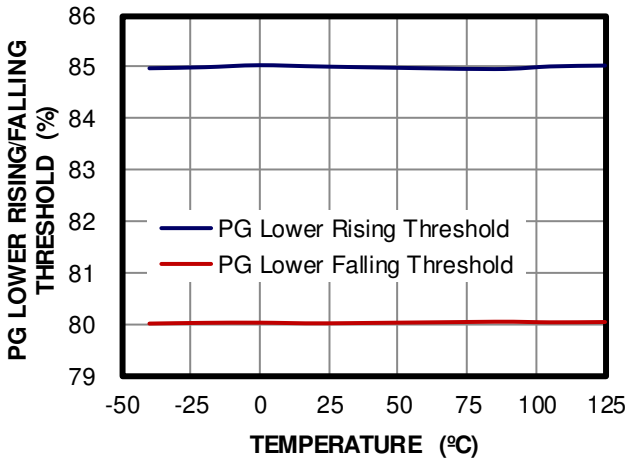
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

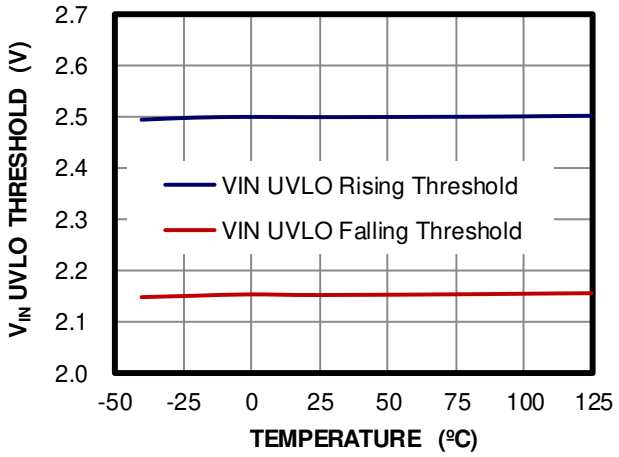
PG Upper Rising/Falling Threshold vs. Temperature



PG Lower Rising/Falling Threshold vs. Temperature



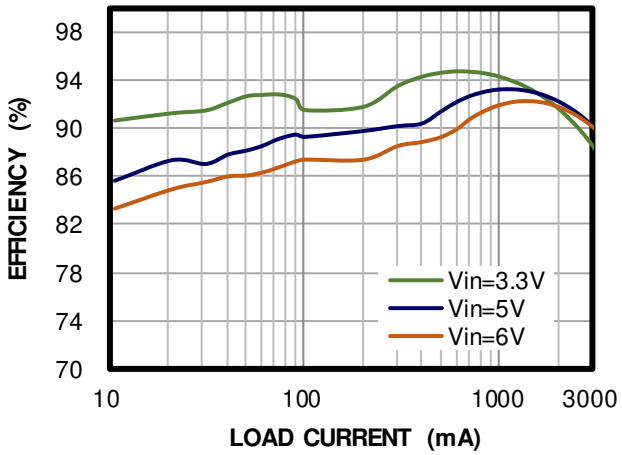
V_{IN} UVLO Threshold vs. Temperature



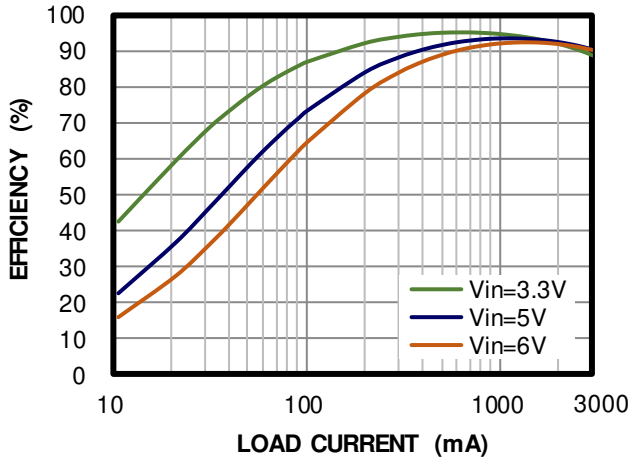
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

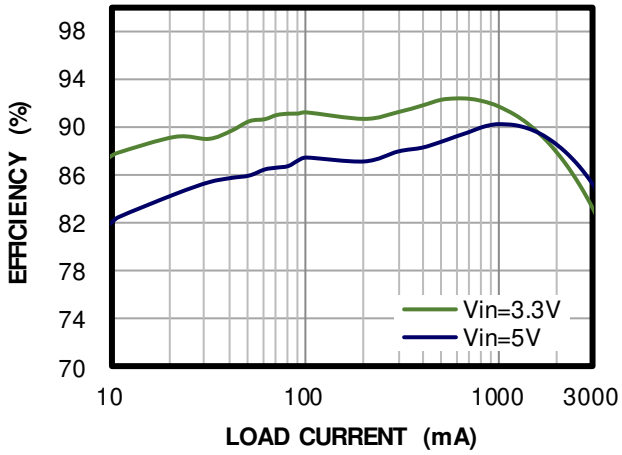
Efficiency vs. Load Current
V_{OUT} = 1.8V, AAM



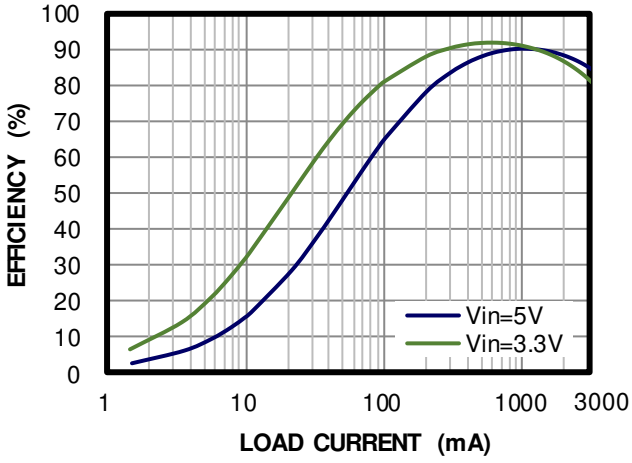
Efficiency vs. Load Current
V_{OUT} = 1.8V, CCM



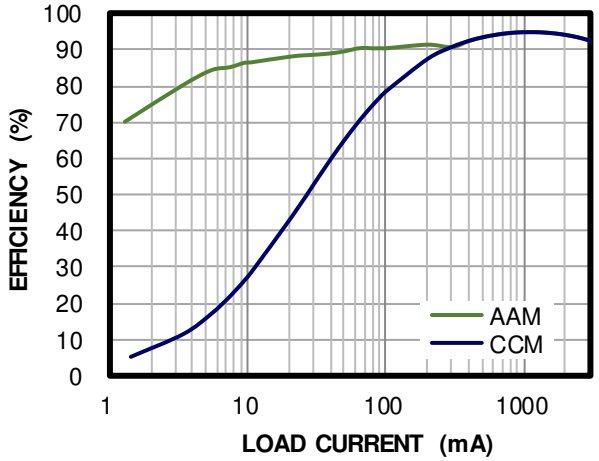
Efficiency vs. Load Current
V_{OUT} = 1.2V, AAM



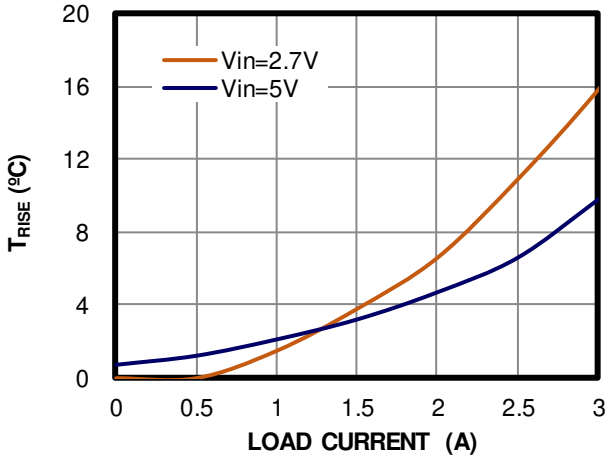
Efficiency vs. Load Current
V_{OUT} = 1.2V, CCM



Efficiency vs. Load Current
V_{IN} = 5V, V_{OUT} = 2.5V



Case Thermal Rise
V_{OUT} = 1.8V, AAM

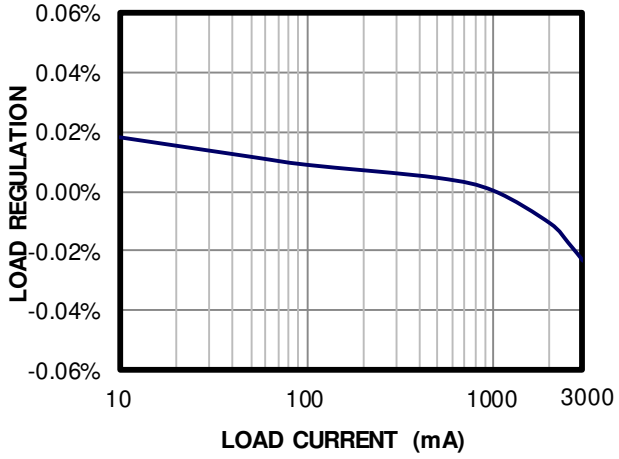


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

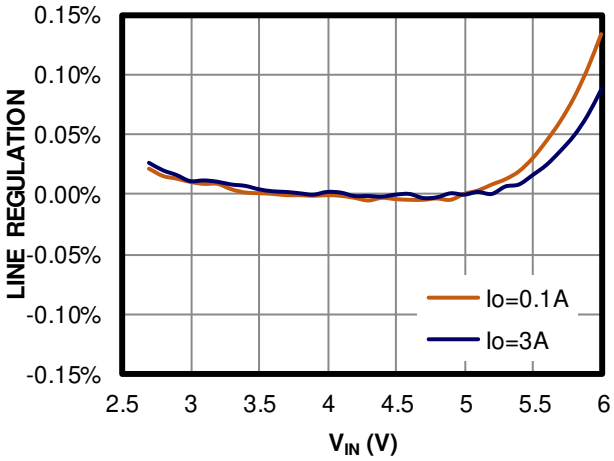
Load Regulation

V_{OUT} = 1.8V, AAM

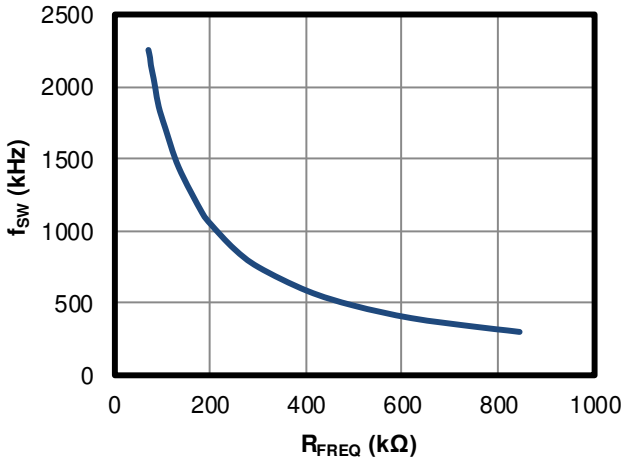


Line Regulation

V_{OUT} = 1.8V, AAM



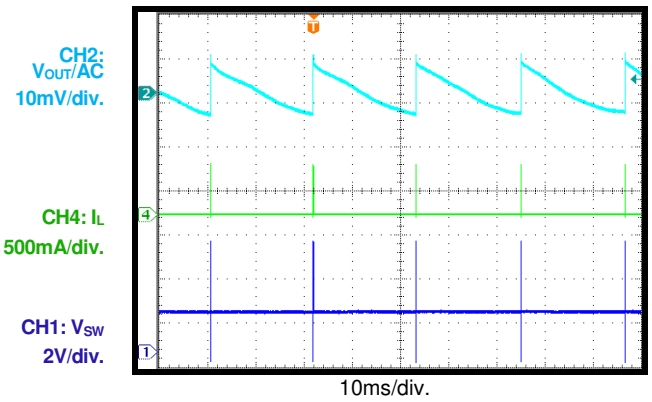
Switching Frequency vs. R_{FREQ}



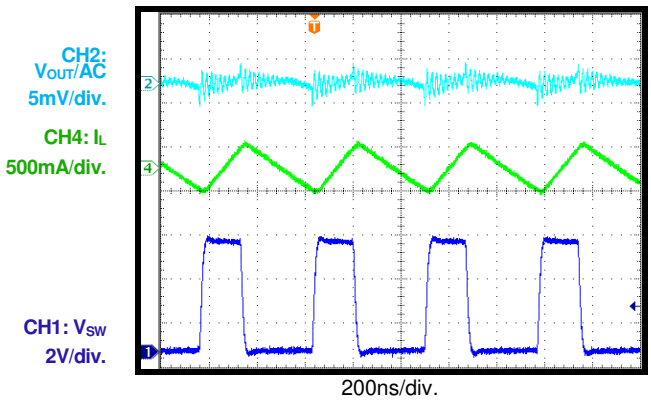
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

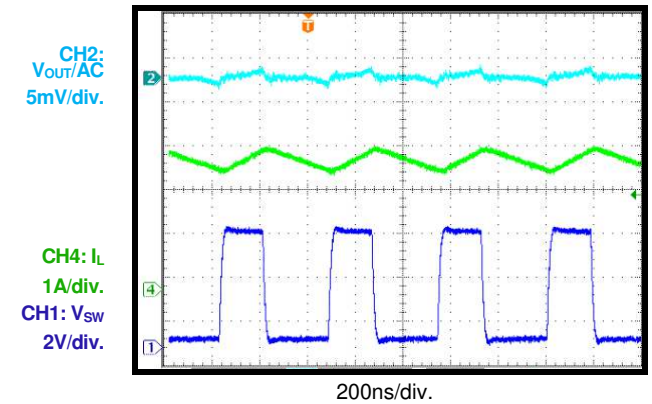
Steady State
I_{OUT} = 0A, AAM



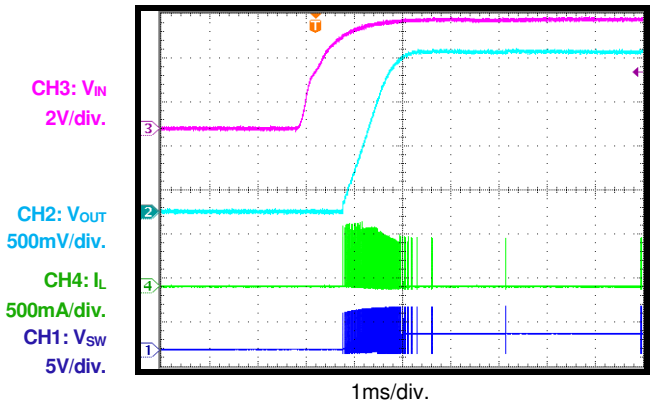
Steady State
I_{OUT} = 0A, CCM



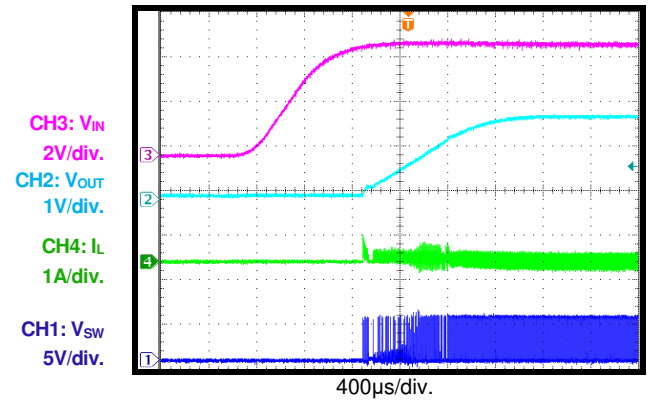
Steady State
I_{OUT} = 3A



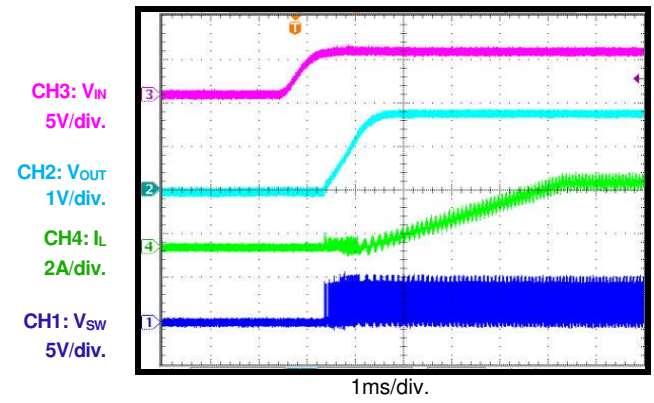
Start-Up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, CCM



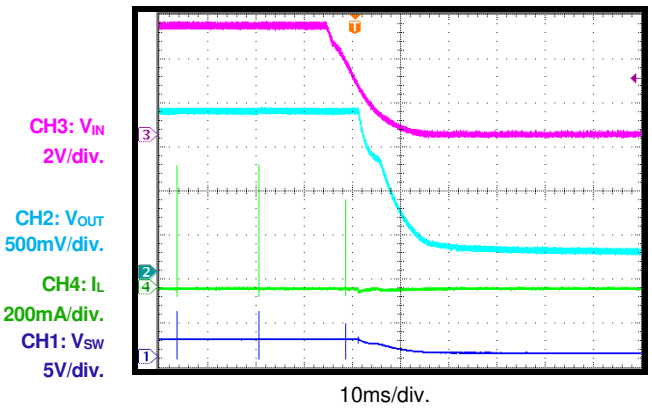
Start-Up through VIN
I_{OUT} = 3A



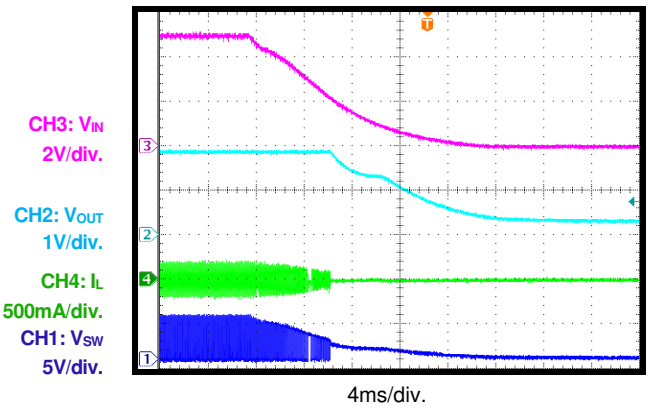
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

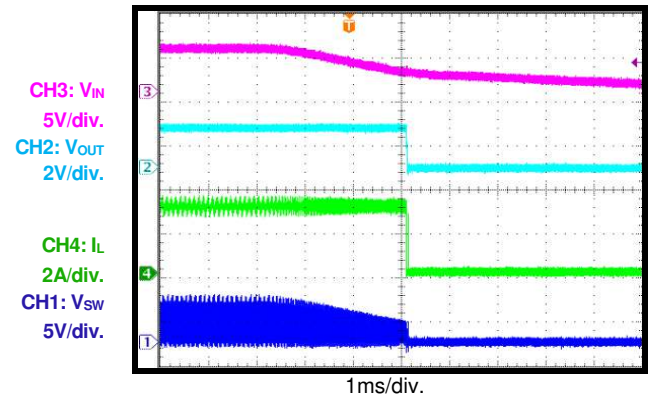
Shutdown through VIN
I_{OUT} = 0A, AAM



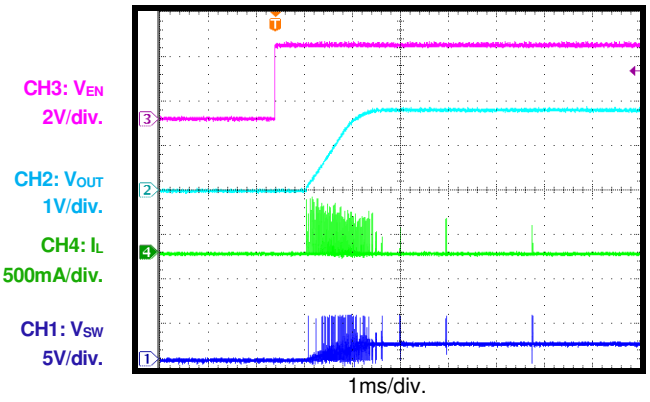
Shutdown through VIN
I_{OUT} = 0A, CCM



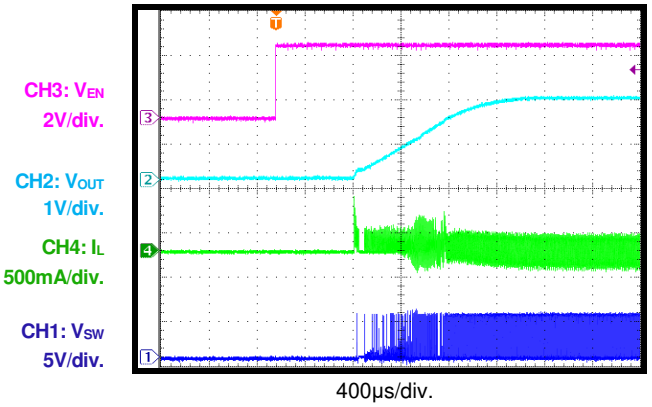
Shutdown through VIN
I_{OUT} = 3A



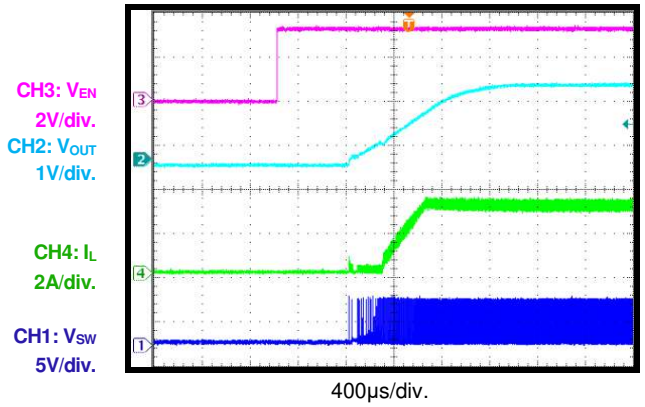
Start-Up through EN
I_{OUT} = 0A, AAM



Start-Up through EN
I_{OUT} = 0A, CCM



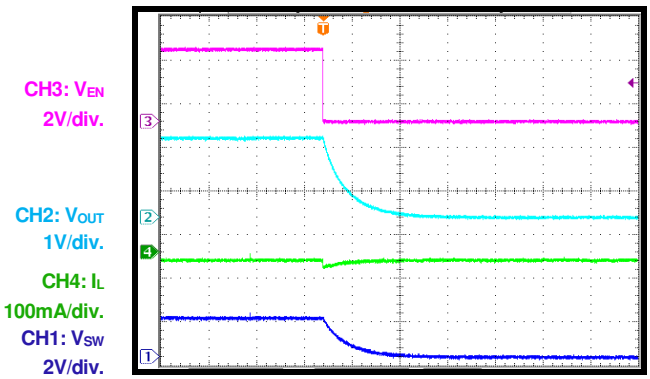
Start-Up through EN
I_{OUT} = 3A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

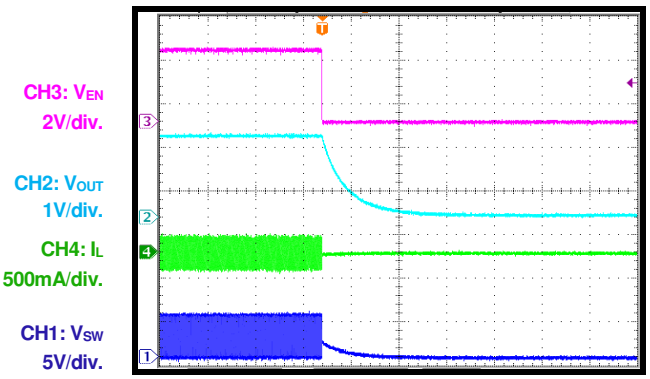
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through EN
I_{OUT} = 0A, AAM



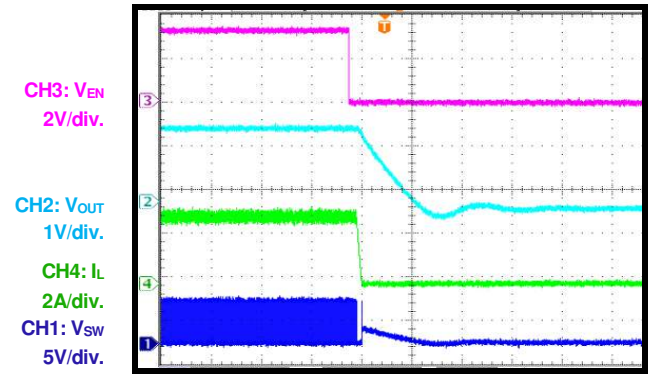
10ms/div.

Shutdown through EN
I_{OUT} = 0A, CCM



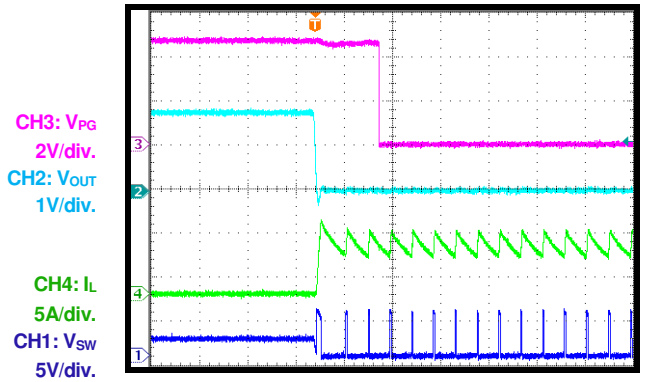
10ms/div.

Shutdown through EN
I_{OUT} = 3A



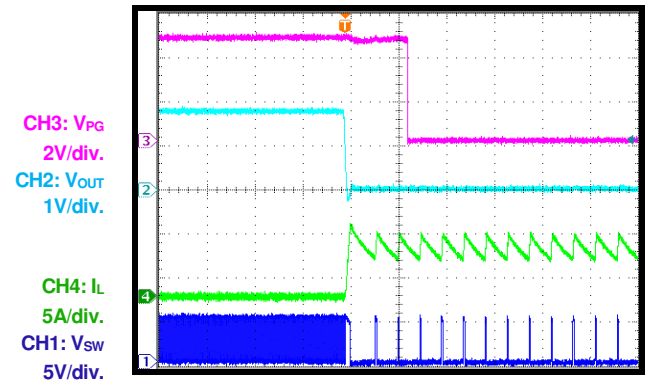
20µs/div.

SCP Entry
I_{OUT} = 0A, AAM



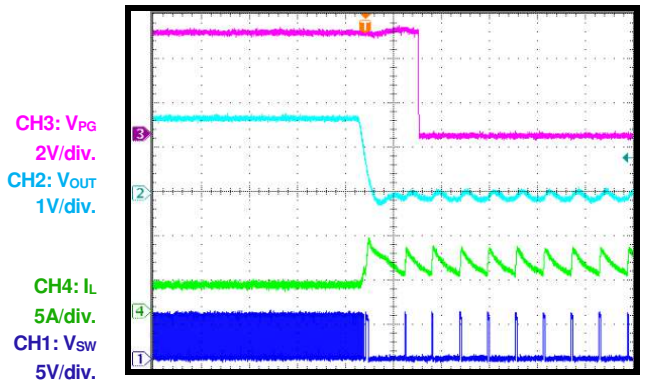
20µs/div.

SCP Entry
I_{OUT} = 0A, CCM



20µs/div.

SCP Entry
I_{OUT} = 3A

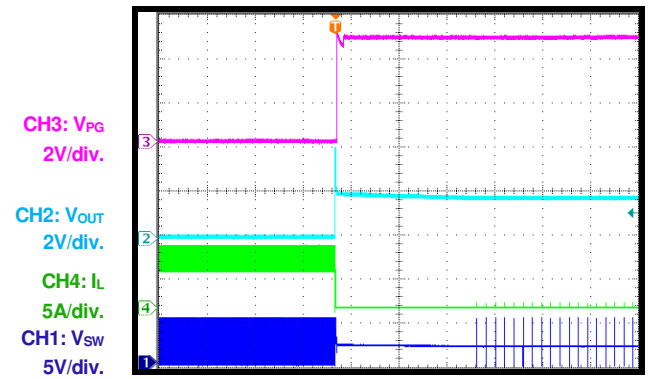


20µs/div.

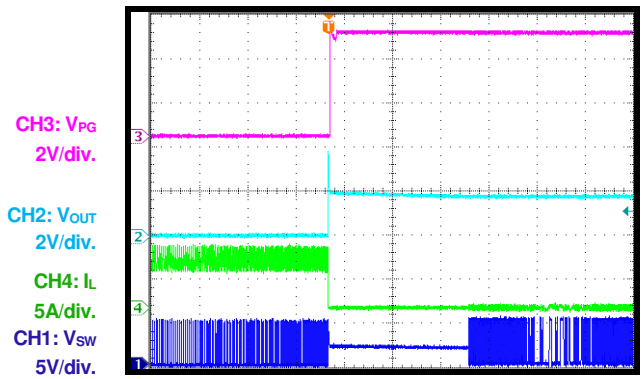
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

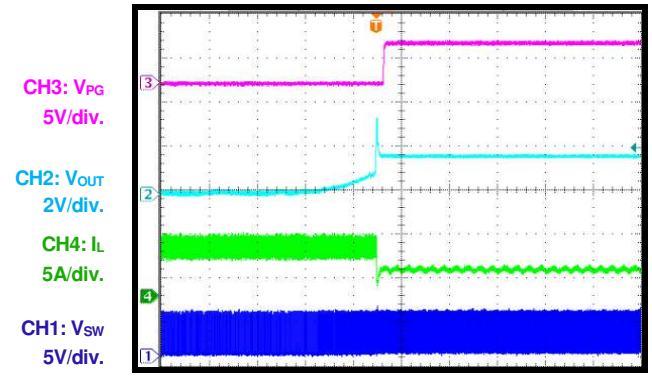
SCP Recovery
I_{OUT} = 0A, AAM



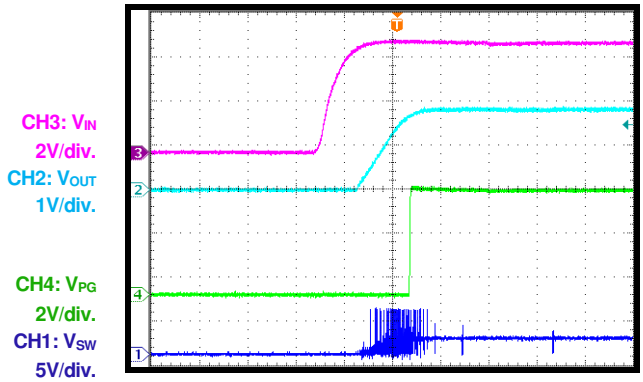
SCP Recovery
I_{OUT} = 0A, CCM



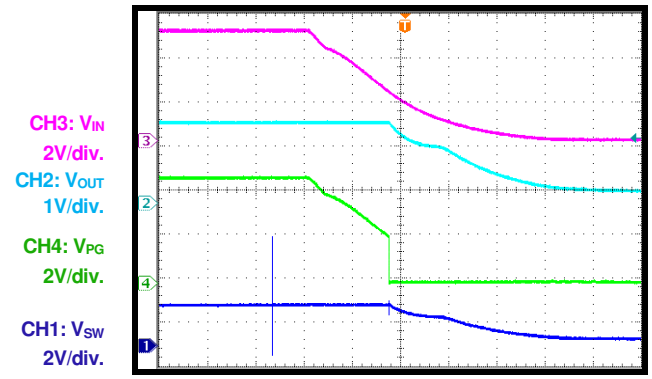
SCP Recovery
I_{OUT} = 3A



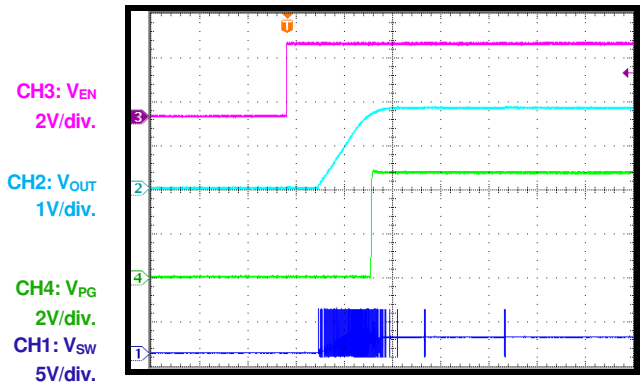
PG in Start-Up through VIN
I_{OUT} = 0A, AAM



PG in Shutdown through VIN
I_{OUT} = 0A, AAM



PG in Start-Up through EN
I_{OUT} = 0A, AAM

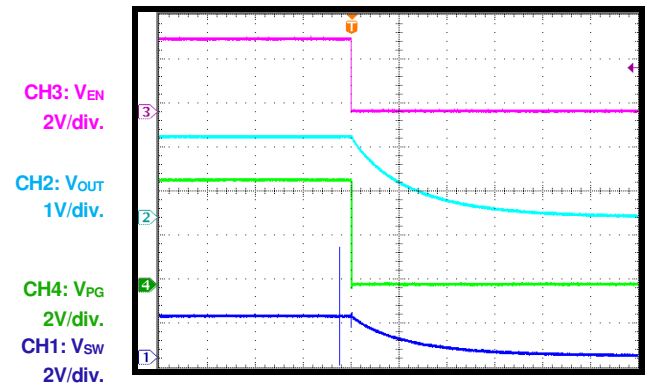


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

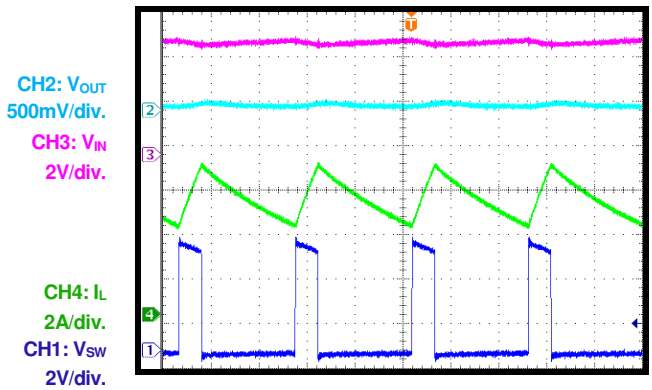
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

PG in Shutdown through EN

I_{OUT} = 0A, AAM

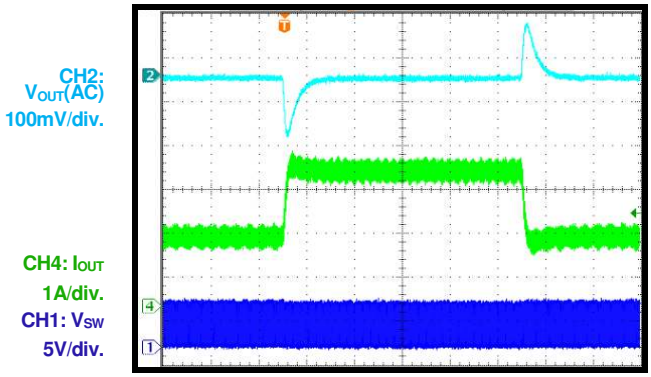


SCP Steady State



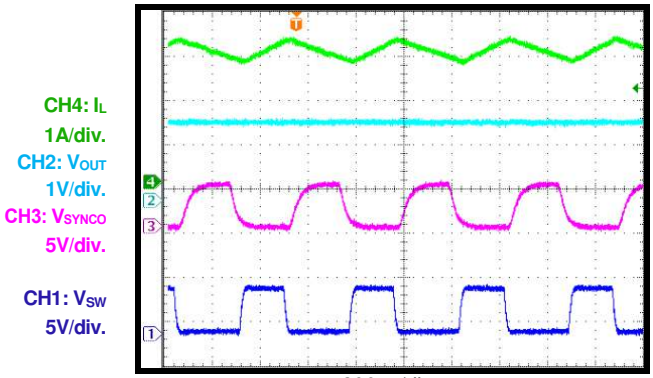
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



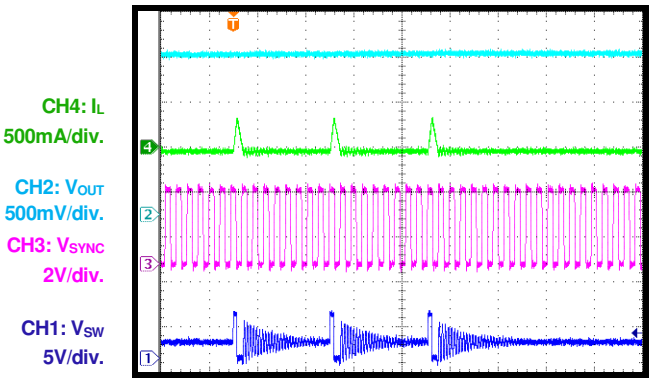
SYNCO

I_{OUT} = 3A



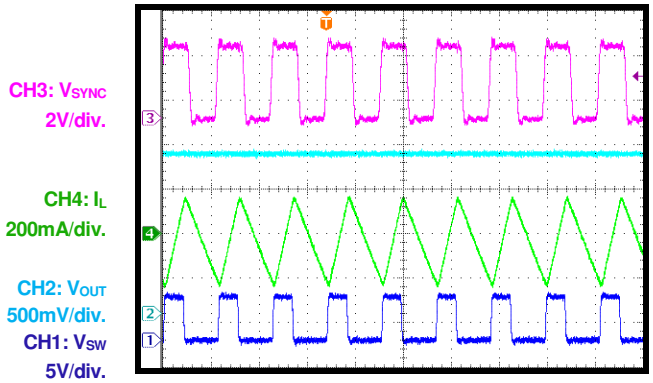
SYNCIN

I_{OUT} = 0A, AAM, SYNC clock = 2.2MHz



SYNCIN

I_{OUT} = 0A, FCCM, SYNC clock = 2.2MHz

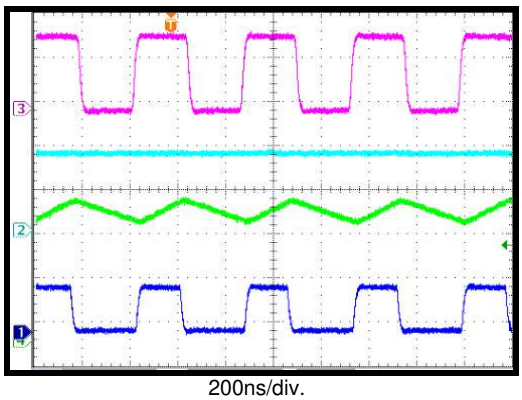


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

SYNCIN

I_{OUT} = 3A, SYNC clock = 2.2MHz



FUNCTIONAL BLOCK DIAGRAM

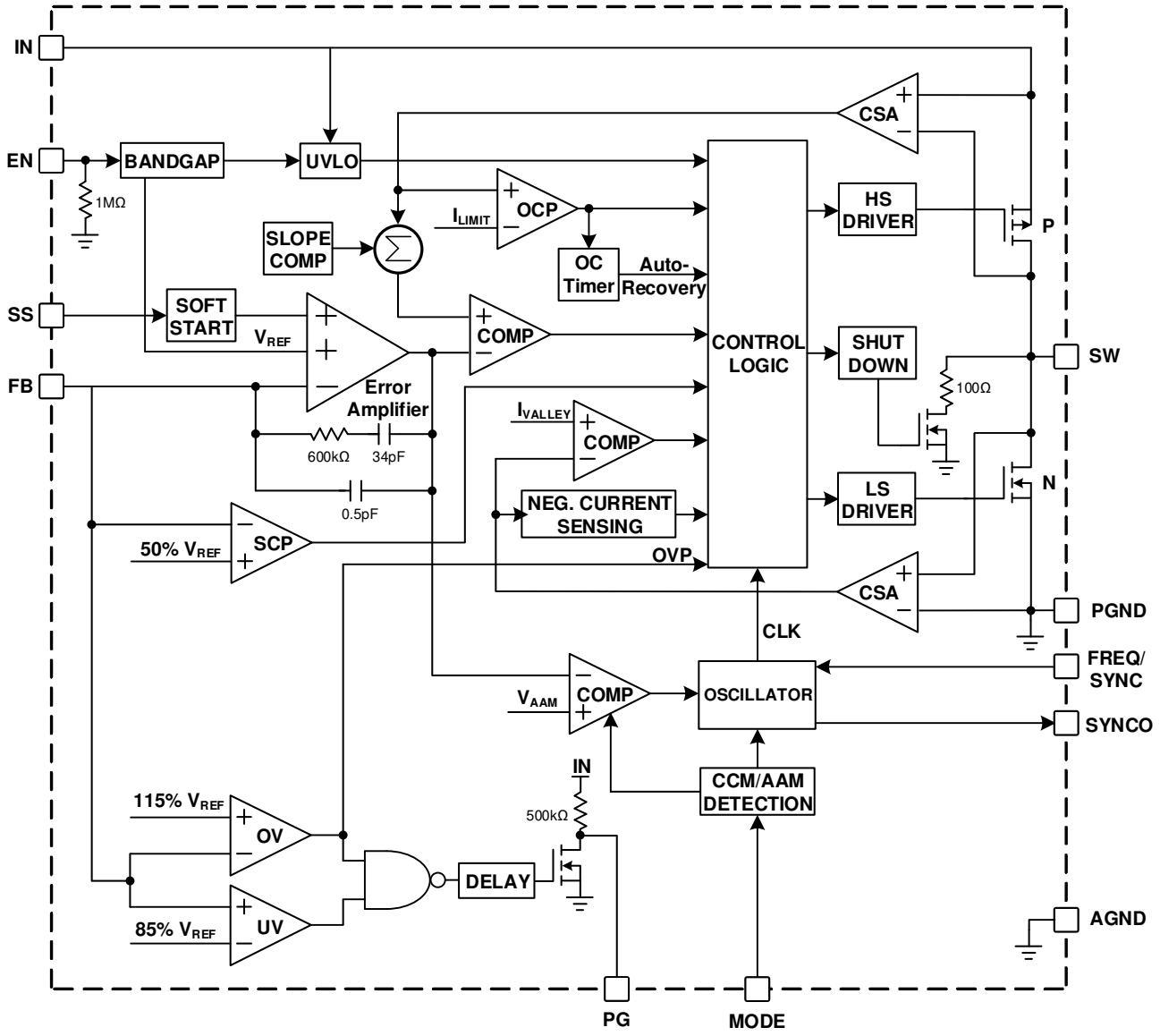


Figure 1: Functional Block Diagram

OPERATION

The MPQ2124 is a fully integrated, synchronous rectified, step-down, non-isolated switch-mode converter. It uses peak current mode control with internal compensation for faster transient response and cycle-by-cycle current limiting.

Figure 1 shows the device's functional block diagram. It is available with a 2.7V to 6.0V input supply range, and can achieve up to 3A of continuous output current with excellent load and line regulation over an ambient temperature range of -40°C to +125°C. The output voltage can be regulated as low as 0.606V.

The MPQ2124 is optimized for low-voltage portable applications where efficiency and small size are critical. It can operate with a switching frequency up to 2.2MHz, which enables the use of a smaller inductor while still providing excellent efficiency. It also allows for high power conversion efficiency under light-load conditions with AAM.

Forced Continuous Conduction Mode (FCCM)

Pulling MODE high (>1.2V) forces the converter into forced continuous conduction mode (FCCM). In FCCM, the MPQ2124 operates in a fixed-frequency, peak current control mode to regulate the output voltage, regardless of the output current. An internal clock initiates a FCCM cycle. At the rising edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage, which is the output of the internal error amplifier. The output voltage of the error amplifier depends on the difference between the output feedback voltage and the internal high-precision reference voltage, and determines how much energy should be transferred to the load. The higher the load current, the higher the COMP voltage.

When the HS-FET is off, the low-side switch (LS-FET) turns on and remains on until the next clock cycle starts. During this time, the inductor current flows through the LS-FET. In order to avoid shoot-through, a dead time is inserted to avoid the HS-FET and LS-FET turning on at the same time. For each turn-on/off period in a switching cycle, the HS-FET remains on/off with a minimum on/off time limit.

Advanced Asynchronous Mode (AAM)

Pulling MODE low (<0.4V) forces the converter into light-load advanced asynchronous mode (AAM). There is an internally fixed AAM threshold voltage (V_{AAM}). Under light-load conditions, the value of V_{COMP} is low. If V_{COMP} exceeds V_{AAM}, the MPQ2124 enters discontinuous conduction operation with a fixed frequency, as long as the inductor current approaches zero. If the load decreases further, or there is no load that makes V_{COMP} fall below V_{AAM}, the internal clock is blocked, making the MPQ2124 skip some pulses. During this time, V_{FB} is below V_{REF}, so V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset, and the crossover time is taken as a benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from a light-load condition, V_{COMP} becomes larger, and the switching frequency increases.

If the output current exceeds the critical level, when V_{COMP} is above V_{AAM}, the MPQ2124 resumes fixed-frequency control, which is the same as FCCM (see Figure 2).

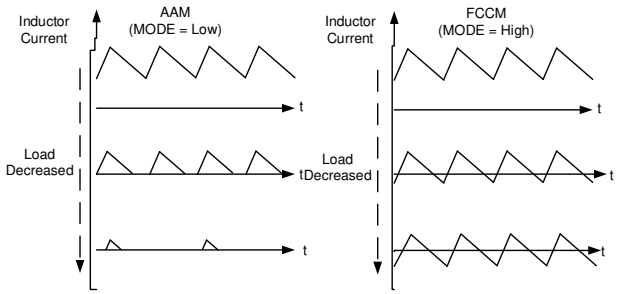


Figure 2: AAM and FCCM

Enable

The MPQ2124 can be enabled or disabled via a remote EN signal referenced to ground. The remote EN control operates with positive logic that is compatible with popular logic devices. Positive logic implies that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the converter is enabled by pulling EN above 1.2V. Leaving the EN pin floating or grounded disables the MPQ2124. There is an internal 1MΩ resistor from EN to ground.

Oscillator and SYNC Function

The oscillating frequency of the MPQ2124 can be programmed by an external frequency resistor. The frequency resistor should be located between FREQ and GND, as close to the device as possible.

Select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 10.

The FREQ pin can also be used to synchronize the internal oscillator rising edge to an external clock falling edge. Choose a proper amplitude for the SYNC clock to drive the internal logic (see the Electrical Characteristics section on page 5). It is recommended to keep the external SYNC frequency between 300kHz and 2.2MHz. There is no pulse width requirement, but there is always parasitic capacitance of the pad. Therefore, if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application. Be sure to add the external SYNC clock (300kHz to 2.2MHz) before the device starts up, and keep the clock on until the device is off. The SYNC signal must not be constant high, constant low, or high/low transition during operation.

The MPQ2124 also has SYNCO pin, which can output a 180° phase-shift clock. This signal can be used to synchronize other devices to keep the same operation frequency but with the opposite phase, which reduces the total input current ripple.

Soft Start and Output Discharge

The MPQ2124 has soft start (SS), which ramps up the output voltage in a controlled slew rate when EN goes high, avoiding overshoot during start-up.

When the soft-start period begins, an internal current source charges the external soft-start capacitor. When the SS voltage (V_{SS}) falls below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. After soft start finishes, the MPQ2124 enters steady state. SS can be used for tracking and sequencing. The SS time (t_{SS}) set by the external SS capacitor can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the internal 4μA SS charge current.

When SS is floating, the SS time is 1ms following the internal setting.

When disabled or in an input shutdown, the MPQ2124 discharges the output voltage to GND through an internal 100Ω resistor that is in parallel to the LS-FET.

Pre-Biased Start-Up

At start-up, if $V_{FB} > V_{SS}$ (which means the output has a pre-biased voltage), neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB}.

100% Duty Cycle

The MPQ2124 can operate with 100% duty cycle, which can help extend the battery life. When the input voltage is too low to maintain output regulation, the device turns the HS-FET fully on to achieve maximum output voltage.

Power Good Indicator

The MPQ2124 has power good (PG) indication. PG is the open drain of the MOSFET. In the presence of an input voltage, the MOSFET turns on so that PG is pulled to GND before soft start is ready. When the output voltage is within a ±15% window of the rated voltage set by FB, PG is pulled up to V_{IN} by an internal resistor after a delay. If V_{FB} moves outside the ±15% range with a hysteresis, the device pulls PG low to indicate a failure output status.

Over-Current Protection (OCP)

The MPQ2124 has a cycle-by-cycle peak current limit control. The inductor current is monitored during a HS-FET on state. Once the inductor current hits the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor falls below a certain current threshold, called the valley current limit. It is very useful to prevent the inductor current from running away and possibly damaging the components.

When the valley current limit is triggered, the OCP timer starts immediately. The OCP timer is

set at 100µs. Reaching the valley current limit during each cycle of this 100µs timeframe triggers SCP.

Short-Circuit Protection (SCP)

When a short circuit occurs, the MPQ2124 immediately reaches its current limit. Meanwhile, the output voltage drops until V_{FB} is below 50% of V_{REF} (0.606V). The device considers this an output dead short, and immediately triggers SCP. In SCP, the inductor current is monitored during the HS-FET on state. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor falls below a certain current threshold, called the valley current limit. The device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection mode is very useful to prevent the inductor current from running away and possibly damaging the components.

Over-Voltage Protection (OVP)

The MPQ2124 monitors the output voltage through FB to detect output over-voltage conditions. If V_{FB} exceeds 115% of V_{REF} (0.606V), OVP is triggered. The LS-FET turns on to discharge V_{OUT} until the inductor current drops to zero while the HS-FET remains off. Then the LS-FET turns off, and the output is discharged through the internal 100Ω resistor in parallel to the LS-FET. The control does not resume switching until the output is within regulation.

Under-Voltage Lockout (UVLO) Protection

The MPQ2124 has input under-voltage lockout (UVLO) protection to ensure the device maintains reliable output power. Assuming EN is active, the MPQ2124 is powered on when the input voltage exceeds the UVLO rising threshold. It is powered off when the input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient supply voltage. It is a non-latch protection.

Thermal Shutdown

The MPQ2124 offers thermal protection by internally monitoring the IC temperature. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold value (typically 170°C), the whole chip shuts down. This is a non-latch protection. There is a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device resumes operation by initiating a soft start.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, the IC keeps its SS output low to ensure the rest of the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN low, V_{IN} UVLO, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. Then the COMP voltage and internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 3). The feedback resistor (R4) must account for both stability and dynamic response, so it cannot be too large or too small. R4 is estimated to be 100kΩ. R5 is then given using Equation (2):

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

Using a T-type feedback network is highly recommended (see Figure 3).

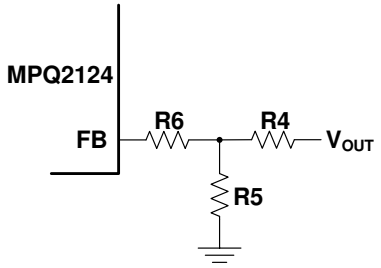


Figure 3: Feedback Network

R6 and R4 are used to set the loop bandwidth. A higher R6 + R4 value means lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth to about 0.1 x f_{SW}.

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. Change the resistance of R_T for loop stability if necessary.

Table 1: Resistor Values for Typical V_{OUT}

V_{OUT} (V)	R6 (kΩ)	R4 (kΩ)	R5 (kΩ)
1.2	100	100 (1%)	100 (1%)
1.5	100	100 (1%)	66.5 (1%)
1.8	100	100 (1%)	49.9 (1%)
2.5	100	100 (1%)	31.6 (1%)
3.3	100	100 (1%)	22.1 (1%)

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. For a default 2.1MHz application, a 0.47µH to 1.5µH inductor is recommended. For highest efficiency, choose an inductor with a DC resistance less than 15mΩ.

When setting the frequency or SYNC function, the inductance may need to be increased as the frequency decreases. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, a larger-value inductor is physically larger, and has a higher series resistance and lower saturation current. A good rule for determining the inductance value is to allow the inductor ripple current to be approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Other capacitors, including Y5V and Z5U, must not be used as these types lose too much capacitance with frequency, temperature, and bias voltage.

Be sure to place the input capacitors as close to IN as possible. For most applications, a 22µF capacitor is sufficient. For a higher output voltage, use a 47µF capacitor to improve system stability. For a small solution size, it is better to choose a proper package size capacitor with a rating voltage compliant to the input spec.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating, which should be greater than the

converter's maximum input ripple current. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating that is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1μF) placed as close to the IC as possible. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the relevant specifications.

The capacitance causes most of the input voltage ripple, which can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Low-ESR ceramic capacitors are recommended to keep the output voltage ripple low and the size small. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Another consideration for the output capacitance is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT}, which causes its voltage to rise. In order to achieve a desired overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the maximum allowable overshoot.

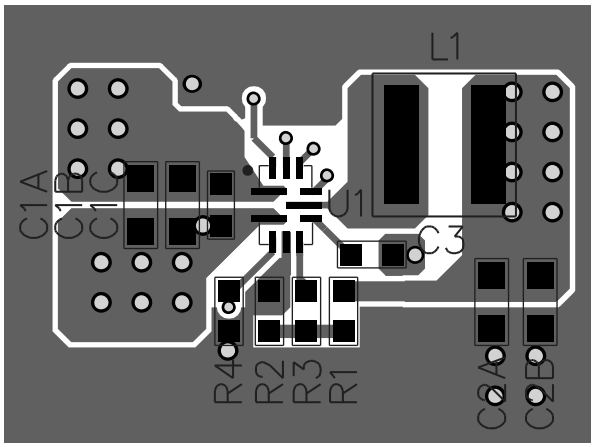
After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2124 can be optimized for a wide range of capacitance and ESR values.

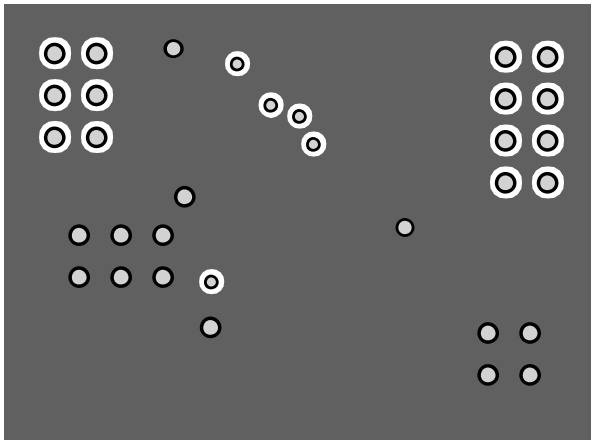
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For optimal performance, refer to Figure 4 and follow the guidelines below:

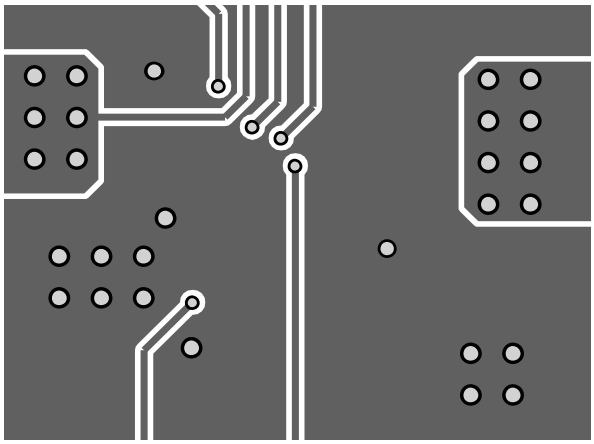
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to IN as possible to minimize high-frequency noise.
3. Place the feedback resistor divider as close as possible to FB, and keep the FB trace away from the switching node.
4. Connect the bottom IN and SW pads to a large copper area to achieve better thermal performance.
5. Use large copper areas for power planes (IN, SW, OUT, and GND) to minimize conduction loss and thermal stress.
6. A 4-layer layout is strongly recommended to achieve better thermal performance. Use multiple vias to connect the power planes to the internal layers.



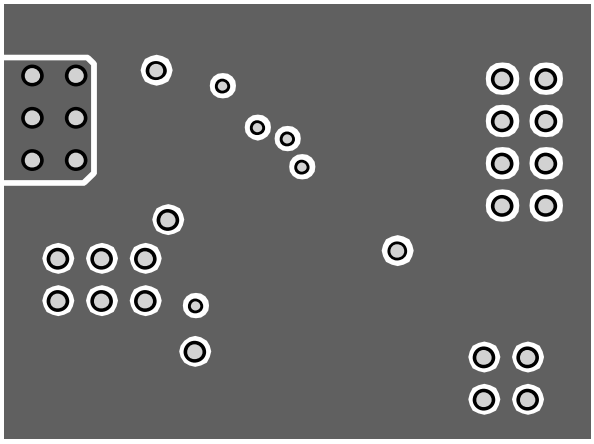
Top and Top Silk Layer



Inner Layer 1



Inner Layer 2



Bottom and Bottom Silk Layer

Figure 4: Recommended PCB Layout (7)

Note:

7) The recommended PCB layout is based on the Typical Application Circuit section on page 24 (see Figure 5).

TYPICAL APPLICATION CIRCUIT

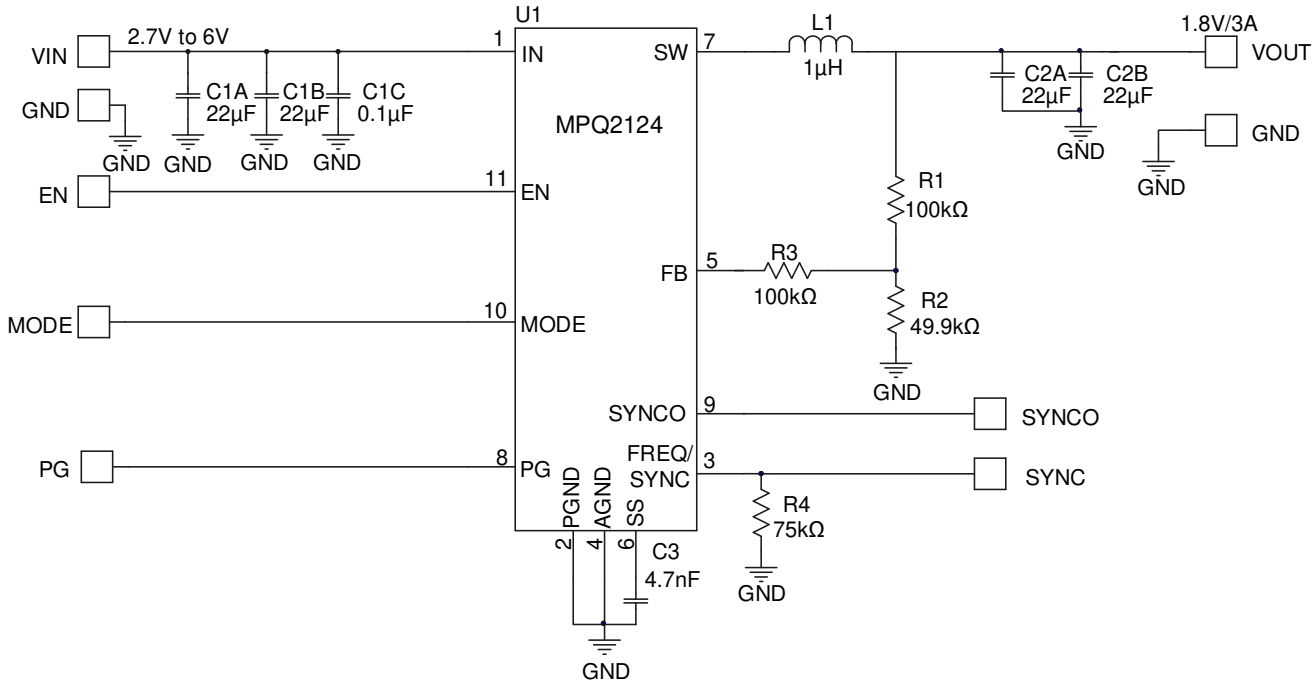


Figure 5: V_{OUT} = 1.8V, I_{OUT} = 3A Application Circuit

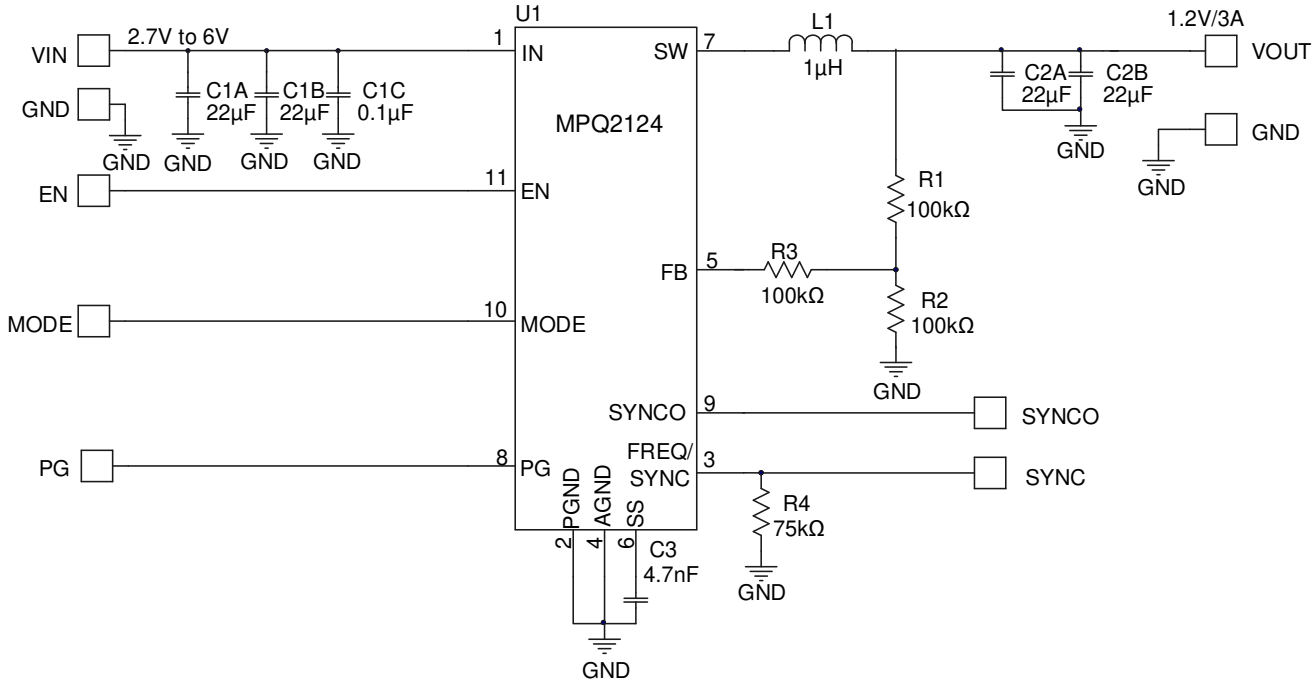
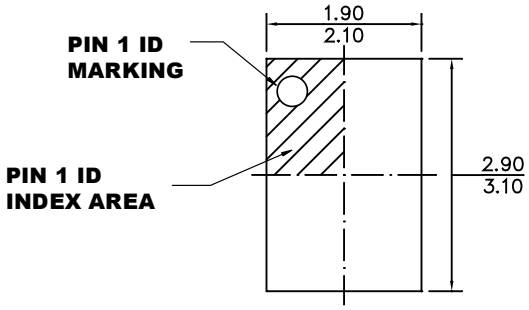


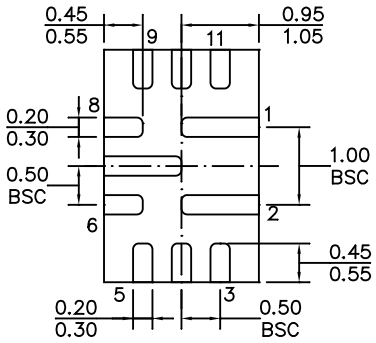
Figure 6: V_{OUT} = 1.2V, I_{OUT} = 3A Application Circuit

PACKAGE INFORMATION

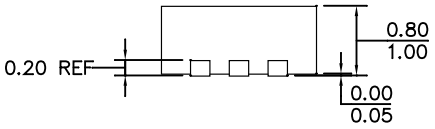
QFN-11 (2mmx3mm)



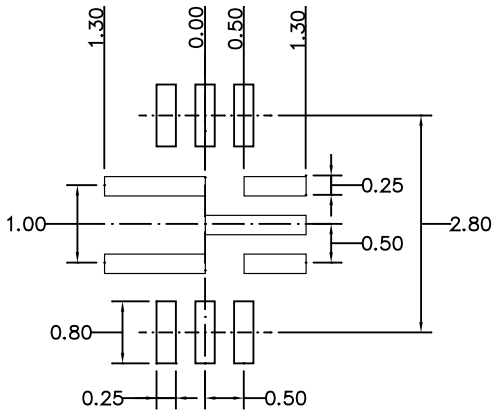
TOP VIEW



BOTTOM VIEW



SIDE VIEW

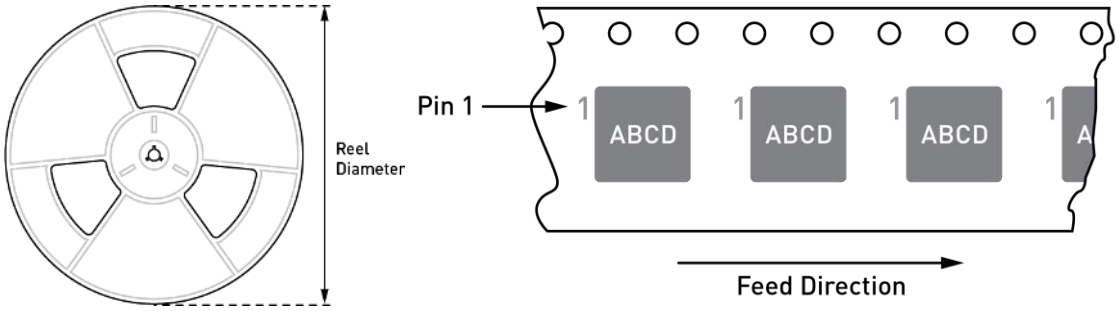


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 1, 2, AND 7 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2124GD-AEC1–Z	QFN-11 (2mmx3mm)	5000	13in	12mm	8mm