19-2659; Rev 0; 10/02

EVALUATION KIT AVAILABLE

W-CDMA/N-CDMA Cellular Phone HBT PA Management ICs

General Description

The MAX1958/MAX1959 power amplifier (PA) power-management ICs (PMICs) integrate an 800mA, dynamically adjustable step-down converter, a 5mA Rail-to-Rail® operational amplifier (op amp), and a precision temperature sensor to power a heterojunction bipolar transistor (HBT) PA in W-CDMA and N-CDMA cell phones.

The high-efficiency, pulse-width modulated (PWM), DC-to-DC buck converter is optimized to provide a guaranteed output current of 800mA. The output voltage is dynamically controlled to produce any fixed-output voltage in the range of 0.75V to 3.4V (MAX1958) or 1V to 3.6V (MAX1959), with settling time less than 30µs for a full-scale change in voltage and current. The 1MHz PWM switching frequency allows the use of small external components while pulse-skip mode reduces quiescent current to 190µA with light loads. The converter utilizes a low on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows for an IC dropout voltage of only 130mV (typ) at 600mA load.

The micropower op amp is used to provide bias to the HBT PA to maximize efficiency. The amplifier features active discharge in shutdown for full PA bias control. It has 5mA rail-to-rail drive capability, 800kHz gain-bandwidth product, and 120dB open-loop voltage gain.

The precision temperature sensor measures temperatures between -40°C to +125°C, with linear temperature-to-voltage analog output characteristics.

The MAX1958/MAX1959 are available in a 20-pin 5mm × 5mm thin QFN package (0.8mm max height).

Applications

W-CDMA and N-CDMA Cellular Phones

Wireless PDAs and Modems

Typical Operating Circuit and Functional Diagram appear at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

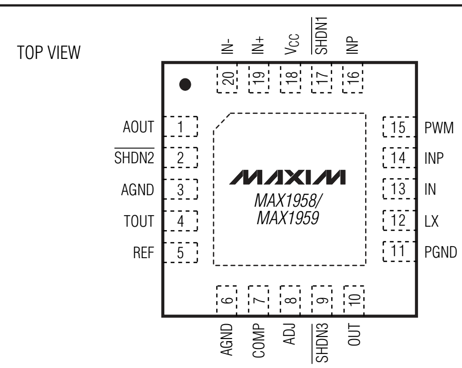
- **Step-Down Converter**
  - **Dynamically Adjustable Output Voltage from 0.75V to 3.4V (MAX1958)**
  - **Dynamically Adjustable Output Voltage from 1V to 3.6V (MAX1959)**
  - **800mA Guaranteed Output Current**
  - **130mV IC Dropout at 600mA Load**
  - **Low Quiescent Current**
    - **190µA (typ) in Skip Mode (MAX1958)**
    - **3mA (typ) in PWM Mode**
    - **0.1µA (typ) in Shutdown Mode**
  - **1MHz Fixed-Frequency PWM operation**
  - **16% to 100% Duty-Cycle Operation**
  - **No External Schottky Diode Required**
  - **Soft-Start**
- **Operational Amplifier**
  - **5mA Rail-to-Rail Output**
  - **Active Discharge in Shutdown**
  - **800kHz Gain-Bandwidth Product**
  - **120dB Open-Loop Voltage Gain (R_L = 100kΩ)**
- **Temperature Sensor**
  - **Accurate Sensor -11.7mV/°C Slope**
  - **-40°C to +125°C-Rated Temperature Range**
- **20-Pin Thin QFN (5mm × 5mm), 0.8mm Height (max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1958ETP	-40°C to +85°C	20 Thin QFN-EP*
MAX1959ETP	-40°C to +85°C	20 Thin QFN-EP

*EP = Exposed paddle.

Pin Configuration



THIN QFN
5mm x 5mm

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

IN, INP, OUT, ADJ, $\overline{SHDN1}$, $\overline{SHDN2}$,
$\overline{SHDN3}$, PWM, V_{CC} to PGND ....-0.3V to +6V
AGND to PGND ....-0.3V to +0.3V
COMP, REF to AGND ....-0.3 to (V_{IN} + 0.3V)
IN+, IN-, AOUT, TOUT to AGND ....-0.3 to (V_{VCC} + 0.3V)
LX Current (Note 1)..±1.6A
Output Short-Circuit Duration....................................Continuous

Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN 5mm x 5mm
(derate 20.8mW/°C above +70°C).............................1670mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: LX has internal clamp diodes to PGND and INP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (STEP-DOWN CONVERTER)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN1}}$ = 3.6V, V_{PWM} = V_{PGND} = V_{AGND} = $V_{\overline{SHDN2}}$ = $V_{\overline{SHDN3}}$ = 0, V_{ADJ} = 1.25V, COMP = IN- = IN+ = AOUT = TOUT = unconnected, C_{REF} = 0.1µF, **T_A = 0°C to +85°C**, V_{OUT} for MAX1958 = 2.2V, V_{OUT} for MAX1959 = 1.7V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		2.6		5.5	V
Undervoltage Lockout Threshold	Rising or falling, hysteresis is 1%	2.20	2.35	2.55	V
Quiescent Current	MAX1958, PWM = AGND		190	300	µA
	MAX1959, PWM = AGND		280	450	
	V_{PWM} = V_{IN}		3		mA
Quiescent Current in Dropout	MAX1958		295	550	µA
	MAX1959		330	600	
Shutdown Supply Current	$V_{\overline{SHDN1}}$ = 0		0.1	6	µA
ERROR AMPLIFIER					
OUT Voltage Accuracy (MAX1958)	V_{ADJ} = 1.932V, I_{LOAD} = 0 to 600mA, V_{PWM} = V_{IN} = 3.8V	3.38	3.40	3.42	V
	V_{ADJ} = 0.426V, I_{LOAD} = 0 to 30mA, V_{PWM} = 0	0.739	0.750	0.761	
	V_{ADJ} = 0.426V, I_{LOAD} = 0 to 30mA, V_{PWM} = V_{IN} = 4.2V	0.739	0.750	0.761	
OUT Voltage Accuracy (MAX1959)	V_{ADJ} = 2.2V, I_{LOAD} = 0 to 600mA, V_{PWM} = V_{IN} = 4V	3.58	3.60	3.62	V
	V_{ADJ} = 0.9V, I_{LOAD} = 0 to 30mA, V_{PWM} = 0	0.985	1.00	1.015	
	V_{ADJ} = 0.9V, I_{LOAD} = 0 to 30mA, V_{PWM} = V_{IN} = 4.2V	0.985	1.00	1.015	
OUT Input Current (MAX1958)	V_{OUT} = 0.75V	2	4	6	µA
	V_{OUT} = 3.4V	11	17	25	
OUT Input Current (MAX1959)	V_{OUT} = 1V	2.5	4.0	6.5	µA
	V_{OUT} = 3.6V	10	16	23	
ADJ Input Current (MAX1958)	V_{ADJ} = 0.426V to 1.932V	-150	+1	+150	nA
ADJ Input Current (MAX1959)	V_{ADJ} = 0.9V to 2.2V	-150	+1	+150	nA
Positive COMP Output Current (MAX1958)	V_{ADJ} = 1V, V_{OUT} = 1.5V, V_{COMP} = 1.25V	-27	-14	-7	µA
Positive COMP Output Current (MAX1959)	V_{ADJ} = 1V, V_{OUT} = 1V, V_{COMP} = 1.25V	-27	-14	-7	µA

ELECTRICAL CHARACTERISTICS (STEP-DOWN CONVERTER) (continued)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN1}}$ = 3.6V, V_{PWM} = V_{PGND} = V_{AGND} = $V_{\overline{SHDN2}}$ = $V_{\overline{SHDN3}}$ = 0, V_{ADJ} = 1.25V, COMP = IN- = IN+ = AOUT = TOUT = unconnected, C_{REF} = 0.1µF, **T_A = 0°C to +85°C**, V_{OUT} for MAX1958 = 2.2V, V_{OUT} for MAX1959 = 1.7V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Negative COMP Output Current (MAX1958)	V_{ADJ} = 1V, V_{OUT} = 2V, V_{COMP} = 1.25V	7	14	27	µA
Negative COMP Output Current (MAX1959)	V_{ADJ} = 1V, V_{OUT} = 1.4V, V_{COMP} = 1.25V	7	14	27	µA
REFERENCE					
REF Output Voltage		1.225	1.250	1.275	V
REF Load Regulation	10µA < I_{REF} < 100µA		2.50	6.25	mV
Undervoltage Lockout Threshold	Rising or falling, 1% hysteresis	0.85	1.00	1.10	V
Supply Rejection	2.6V < V_{IN} < 5.5V		0.07	1.7	mV/V
CONTROLLER					
P-Channel On-Resistance	I_{LX} = 180mA, V_{IN} = 3.6V		0.21	0.40	Ω
	I_{LX} = 180mA, V_{IN} = 2.6V		0.25	0.5	
N-Channel On-Resistance	I_{LX} = 180mA, V_{IN} = 3.6V		0.18	0.30	Ω
	I_{LX} = 180mA, V_{IN} = 2.6V		0.21	0.35	
Current-Sense Transresistance			0.5		V/A
P-Channel Current-Limit Threshold		1.1	1.37	1.6	A
P-Channel Pulse-Skipping Current Threshold	V_{PWM} = 0	0.12	0.15	0.17	A
N-Channel Current-Limit Threshold	V_{PWM} = V_{IN}		-0.5		A
N-Channel Zero-Crossing Comparator	V_{PWM} = 0		20		mA
LX Leakage Current	V_{IN} = 5.5V	-20.0	+0.1	+20.0	µA
LX RMS Current	(Note 1)			1.0	A
Maximum Duty Cycle		100			%
Minimum Duty Cycle	V_{PWM} = 0			0	%
	V_{PWM} = V_{IN} = 4.2V		16		
Oscillator Frequency		0.85	1.00	1.15	MHz
Thermal-Shutdown Threshold	Hysteresis = +15°C		160		°C
LOGIC INPUTS (PWM, $\overline{SHDN1}$)					
Logic Input High	2.6 V < V_{IN} < 5.5 V	1.6			V
Logic Input Low	2.6 V < V_{IN} < 5.5 V			0.6	V
Logic Input Current	V_{IN} = 5.5V		0.1	1	µA

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ELECTRICAL CHARACTERISTICS (OP AMP)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN2}}$ = 2.7V, V_{AOUT} = V_{VCC}/2, R_L = ∞ connected from AOUT to V_{VCC}/2, V_{PGND} = V_{AGND} = $V_{\overline{SHDN1}}$ = $V_{\overline{SHDN3}}$ = V_{PWM} = V_{ADJ} = 0, OUT = LX = TOUT = REF = COMP = unconnected, V_{CM} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			2.6		5.5	V
Supply Current	V_{VCC} = 2.6V			320	800	µA
	V_{VCC} = 5V			375	900	
	$V_{\overline{SHDN2}}$ = 0, V_{VCC} = 5.5V			0.1	2.0	
Input Offset Voltage	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±0.4	±3.0	mV
Input Bias Current	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±10	±100	nA
Input Offset Current	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±1	±10	nA
Input Resistance	V_{IN-} - V_{IN+} ≤ 10mV			4		MΩ
Input Common-Mode Voltage Range, V_{CM}			-0.1		V_{VCC} + 0.1	V
Common-Mode Rejection Ratio, CMRR	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V		60	80		dB
Power-Supply Rejection Ratio, PSRR	2.6V < V_{VCC} < 5.5V		70	90		dB
Large-Signal Voltage Gain, AVOL	V_{AGND} + 0.05V ≤ V_{AOUT} ≤ V_{VCC} - 0.05V	R_L = 100kΩ		120		dB
	V_{AGND} + 0.20V ≤ V_{AOUT} ≤ V_{VCC} - 0.20V	R_L = 2kΩ	85	110		
Output Voltage Swing High, VOH	$\lvert V_{VCC} - V_{VOH} \rvert$	R_L = 100kΩ		1		mV
		R_L = 2kΩ		35	90	
Output Voltage Swing Low, VOL	$\lvert V_{VOL} - V_{AGND} \rvert$	R_L = 100kΩ		1		mV
		RL = 2kΩ		30	90	
Output Short-Circuit Current	Sourcing, V_{VCC} = 5V			11		mA
	Sinking, V_{VCC} = 5V			30		
$\overline{SHDN2}$ Logic Low	2.6V < V_{VCC} < 5.5V				0.3 x V_{VCC}	V
$\overline{SHDN2}$ Logic High	2.6V < V_{VCC} < 5.5V		0.7 x V_{VCC}			V
$\overline{SHDN2}$ Input Current	0 < $V_{\overline{SHDN2}}$ < V_{VCC}			±0.5	±120	nA
Gain Bandwidth Product, GBW				1		MHz
Phase Margin, ϕM				70		Degrees
Gain Margin, GM				20		dB
Slew Rate, SR				0.4		V/µs
Input Voltage Noise Density	f = 10kHz			52		nV/√Hz
Input Current Noise Density	f = 10kHz			0.1		pA/√Hz
Capacitive-Load Stability	AVCL = 1V/V (Note 2)				470	pF
Shutdown Delay Time				3		µs
Enable Delay Time				4		µs

ELECTRICAL CHARACTERISTICS (OP AMP) (continued)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN2}}$ = 2.7V, V_{AOUT} = V_{VCC}/2, R_L = ∞ connected from AOUT to V_{VCC}/2, V_{PGND} = V_{AGND} = $V_{\overline{SHDN1}}$ = $V_{\overline{SHDN3}}$ = V_{PWM} = V_{ADJ} = 0, OUT = LX = TOUT = REF = COMP = unconnected, V_{CM} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On Time			4		µs
Input Capacitance			2.5		pF
Total Harmonic Distortion	f =10kHz, V_{AOUT} = 2V_{P-P}, AVCL =1, V_{VCC} = 5V, R_{AOUT} = 100kΩ to V_{VCC}/2		0.01		%
Settling Time to 0.01%	ΔV_{AOUT} = 4V step, V_{VCC} = 5V, AVCL = 1		10		µs
Active Discharge Output Impedance	$V_{\overline{SHDN2}}$ = 0, I_{AOUT} = 1mA		100	500	Ω

ELECTRICAL CHARACTERISTICS (TEMPERATURE SENSOR)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN3}}$ = 2.7V, V_{AGND} = V_{PGND} = V_{PWM} = $V_{\overline{SHDN1}}$ = $V_{\overline{SHDN2}}$ = V_{ADJ} = 0, IN- = IN+ = AOUT = COMP = LX = OUT = REF = unconnected, C_{TOUT} = 0.01µF (min), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Sensor Error (Note 3)	T_A = 0°C (Note 2)	-3.5		+3.5	°C
	T_A = +25°C (Note 2)	-2.5		+2.5	
	T_A = +85°C	-2.5		+2.5	
Output Voltage at +27°C			1.56		V
Sensor Gain (Note 4)			-11.64		mV/°C
Nonlinearity			±0.4		%
Load Regulation	0 ≤ I_{LOAD} ≤ 15µA			-5	mV
Line Regulation	2.6V ≤ V_{VCC} ≤ 5.5V			-2.3	mV/V
Quiescent Current	2.6V ≤ V_{VCC} ≤ 5.5V		10	18	µA
$\overline{SHDN3}$ Logic High Voltage	2.6V < V_{VCC} < 5.5V	1.6			V
$\overline{SHDN3}$ Logic Low Voltage	2.6V < V_{VCC} < 5.5V			0.6	V
$\overline{SHDN3}$ Current	V_{VCC} = 5.5V		0.1	1.0	µA

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ELECTRICAL CHARACTERISTICS (STEP-DOWN CONVERTER)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN1}}$ = 3.6V, V_{PWM} = V_{PGND} = V_{AGND} = $V_{\overline{SHDN2}}$ = $V_{\overline{SHDN3}}$ = 0, V_{ADJ} = 1.25V, COMP = IN- = IN+ = AOUT = TOUT = unconnected, C_{REF} = 0.1µF, **T_A = -40°C to +85°C**, V_{OUT} for MAX1958 = 2.2V, V_{OUT} for MAX1959 = 1.7V, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		2.6		5.5	V
Undervoltage Lockout Threshold	Rising or falling, hysteresis is 1%	2.20		2.55	V
Quiescent Current	PWM = AGND (MAX1958)			300	µA
	PWM = AGND (MAX1959)			450	
Quiescent Current in Dropout	MAX1958			550	µA
	MAX1959			600	
Shutdown Supply Current	$V_{\overline{SHDN1}}$ = 0			6	µA
ERROR AMPLIFIER					
OUT Voltage Accuracy (MAX1958)	V_{ADJ} = 1.932V, I_{LOAD} = 0 to 600mA, V_{PWM} = V_{IN} = 3.8V	3.36		3.44	V
	V_{ADJ} = 0.426V, I_{LOAD} = 0 to 30mA, V_{PWM} = 0	0.739		0.761	
	V_{ADJ} = 0.426V, I_{LOAD} = 0 to 30mA, V_{PWM} = V_{IN} = 4.2V	0.739		0.761	
OUT Voltage Accuracy (MAX1959)	V_{ADJ} = 2.2V, I_{LOAD} = 0 to 600mA, V_{PWM} = V_{IN} = 4V	3.570		3.625	V
	V_{ADJ} = 0.9V, I_{LOAD} = 0 to 30mA, V_{PWM} = 0	0.98		1.02	
	V_{ADJ} = 0.9V, I_{LOAD} = 0 to 30mA, V_{PWM} = V_{IN} = 4.2V	0.98		1.02	
OUT Input Current (MAX1958)	V_{OUT} = 0.75V	2		6	µA
	V_{OUT} = 3.4V	11		25	
OUT Input Current (MAX1959)	V_{OUT} = 1V	2.5		6.5	µA
	V_{OUT} = 3.6V	10.0		23.0	
ADJ Input Current (MAX1958)	V_{ADJ} = 0.426V to 1.932V	-150		+150	nA
ADJ Input Current (MAX1959)	V_{ADJ} = 0.9V to 2.2V	-150		+150	nA
Positive COMP Output Current (MAX1958)	V_{ADJ} = 1V, V_{OUT} = 1.5V, V_{COMP} = 1.25V	-27.0		-6.5	µA
Positive COMP Output Current (MAX1959)	V_{ADJ} = 1V, V_{OUT} =1V, V_{COMP} = 1.25V	-27.0		-6.5	µA
Negative COMP Output Current (MAX1958)	V_{ADJ} = 1V, V_{OUT} = 2V, V_{COMP} = 1.25V	6.5		27.0	µA
Negative COMP Output Current (MAX1959)	V_{ADJ} = 1V, V_{OUT} = 1.4V, V_{COMP} =1.25V	6.5		27.0	µA
REFERENCE					
REF Output Voltage		1.226		1.275	V
REF Load Regulation	10µA < I_{REF} < 100µA			6.25	mV
Undervoltage Lockout Threshold	Rising or falling, 1% hysteresis	0.85		1.10	V
Supply Rejection	2.6V < V_{IN} < 5.5V			1.7	mV/V

ELECTRICAL CHARACTERISTICS (STEP-DOWN CONVERTER) (continued)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN1}}$ = 3.6V, V_{PWM} = V_{PGND} = V_{AGND} = $V_{\overline{SHDN2}}$ = $V_{\overline{SHDN3}}$ = 0, V_{ADJ} = 1.25V, COMP = IN- = IN+ = AOUT = TOUT = unconnected, C_{REF} = 0.1µF, **T_A = -40°C to +85°C**, V_{OUT} for MAX1958 = 2.2V, V_{OUT} for MAX1959 = 1.7V, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER					
P-Channel On-Resistance	I_{LX} = 180mA, V_{IN} = 3.6V			0.4	Ω
	I_{LX} = 180mA, V_{IN} = 2.6V			0.5	
N-Channel On-Resistance	I_{LX} = 180mA, V_{IN} = 3.6V			0.3	Ω
	I_{LX} = 180mA, V_{IN} = 2.6V			0.35	
P-Channel Current-Limit Threshold		1.1		1.6	A
P-Channel Pulse-Skipping Current Threshold	V_{PWM} = 0	0.11		0.18	A
LX Leakage Current	V_{IN} = 5.5V	-20		+20	µA
LX RMS Current	(Note 1)			1.0	A
Maximum Duty Cycle		100			%
Minimum Duty Cycle	V_{PWM} = 0			0	%
Oscillator Frequency		0.8		1.2	MHz
LOGIC INPUTS (PWM, $\overline{SHDN1}$)					
Logic Input High	2.6V < V_{IN} < 5.5V	1.6			V
Logic Input Low	2.6V < V_{IN} < 5.5V			0.6	V
Logic Input Current	V_{IN} = 5.5V			1	µA

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ELECTRICAL CHARACTERISTICS (OP AMP)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN2}}$ = 2.7V, V_{AOUT} = V_{VCC}/2, R_L = ∞ connected from AOUT to V_{VCC}/2, V_{PGND} = V_{AGND} = $V_{\overline{SHDN1}}$ = $V_{\overline{SHDN3}}$ = V_{PWM} = V_{ADJ} = 0, OUT = LX = TOUT = REF = COMP = unconnected, V_{CM} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		2.6		5.5	V
Supply Current	V_{VCC} = 2.6V			800	µA
	V_{VCC} = 5V			900	
	$V_{\overline{SHDN2}}$ = 0, V_{VCC} = 5.5V			2.0	
Input Offset Voltage	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±3.0	mV
Input Bias Current	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±100	nA
Input Offset Current	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V			±10	nA
Input Common-Mode Voltage Range, V_{CM}		V_{AGND} - 0.1V		V_{VCC} + 0.1V	V
Common-Mode Rejection Ratio, CMRR	V_{AGND} - 0.1V ≤ V_{CM} ≤ V_{VCC} + 0.1V	60			dB
Power-Supply Rejection Ratio, PSRR	2.6V < V_{VCC} < 5.5V	70			dB
Large-Signal Voltage Gain, AVOL	V_{AGND} + 0.20V ≤ V_{OUT} ≤ V_{VCC} - 0.20V, R_L = 2kΩ	85			dB
Output Voltage Swing High, VOH	$\lvert V_{VCC} - V_{VOH} \rvert$, R_L = 2kΩ			90	
Output Voltage Swing Low, VOL	$\lvert V_{VOL} - V_{AGND} \rvert$, RL = 2kΩ			90	mV
$\overline{SHDN2}$ Logic Low	2.6V < V_{VCC} < 5.5V			0.3 x V_{VCC}	V
$\overline{SHDN2}$ Logic High	2.6V < V_{VCC} < 5.5V	0.7 x V_{VCC}			V
$\overline{SHDN2}$ Input Current	0 < $V_{\overline{SHDN2}}$ < V_{VCC}			±120	nA
Capacitive-Load Stability	AVCL = 1V/V (Note 2)			470	pF
Active Discharge Output Impedance	$V_{\overline{SHDN2}}$ = 0, I_{AOUT} = 1mA			500	Ω

ELECTRICAL CHARACTERISTICS (TEMPERATURE SENSOR)

(V_{INP} = V_{IN} = V_{VCC} = $V_{\overline{SHDN3}}$ = 2.7V, V_{AGND} = V_{PGND} = V_{PWM} = $V_{\overline{SHDN1}}$ = $V_{\overline{SHDN2}}$ = V_{ADJ} = 0, IN- = IN+ = AOUT = COMP = LX = OUT = REF = unconnected, C_{TOUT} = 0.01µF (min), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

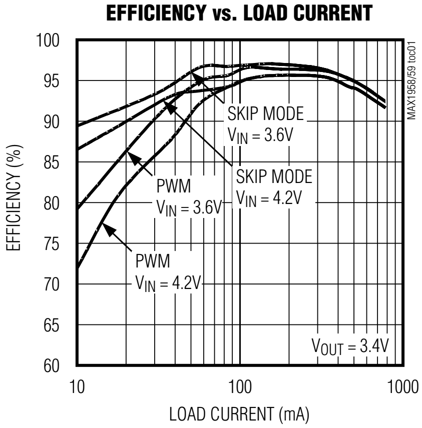
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Sensor Error (Note 3)	T_A = -40°C (Note 2)	-7		+4	°C
	T_A = +25°C (Note 2)	-2.5		+2.5	
	T_A = +85°C	-2.5		+2.5	
Load Regulation	0 ≤ I_{LOAD} ≤ 15µA			-5	mV
Line Regulation	2.6V ≤ V_{VCC} ≤ 5.5V			-2.3	mV/V
Quiescent Current	2.6V ≤ V_{VCC} ≤ 5.5V			18	µA
$\overline{SHDN3}$ Logic High Voltage	2.6V < V_{VCC} < 5.5V	1.6			V
$\overline{SHDN3}$ Logic Low Voltage	2.6V < V_{VCC} < 5.5V			0.6	V
$\overline{SHDN3}$ Current	V_{VCC} = 5.5V			1	µA

Note 2: Guaranteed by design, not production tested.
Note 3: $V_{TOUT} = (-4 \times 10^{-6}) \times (T^{2}°C) - (1.13 \times 10^{-2}) \times (T°C) + 1.8708V$.
Note 4: Linearized gain = V_{TOUT} = -11.64mV/°C + 1.8778V.
Note 5: Specifications to -40°C are guaranteed by design and not subject to production test.

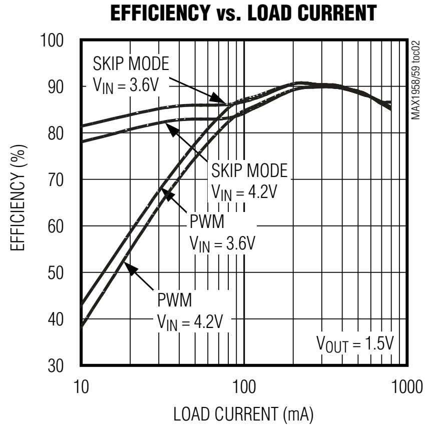
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

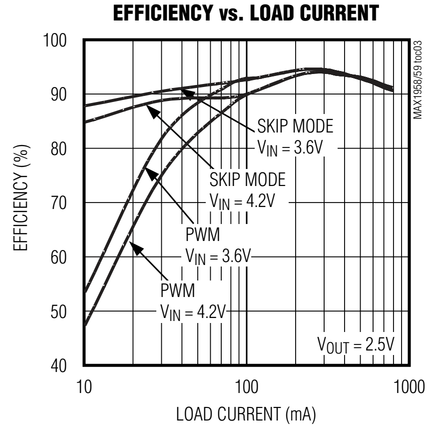
EFFICIENCY vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT



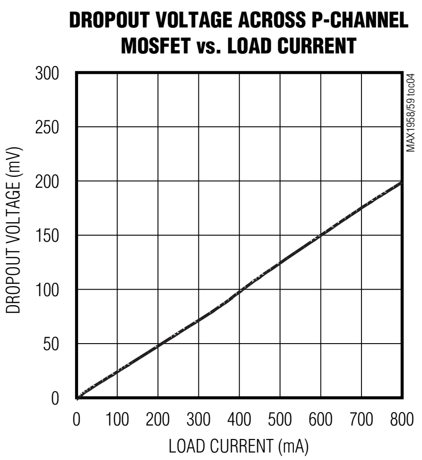
EFFICIENCY vs. LOAD CURRENT

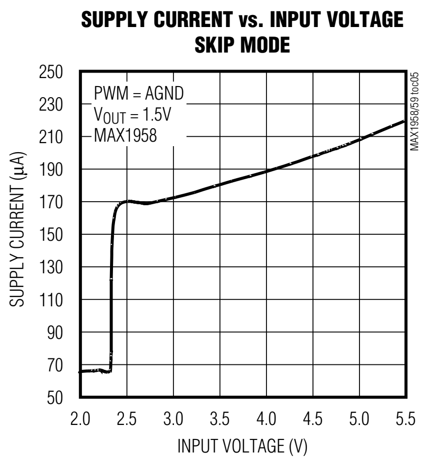


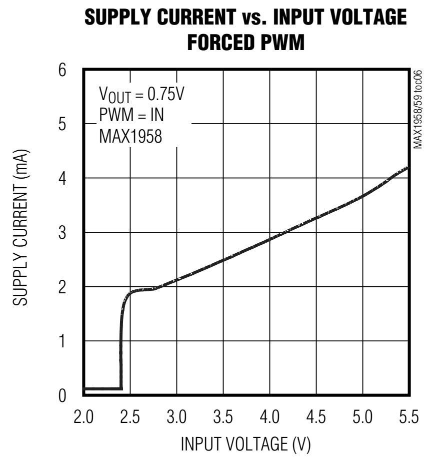
W-CDMA/N-CDMA Cellular Phone HBT PA Management ICs

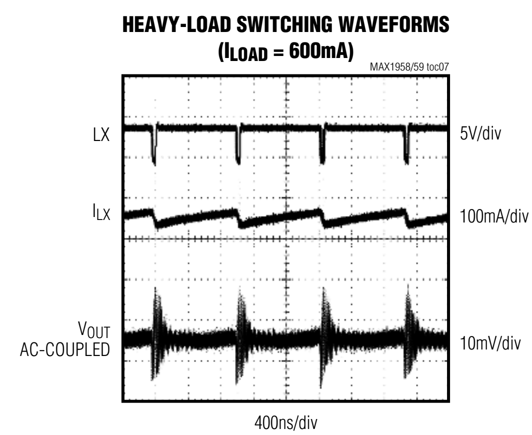
Typical Operating Characteristics (continued)

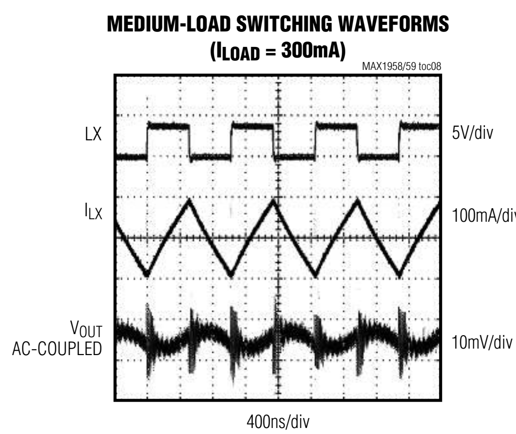
(T_A = +25°C, unless otherwise noted.)

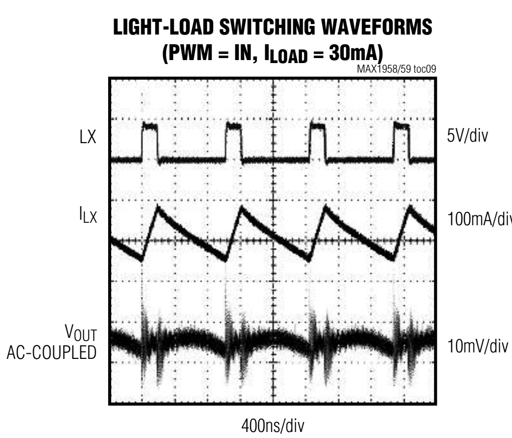


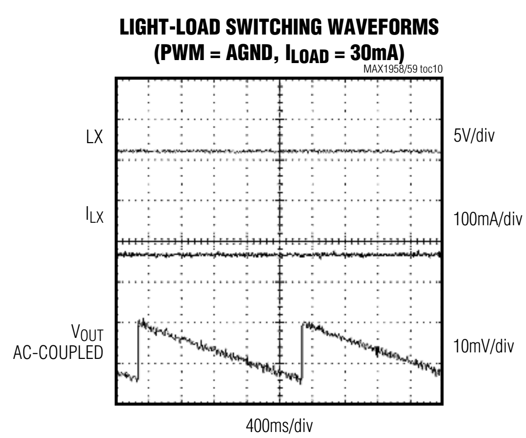






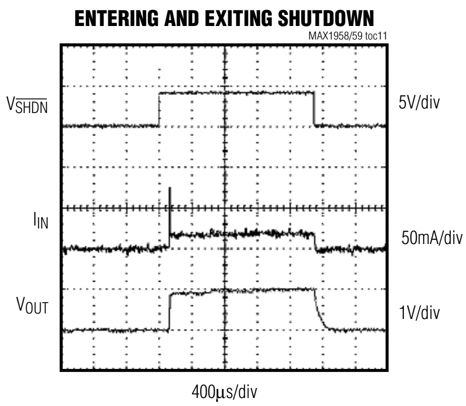


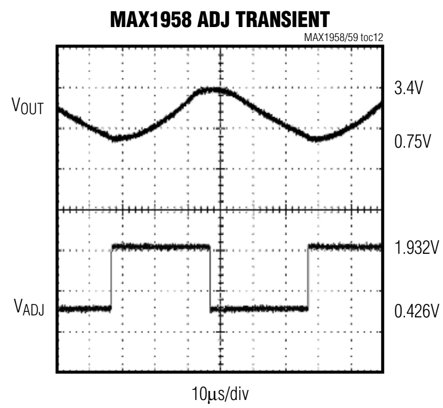


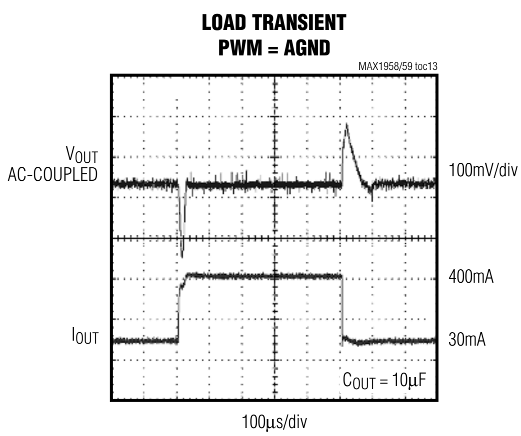


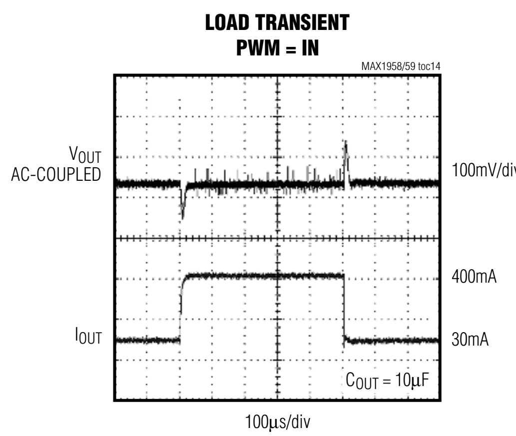
Typical Operating Characteristics (continued)

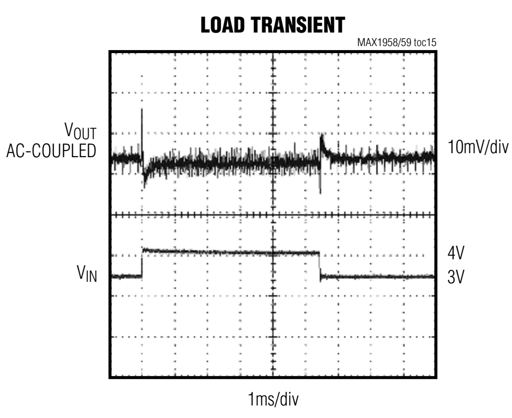
(T_A = +25°C, unless otherwise noted.)

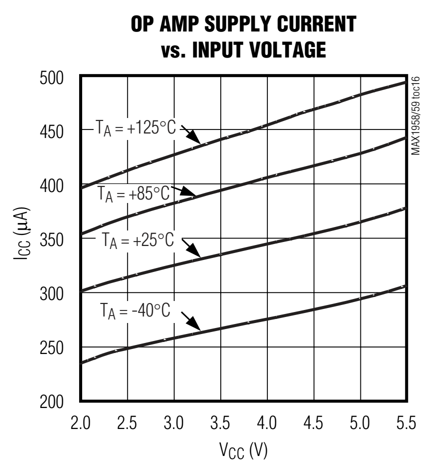






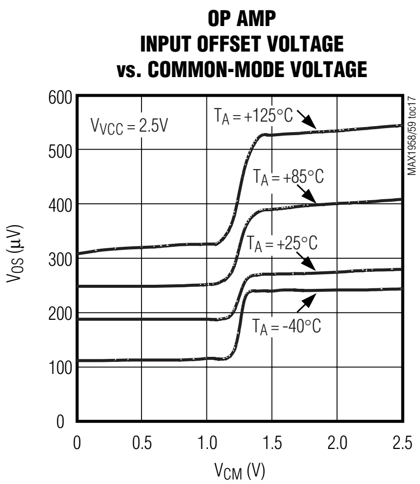


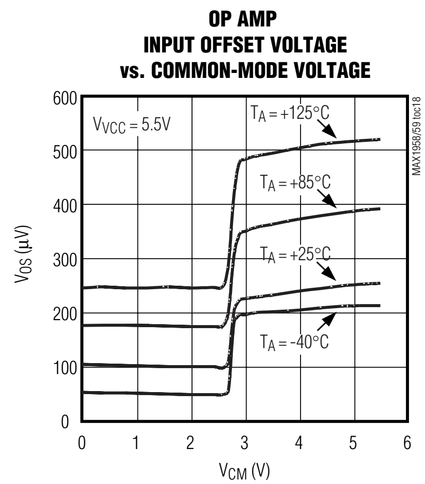


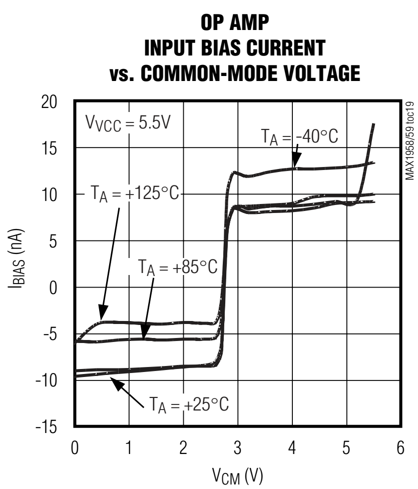


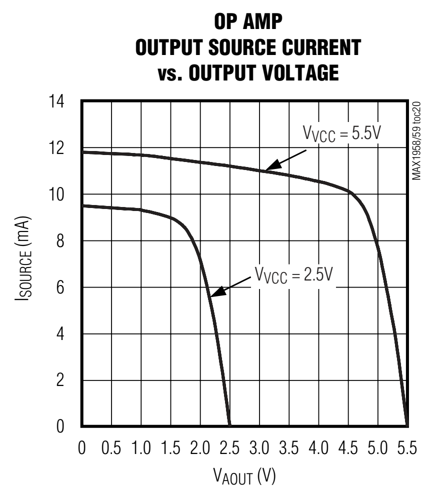
Typical Operating Characteristics (continued)

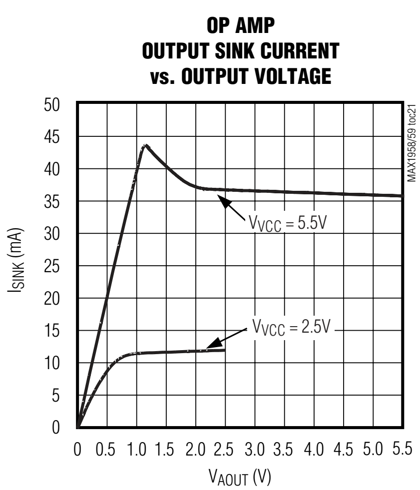
(T_A = +25°C, unless otherwise noted.)

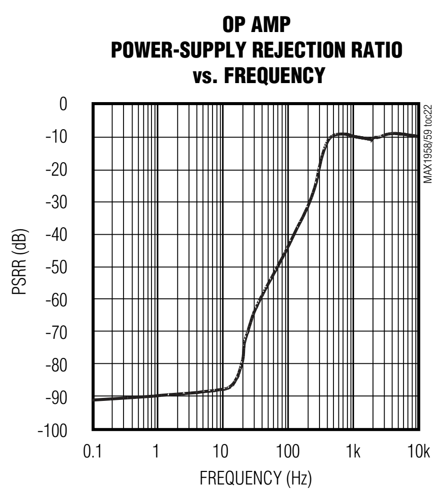








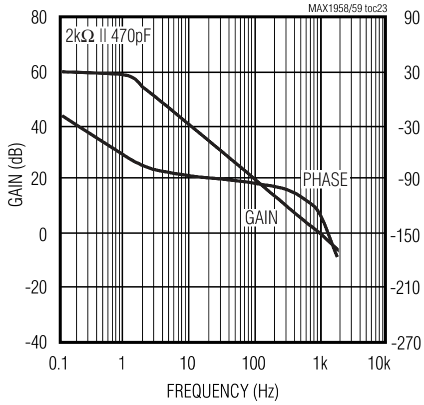




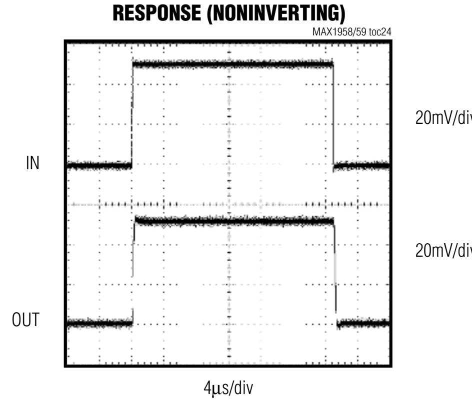
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

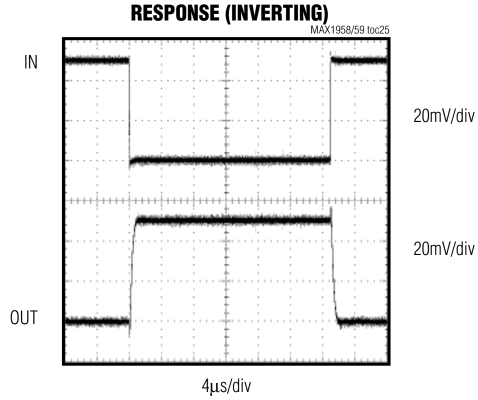
OP AMP GAIN AND PHASE vs. FREQUENCY



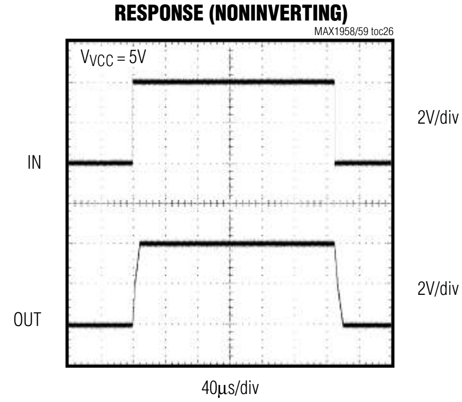
OP AMP SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



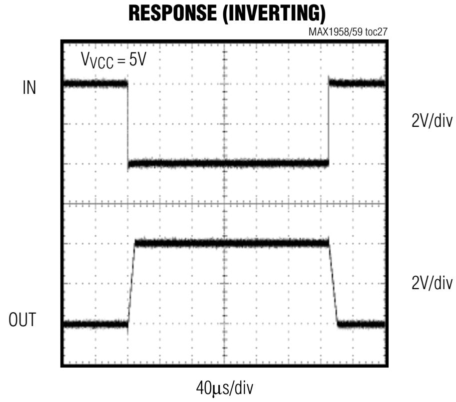
OP AMP SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



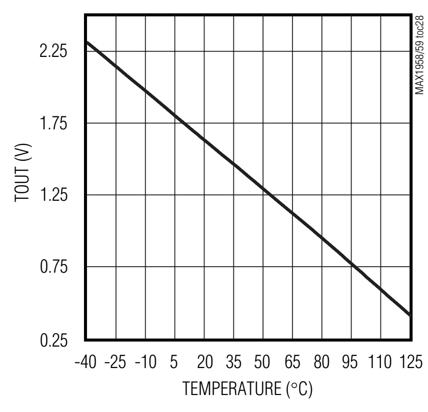
OP AMP LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



OP AMP LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



TEMPERATURE SENSOR TOUT VOLTAGE vs. TEMPERATURE



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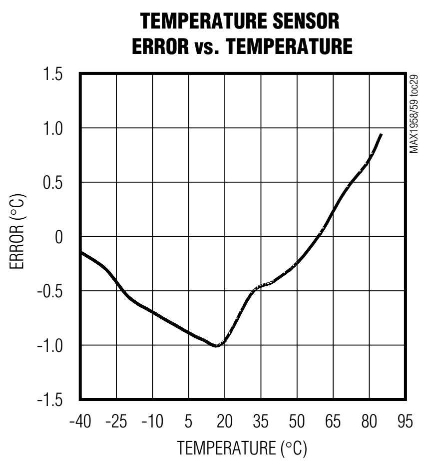
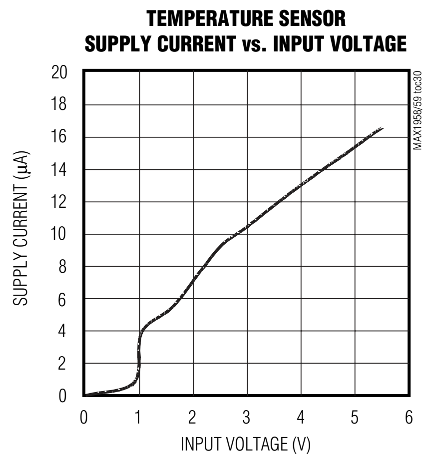
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	AOUT	Op-Amp Output. AOUT discharges to AGND during shutdown.
2	$\overline{SHDN2}$	Shutdown Control Input for the Op Amp. Drive to AGND to shut down the op amp. Connect to V_{CC} or drive high for normal operation.
3	AGND	Analog Ground. Ground for op amp, temperature sensor, and the precision circuits in the DC-to-DC regulator. Connect to pin 6.
4	TOUT	Analog Voltage Output Representing the Die Temperature. Bypass to AGND with a 0.01µF capacitor.
5	REF	Internal 1.25V Reference. Bypass to AGND with a 0.1µF capacitor.
6	AGND	Analog Ground. Connect to pin 3.
7	COMP	Compensation. Typically, connect a 22pF capacitor from COMP to AGND and a 9.1kΩ resistor and 560pF capacitor in series from COMP to AGND to stabilize the regulator (see the *Compensation and Stability* section).
8	ADJ	External Reference Input. Connect ADJ to the output of a D/A converter for dynamic adjustment of the regulator's output voltage. OUT regulates at (1.76 x V_{ADJ}) for the MAX1958 and (2 x V_{ADJ} - 0.8V) for the MAX1959.
9	$\overline{SHDN3}$	Shutdown Control Input for the Temperature Sensor. Drive to AGND to shut down the temperature sensor. Connect to V_{CC} or drive high for normal operation.
10	OUT	Output Voltage Feedback. Connect OUT directly to the output. OUT is high impedance during shutdown.
11	PGND	Power Ground for the DC-to-DC Converter
12	LX	Inductor Connection to the Internal Power MOSFETs
13	IN	Low-Current Supply Voltage Input. Connect to INP at the IC.

Pin Description (continued)

PIN	NAME	FUNCTION
14	INP	High-Current Supply Voltage Input. Connect to a 2.6V to 5.5V source. Bypass to PGND with a low-ESR 4.7µF capacitor. Connect to pin 16.
15	PWM	PWM/Skip-Mode Input. Drive low to use PWM mode at medium and heavy loads and pulse-skipping mode at light loads. Drive high to force PWM mode at all loads.
16	INP	Supply Voltage Input. Connect to pin 14.
17	$\overline{\text{SHDN1}}$	Shutdown Control Input for the Converter. Drive to AGND to shut down the converter. Connect to IN or drive high for normal operation.
18	V_{CC}	Supply Input for Op Amp and Temperature-Sensor Circuitry. Connect to INP through an RC filter.
19	IN+	Noninverting Input for the Op Amp
20	IN-	Inverting Input for the Op Amp
—	Exposed Paddle	Connect to Large AGND Plane. Internally connected to AGND.

Detailed Description

PWM Step-Down DC-to-DC Converter

The PWM step-down DC-to-DC converter is optimized for low-voltage, battery-powered applications where high efficiency and small size are priorities. It is specifically intended to power the linear HBT PA in N-CDMA/W-CDMA handsets. An analog control signal (ADJ) dynamically adjusts the converter's output voltage from 0.75V to 3.4V (MAX1958) or 1V to 3.6V (MAX1959) with a settling time of approximately 30µs. The MAX1958/MAX1959 operate at a high 1MHz switching frequency that reduces external component size. The IC contains an internal synchronous rectifier that increases efficiency and eliminates the need for an external Schottky diode. The normal operating mode uses constant-frequency PWM switching at medium and heavy loads and pulse skips at light loads to reduce supply current and extend battery life. An additional forced-PWM mode switches at a constant frequency, regardless of load, to provide a well-controlled noise spectrum for easier filtering in noise-sensitive applications. The MAX1958/MAX1959 are capable of 100% duty-cycle operation to increase efficiency in dropout. Battery life is maximized with a 0.1µA (typ) logic-controlled shutdown mode.

Normal-Mode Operation

Connecting PWM to GND enables PWM/pulse-skipping operation. This proprietary control scheme uses pulse-skipping mode at light loads to improve efficiency and reduce quiescent current to 190µA for the MAX1958 and 280µA for the MAX1959. With PWM/pulse-skipping mode enabled, the MAX1958/MAX1959 initiate pulse-skipping operation when the peak inductor current drops below 150mA. During pulse-skipping operation, switching occurs only as necessary to service the load, thereby reducing the switching frequency and associated losses in the internal switch, synchronous rectifier, and inductor.

During pulse-skipping operation, a switching cycle initiates when the error amplifier senses that the output voltage has dropped below the regulation point. If the output voltage is low, the high-side P-channel MOSFET switch turns on and conducts current through the inductor to the output filter capacitor and load. The PMOS switch turns off when the output voltage rises above the regulation point and the error amplifier is satisfied. The MAX1958/MAX1959 then wait until the error amplifier senses an out-of-regulation output voltage to start the cycle again.

At peak inductor currents above 150mA, the MAX1958/MAX1959 operate in PWM mode. During PWM operation, the output voltage is regulated by switching at a constant frequency and then modulating the power transferred to the load using the error comparator. The error amplifier output, the main switch current-sense signal, and the slope compensation ramp are all summed at the PWM comparator (see the *Functional Diagram*). The comparator modulates the output power by adjusting the peak inductor current during the first half of each cycle based on the output error voltage. The MAX1958/MAX1959 have relatively low AC loop gain coupled with a high-gain integrator to enable the use of a small, low-valued output filter capacitor. The resulting load regulation is ≤1.5% from 0

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to 600mA. Some jitter is normal during the transition from pulse-skipping mode to PWM mode with loads around 75mA. This has no adverse impact on regulation.

Forced-PWM Operation

To force PWM operation at all loads, connect PWM to IN. Forced-PWM operation is desirable in sensitive RF and data-acquisition applications to ensure that switching-noise harmonics are predictable and can be easily filtered. This is to ensure that the switching noise does not interfere with sensitive IF and data sampling frequencies. A minimum load is not required during forced-PWM operation because the synchronous rectifier passes reverse inductor current as needed to allow constant-frequency operation with no load. Forced-PWM operation has higher quiescent current than pulse-skipping mode (3mA typically compared to 190µA) due to continuous switching.

100% Duty-Cycle Operation

The maximum on-time can exceed one internal oscillator cycle, which permits operation at 100% duty cycle. As the input voltage drops, the duty cycle increases until the internal P-channel MOSFET stays on continuously. Dropout voltage at 100% duty cycle is the output current multiplied by the sum of the internal PMOS on-resistance (typically 0.25Ω) and the inductor resistance. Near dropout, cycles may be skipped, reducing switching frequency. However, voltage ripple remains small because the current ripple is still low.

Dropout

Dropout occurs when the desired output regulation voltage is higher than the input voltage minus the voltage drops in the circuit. In this situation, the duty cycle is 100%, so the high-side P-channel MOSFET is held on continuously and supplies current to the output up to the current limit. The output voltage in dropout falls to the input voltage minus the voltage drops. The largest voltage drops occur across the inductor and high-side MOSFET. The dropout voltage increases as the load current increases.

During dropout, the high-side, P-channel MOSFET turns on and the controller enters a low-current consumption mode. Every 6µs (six cycles), the MAX1958/MAX1959 check to see if the device is in dropout. The IC remains in this mode until it is no longer in dropout.

COMP Clamp

The MAX1958/MAX1959 compensation network has a 1V to 2.25V error-regulation range. The clamp optimizes transient response by preventing the voltage on COMP from rising too high or falling too low.

Undervoltage Lockout (UVLO)

The DC-to-DC converter portion of the MAX1958/MAX1959 is disabled if battery voltage on IN is below the UVLO threshold of 2.35V (typ). LX remains high impedance until the supply voltage exceeds the UVLO threshold. This guarantees the integrity of the output voltage and prevents excessive current during startup and as the battery supply drops in voltage during use. The op amp and temperature sensor are not connected to the UVLO and therefore continue to operate normally.

Synchronous Rectification

An N-channel synchronous rectifier operates during the second half of each switching cycle (off-time). When the inductor current falls below the N-channel current-comparator threshold or when the PWM reaches the end of the oscillator period, the synchronous rectifier turns off. This prevents reverse current flow from the output to the input in pulse-skipping mode. During PWM operation, small amounts of reverse current flow through the N-channel MOSFET during light loads. This allows regulation with a constant switching frequency and eliminates minimum load requirements for fixed-frequency operation. The N-channel reverse-current comparator threshold is -500mA. The N-channel zero-crossing threshold in pulse-skipping mode is 20mA (see the *Forced-PWM Operation* and *Normal-Mode Operation* sections)

Shutdown Mode

Driving $\overline{\text{SHDN1}}$ to ground puts the DC-to-DC converter into shutdown mode. In shutdown mode, the reference, control circuitry, internal-switching MOSFET, and synchronous rectifier turn off and the output (LX) becomes high impedance. Input current falls to 0.1µA (typ) during shutdown mode. Drive $\overline{\text{SHDN1}}$ high for normal operation.

Thermal Limit

The thermal limit is set at approximately +160°C and shuts down only the converter. In this state, both main MOSFETs are turned off. Once the IC cools by 15°C, the converter operates normally. A continuous overload condition results in a pulsed output. During thermal-limit conditions, the op amp and temperature sensor continue to operate.

Current-Sense Comparators

The IC uses several internal current-sense comparators. In PWM operation, the current-sense amplifier, combined with the PWM comparator, sets the cycle-by-cycle current limit and provides improved load and line response. This allows tighter specification of the inductor-saturation current limit to reduce inductor cost. A second 150mA current-sense comparator monitors the current through the P-channel switch and controls entry into pulse-skipping mode. A third current-sense comparator monitors current through the internal N-channel MOSFET to prevent excessive reverse currents and determines when to turn off the synchronous rectifier. A fourth comparator used at the P-channel MOSFET detects overcurrent. This protects the system, external components, and internal MOSFETs during overload conditions.

Rail-to-Rail Op Amp

The MAX1958/MAX1959 contain a rail-to-rail op amp that can be used to provide bias for the HBT PA. As the power needs of the PA change, the op amp can be used to dynamically change the bias point for the PA in order to optimize efficiency.

Rail-to-Rail Input Stage

The op amp in the MAX1958/MAX1959 has rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of composite NPN and PNP differential stages, which operate together to provide a common-mode range extending beyond both supply rails. The crossover region of these two pairs occurs halfway between VCL and AGND. The input offset voltage is typically ±400µV.

The MAX1958/MAX1959 op amp inputs are protected from large differential input voltages by internal 5.3kΩ series resistors and back-to-back triple-diode stacks across the inputs (Figure 1). For differential input voltages much less than 2.1V (three diode drops), input resistance is typically 4MΩ. For differential voltages greater than 2.1V, input resistance is around 10.6kΩ, and the input bias current can be approximated by the following equation:

$$I_{BIAS} = \frac{(V_{DIFF} - 2.1V)}{10.6k\Omega}$$

In the region where the differential input voltage increases to about 2.1V, the input resistance decreases exponentially from 4MΩ to 10.6kΩ as the diodes begin to conduct. It follows that the bias current increases with the same curve.

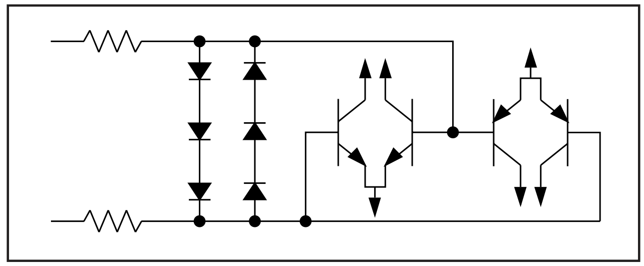

Figure 1. Input Protection Circuit

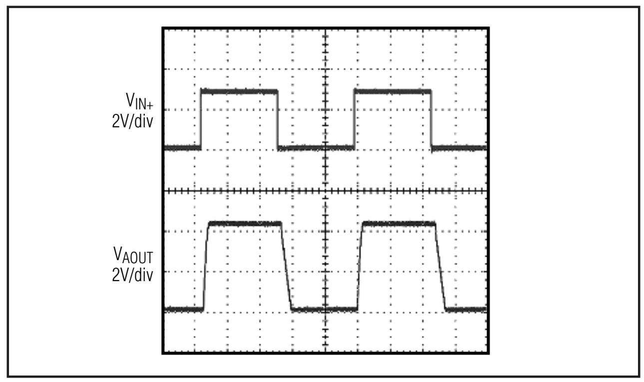

Figure 2. Op-Amp Output Voltage Swing

Rail-to-Rail Output Stage

The MAX1958/MAX1959 op amp can drive down to a 2kΩ load and still typically swing within 35mV of the supply rails. Figure 2 shows the output voltage swing of the MAX1958 configured with A_V = 1.57V/V and with V_{VCC} at 4.2V.

Temperature Sensor

The MAX1958/MAX1959 analog temperature sensor's output voltage is a linear function of its die temperature. The slope of the output voltage is approximately -11.64mV/°C and there is a 1.878V offset at 0°C to allow measurement of positive temperatures. The temperature sensor functions from -40°C to +125°C .The temperature error is less than ±2.5°C at temperatures from +25°C to +85°C.

Nonlinearity

The benefit of silicon analog temperature sensors over thermistors is the linearity over extended temperatures. The nonlinearity of the MAX1958/MAX1959 is typically ±0.4% over the 0°C to +85°C temperature range.

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Transfer Function

The temperature-to-voltage transfer function has an approximately linear negative slope and can be described by the following equation:

$$V_{TOUT} = -11.64\frac{mV}{°C} \times T + 1.878V$$

T is the die temperature in °C. Therefore:

$$T = \frac{V_{TOUT} - 1.878V}{-11.64mV/°C}$$

To account for the small amount of curvature in the transfer function, use the equation below to obtain a more accurate temperature reading:

$$V_{TOUT} = (-4 \times 10^{-6} \times T^2) + (-1.13 \times 10^{-2} \times T) + 1.8708V$$

Applications Information

PWM Step-Down DC-to-DC Converter

Setting the Output Voltage

The MAX1958/MAX1959 are optimized for highest system efficiency when applying power to a linear HBT PA in N-CDMA/W-CDMA handsets. The supply voltage to the PA is reduced (from 3.4V to as low as 0.75V for MAX1958) when transmitting at less than full power to greatly conserve supply current and extend battery life. The typical load profile for a W-CDMA PA can be seen in Figure 3. The MAX1958/MAX1959 dramatically reduce battery drain in these applications.

The MAX1958 output voltage is dynamically adjustable from 0.75V to 3.4V and MAX1959 output voltage is dynamically adjustable from 1V to 3.6V using the ADJ input. The input voltage cannot be lower than the output voltage. V_{OUT} can be adjusted during operation by driving ADJ with an external DAC. The output voltage for the MAX1958 is determined as:

$$V_{OUT} = 1.76 \times V_{ADJ}$$

The output voltage for the MAX1959 is determined as:

$$V_{OUT} = 2 \times V_{ADJ} - 0.8V$$

The MAX1958/MAX1959 output voltage responds to a full-scale change in voltage and current in approximately 30µs.

Compensation and Stability

The MAX1958/MAX1959 are externally compensated with a resistor and a capacitor (R_C and C_C, *Typical Application Circuit*) in series from COMP to AGND. An additional capacitor (C_f) is required from COMP to AGND. The capacitor, C_C, integrates the current from the transimpedance amplifier, averaging output capacitor ripple. This sets the device speed for transient response and allows the use of small ceramic output capacitors because the phase-shifted capacitor ripple does not disturb the current-regulation loop. The resistor, R_C, sets the proportional gain of the output error voltage by a factor of $g_m \times R_C$. Increasing this resistor also increases the sensitivity of the control loop to output ripple.

The series resistor and capacitor set a compensation zero that defines the system's transient response. The load creates a dynamic pole, shifting in frequency with changes in load. As the load decreases, the pole frequency decreases. System stability requires that the compensation zero must be placed to ensure adequate phase margin (at least 30° at unity gain). The following is a design procedure for the compensation network.

Select an appropriate converter bandwidth (f_C) to stabilize the system while maximizing transient response. This bandwidth should not exceed 1/10 of the switching frequency.

Calculate the compensation capacitor, C_C, based on this bandwidth:

$$C_C = \left(\frac{V_{OUT}}{I_{OUT(MAX)}}\right) \times \left(\frac{1}{R_{CS}}\right) \times \left(g_m \times \frac{R2}{R1 + R2}\right) \times \frac{1}{2\pi f_C}$$

Resistors R1 and R2 are internal to the MAX1958/MAX1959. For the MAX1958, use R1 = 95kΩ and R2 = 125kΩ as nominal values for calculations. For the MAX1959, use R1 = 125kΩ and R2 = 125kΩ as nominal values for calculations. $I_{OUT(MAX)}$ is the maximum output current, R_{CS} = 0.5V/A, and g_m = 250µS. Select the closest standard value C_C that gives an acceptable bandwidth.

Calculate the equivalent load impedance, R_L, by:

$$R_L = \frac{V_{OUT}}{I_{OUT(MAX)}}$$

Calculate the compensation resistance (R_C) to cancel out the dominant pole created by the output load and the output capacitance:

$$\frac{1}{2\pi \times R_L \times C_{OUT}} = \frac{1}{2\pi \times R_C \times C_C}$$

Solving for R_C gives:

$$R_C = \frac{R_L \times C_{OUT}}{C_C}$$

Calculate the high-frequency compensation pole to cancel the zero created by the output capacitor's equivalent series resistance (ESR):

$$\frac{1}{2\pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2\pi \times R_C \times C_f}$$

Solving for C_f gives:

$$Cf = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

Use the calculated value for C_f or 22pF, whichever is larger.

Inductor Selection

There are several parameters that must be examined when determining an optimum inductor value. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple current. A good compromise between size, efficiency, and cost is an LIR of 30%. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency (1MHz). Choose a standard-value inductor close to the calculated value. The exact inductor value is not critical and can be adjusted in order to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. For any area-restricted applications, find a low-core-loss inductor having the lowest possible DC resistance. Ferrite cores are often the best choice. The inductor's saturation current rating must exceed the expected peak inductor current (I_{PEAK}). Consult the inductor manufacturer for saturation current ratings. Determine I_{PEAK} as:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents are not required from the source.

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or organic) are preferred due to their resistance to power-up surge currents. I_{RMS} is calculated as follows:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure stability of the regulation control loop. The output capacitor must have low impedance at the switching frequency. An additional constraint on the output capacitor is load transients. If it is desired for the output voltage to swing from 0.75V to 3.4V in 30µs, the output capacitor should be approximately 4.7µF or less. Ceramic capacitors are recommended. The output ripple is approximately:

$$V_{RIPPLE} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{2\pi \times f_S \times C_{OUT}}\right)$$

See the *Compensation and Stability* section for a discussion of the influence of output capacitance and ESR on regulation control-loop stability.

Rail-to-Rail Op Amp

Shutdown Mode

The MAX1958/MAX1959 op amp (Figure 4) features a low-power shutdown mode. When $\overline{SHDN2}$ is pulled low, the supply current for the amplifier drops to 0.1µA, the amplifier is disabled, and the output is actively discharged to AGND with an internal 100Ω switch. Pulling $\overline{SHDN2}$ high enables the amplifier.

Due to the output leakage currents of three-state devices and the small internal pullup current for $\overline{SHDN2}$, do not leave $\overline{SHDN2}$ unconnected. Floating

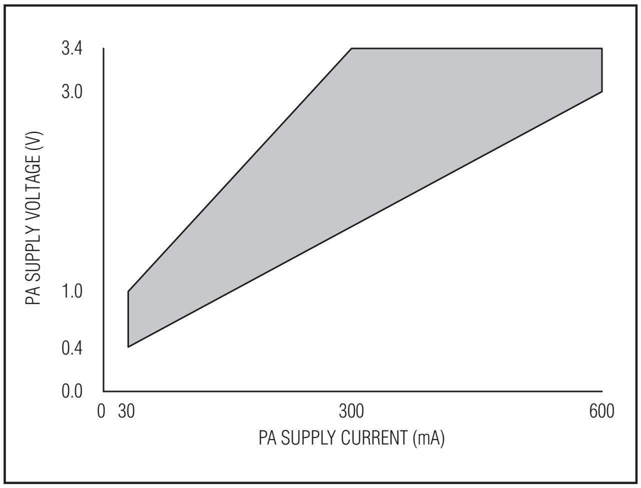


Figure 3. Typical W-CDMA Power Amplifier Load Profile

$\overline{SHDN2}$ may result in indeterminate logic levels, and could adversely affect op-amp operation.

Driving Capacitive Loads

The MAX1958/MAX1959 op amp is unity-gain stable for capacitive loads up to 470pF. Applications that require a greater capacitive drive capability should use an isolation resistor (R_{ISO}) between the output and the capacitive load (Figure 5). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage-divider with R_{LOAD}.

Power-Supply Bypass

The power-supply voltage applied to V_{CC} for the op amp and temperature sensor in the MAX1958/MAX1959 circuit is filtered from INP. Connect V_{CC} to INP through an RC network (R2 and C7 in Figure 4) to ensure a quiet power supply.

Temperature Sensor

The temperature sensor provides information about the MAX1958/MAX1959 die temperature. The voltage at TOUT (V_{TOUT}) is related to die temperature as follows:

$$V_{TOUT} = (-4 \times 10^{-6} \times T^2) + (-1.13 \times 10^{-2} \times T) + 1.8708V$$

For stable operation, bypass TOUT to AGND with at least a 0.01µF capacitor.

Temperature Sensor Error Due to Die Self-Heating

When the 800mA converter and the op amp are both operated at heavy load while the temperature sensor is enabled, the indicated temperature at TOUT deviates several degrees from the actual ambient temperature due to die self-heating effects. At light loads, when die self-heating is low, TOUT tends to be a good approximation of the ambient temperature. At heavier loads, the die self-heating is appreciable; TOUT gives a good approximation of the die temperature, which can be several degrees higher than the ambient temperature.

Sensing Circuit Board and Ambient Temperature

Temperature sensors like those found in the MAX1958/MAX1959 that sense their own die tempera-

Table 1. Recommended Inductors

MANUFACTURER	PART NO.	INDUCTANCE (µH)	DC RESISTANCE (mΩ)	RATED DC MAX CURRENT (mA)	DIMENSIONS L x W x H (mm)
800mA Application					
Sumida	CDRH3D16-4R7	4.7	80	900	3.8 x 3.8 x 1.8
Toko	972AS-4R7M = P5	4.7	220	960	4.6 x 4.6 x 1.2
700mA Application					
Sumida	CMD4D11-4R7	4.7	166	750	3.5 x 5.3 x 1.2
Toko	976AS-4R7 = P5	4.7	320	740	3.6 x 3.6 x 1.2
400mA Application					
Murata	LQH3C4R7M34	4.7	200	450	2.5 x 3.2 x 2
Sumida	CDRH2D11-4R7	4.7	170	500	3.2 x 3.2 x 1.2
300mA Application					
Murata	LQH1C4R7M04	4.7	650	0.34	1.6 x 3.2 x 2

***Note:** Efficiency may vary depending upon the inductor's characteristics. Consult the inductor manufacturer for saturation current ratings.*

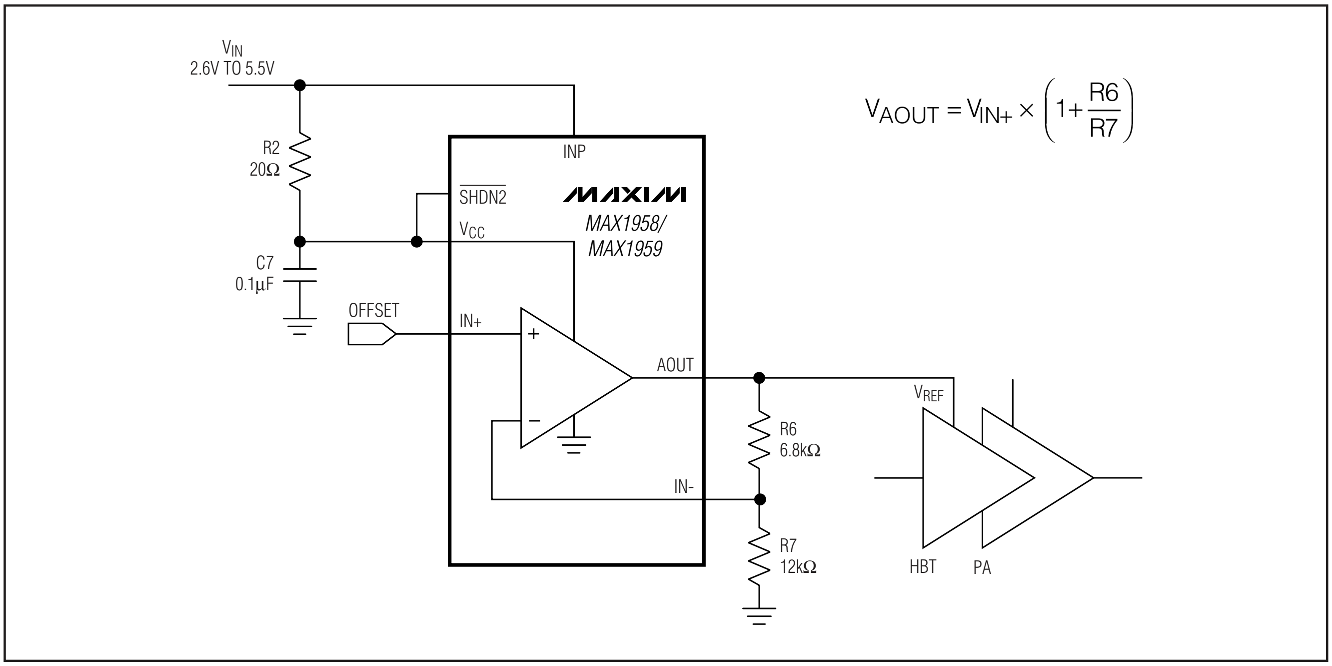


Figure 4. Op-Amp Configuration

tures must be mounted on, or close to, the object whose temperature they are intended to measure. There is a good thermal path between the exposed paddle of the package and the IC die; therefore, the MAX1958/MAX1959 can accurately measure the temperature of the circuit board to which they are soldered. If the sensor is intended to measure the temperature of a heat-generating component on the circuit board, it should be mounted as close as possible to that component and should share supply and ground traces (if they are not noisy) with that component where possible. This maximizes the heat transfer from the component to the sensor.

The thermal path between the plastic package and the die is not as good as the path through the exposed paddle, so the MAX1958/MAX1959, like all temperature sensors in plastic packages, are less sensitive to the temperature of the surrounding air than they are to the temperature of its exposed paddle. They can be successfully used to sense ambient temperature if the circuit board is designed to track the ambient temperature.

As with any IC, the wiring and circuits must be kept insulated and dry to avoid leakage and corrosion, especially if the part is operated at cold temperatures where condensation can occur.

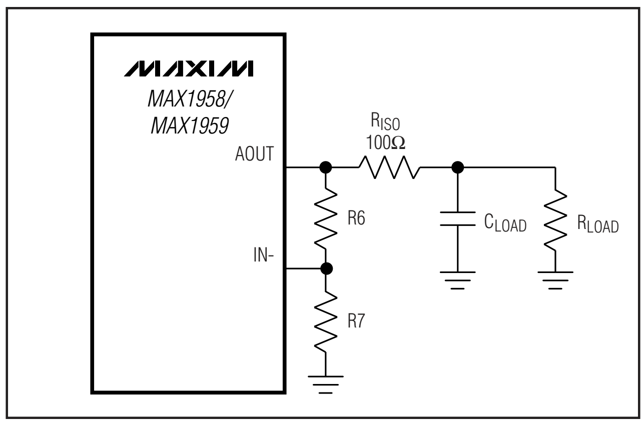


Figure 5. Configuration for Driving Larger Capacitive Loads

The junction-to-ambient thermal resistance (θ_{JA}) is the parameter used to calculate the rise of a device junction temperature (T_J) due to its power dissipation. The θ_{JA} for the 20-pin QFN package is +50°C/W. For the MAX1958/MAX1959, use the following equation to calculate the rise in die temperature:

$$T_J = T_A + \Theta_{JA} \times \left(P_{D(CONVERTER)} + P_{D(OPAMP)} + P_{D(TEMPSENSOR)}\right)$$

The power dissipated by the DC-to-DC converter dominates in this equation. It is then reasonable to assume

W-CDMA/N-CDMA Cellular Phone HBT PA Management ICs

that the rise in die temperature due to the converter is a good approximation of the total rise in die temperature. Therefore:

$$T_J \approx T_A + \Theta_{JA} \times \left(P_{D(CONVERTER)}\right) = T_A + \Theta_{JA} \times (V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT})$$

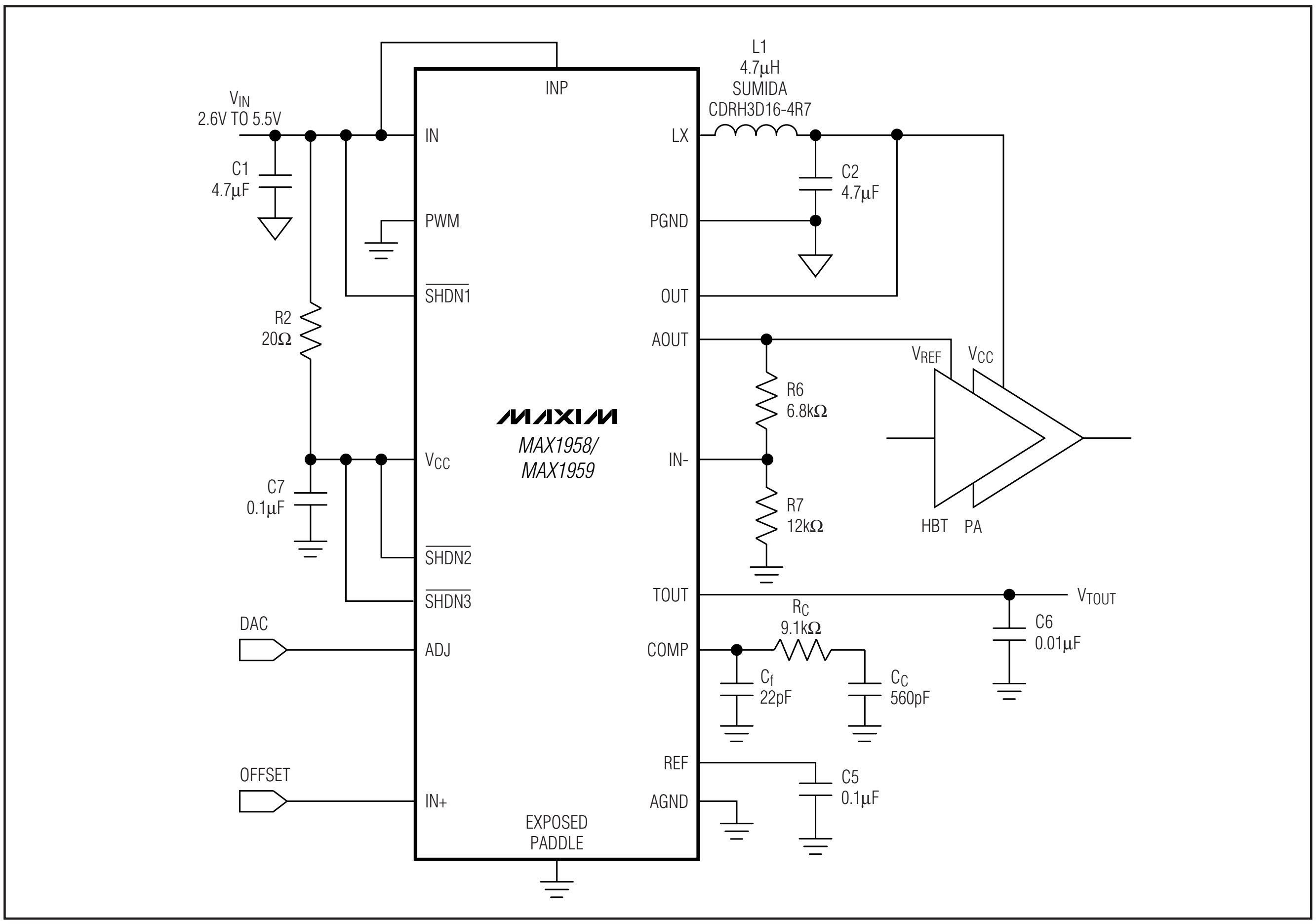
This equation assumes that the losses in the inductor are relatively small. For inductors with high DC resistance, inductor loss must be accounted for in the calculation. The temperature rise due to power dissipation by the converter can be quite significant.

PC Board Layout and Routing

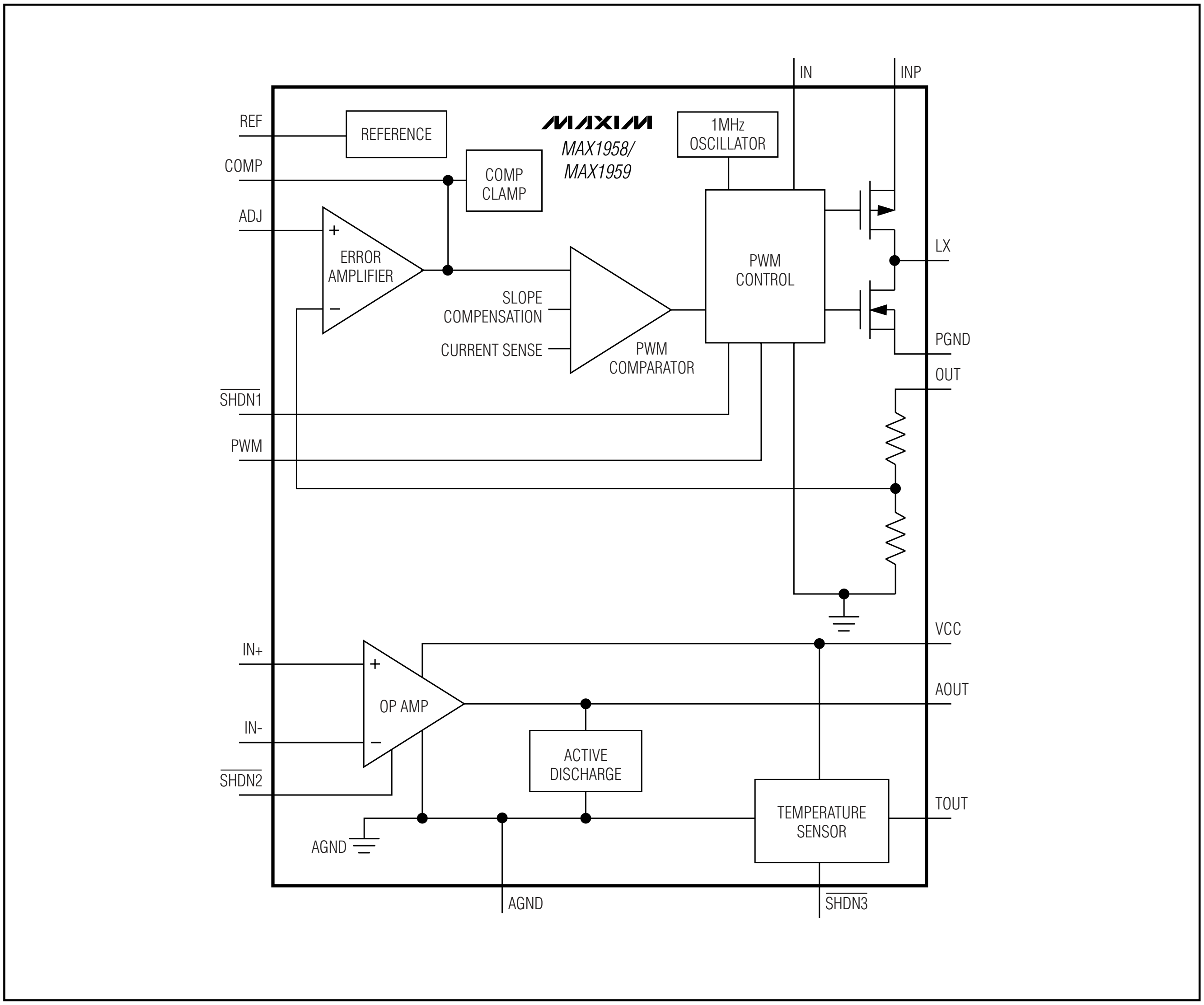
High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes EMI, noise on the feedback paths, and voltage gradients in the ground plane, all of which can cause instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible and keep their traces short, direct, and wide. Connect their ground pins at a single common node in a star ground configuration. Keep noisy traces, such as those from the LX pin, away from the output feedback network. Position the bypass capacitors as close as possible to their respective pins to minimize noise coupling. For optimum performance, place input and output capacitors as close to the device as possible. Connect AGND and PGND to the highest quality system ground. The MAX1958 evaluation kit illustrates an example PC board layout and routing scheme.

Optimize performance of the op amp by decreasing the amount of stray capacitance at the op amp's inputs and output. Decrease stray capacitance by placing external components as close to the device as possible to minimize trace lengths and widths.

Typical Operating Circuit



Functional Diagram



Chip Information

TRANSISTOR COUNT: 3704

PROCESS: BiCMOS

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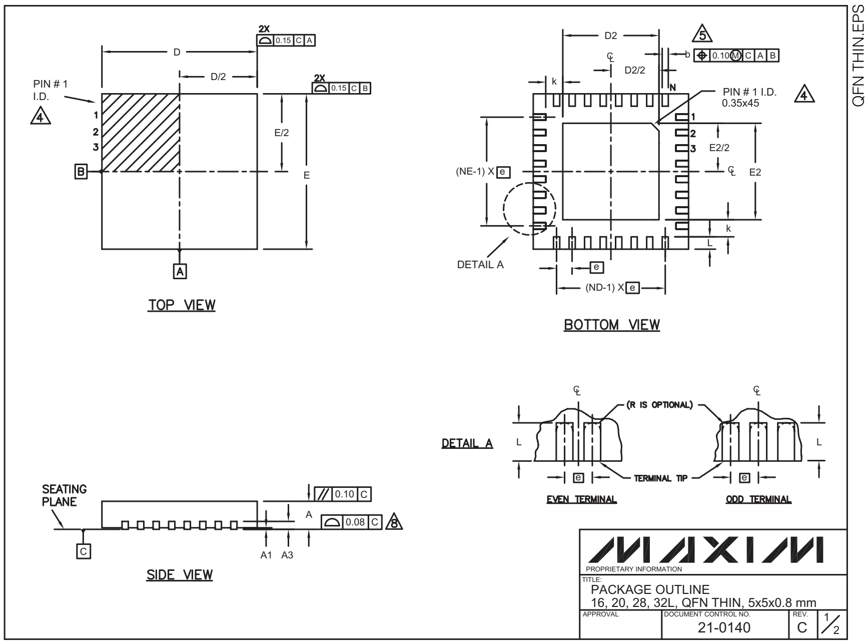
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 2/2

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