# ADS8319 16-Bit, 500-kSPS, Serial Interface, Micropower, Miniature, SAR Analog-to-Digital Converter

## 1 Features

- 500-kHz Sample Rate
- 16-Bit Resolution
- Zero Latency at Full Speed
- Unipolar, Single-Ended Input Range: 0 V to $V_{REF}$
- SPI-Compatible Serial Interface With Daisy-Chain Option
- Excellent Performance:
  - 93.6-dB SNR (Typical) at 10-kHz Input
  - –106-dB THD (Typical) at 10-kHz Input
  - ±1.5-LSB (Maximum) INL
  - ±1-LSB (Maximum) DNL
- Low Power Dissipation: 18 mW (Typical) at 500 kSPS
- Power Scales Linearly with Speed: 3.6 mW / 100 kSPS
- Power Dissipation During Power-Down State: 0.25 µW (Typical)
- 10-Pin VSSOP and VSON Packages

## 2 Applications

- Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation and Process Controls
- Medical Electronics
- Optical Networking

## 3 Description

The ADS8319 device is a 16-bit, 500-kSPS, analog-to-digital converter (ADC) that operates with a 2.25-V to 5.5-V external reference. The device includes a capacitor-based, successive-approximation register (SAR) ADC with inherent sample and hold.

The device includes a 50-MHz, SPI-compatible serial interface. The interface is designed to support daisy-chaining or cascading of multiple devices. Furthermore, a *Busy Indicator* makes synchronizing with the digital host easy.

The device unipolar, single-ended input range supports an input swing of 0 V to $+V_{REF}$.

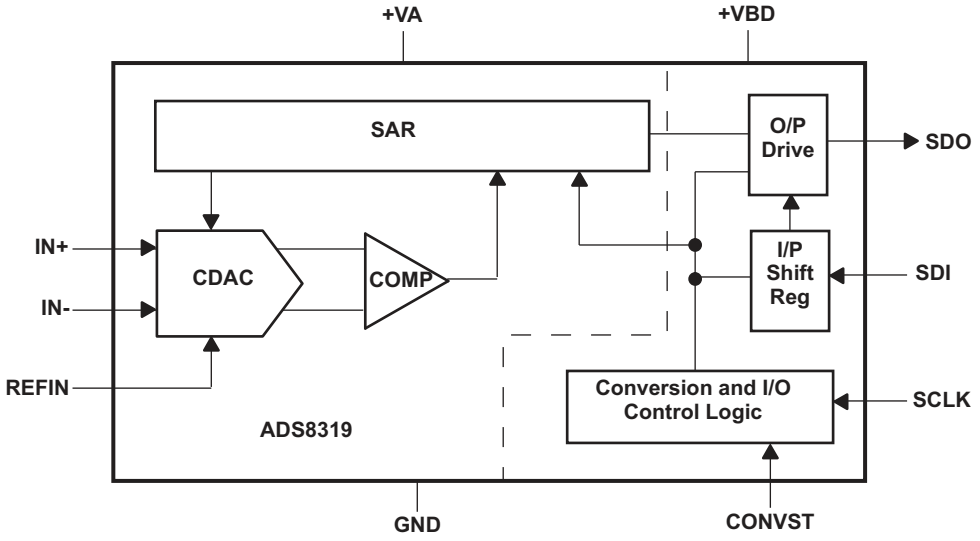
Device operation is optimized for very-low power operation and the power consumption directly scales with speed. This feature makes the device attractive for lower-speed applications. The device is available in 10-pin VSSOP and VSON packages.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADS8319 | VSSOP (10) | 3.00 mm × 3.00 mm |
| | VSON (10) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (December 2015) to Revision C** — **Page**

- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Functional Block Diagram*, *Application and Implementation* section, *Power Supply Recommendations* section, and *Layout* section ... 1
- Changed all references of MSOP to VSSOP ... 1
- Changed all references of SON to VSON ... 1
- Moved Operation temperature From: *Electrical Characteristics* table To: *Recommended Operating Conditions* table ... 4
- Changed Thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 180°C/W To: 107.5°C/W (VSSOP) and From: 70°C/W To: 87.2°C/W (VSON) ... 4

**Changes from Revision A (September 2013) to Revision B** — **Page**

- Deleted data from the Device Comparison Table this is repeated in the POA ... 3
- Changed External Reference Input, $V_{REF}$ parameter maximum specification ... 6
- Changed $V_{DD}$ to $+V_A$ in first sentence fo the *Reference* section ... 18
- Changed Figure 51: added +VBD to device SDI connection ... 21
- Changed Figure 57: changed device number for device blocks ... 24
- Changed Figure 58: changed SDO #2 trace ... 25
- Changed Figure 59: changed device number for device blocks ... 25
- Changed Figure 60: changed SDO #2 trace ... 26

**Changes from Original (May 2008) to Revision A** — **Page**

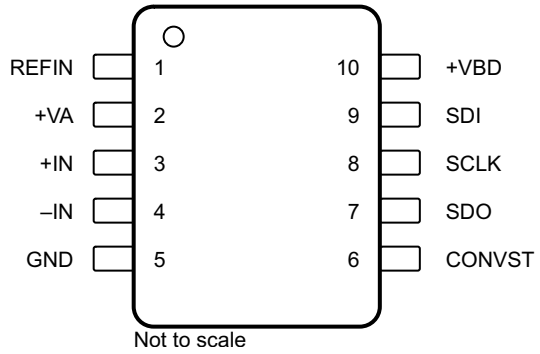
- Changed CBC to CEN in Ordering Information ... 3
- Changed CBE to CEP in Ordering Information ... 3

## 5 Device Comparison Table

| DEVICE | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES AT RESOLUTION (Bits) |
|---|---|---|---|
| ADS8319I | ±2.5 | 1.5, –1 | 16 |
| ADS8319IB | ±1.5 | ±1 | 16 |

## 6 Pin Configuration and Functions

**DGS Package**
**10-Pin VSSOP**
**Top View**

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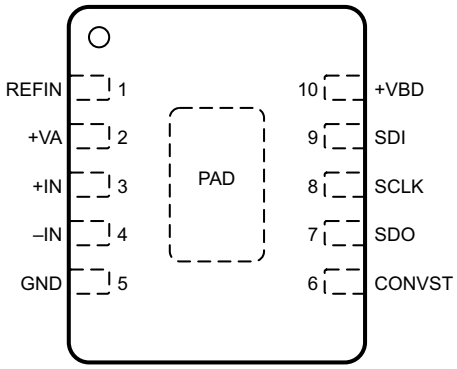
**DRC Package**
**10-Pin VSON With Exposed Thermal Pad**
**Top View**

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**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CONVST | 6 | Input | Convert input. CONVST also functions as the $\overline{CS}$ input in 3-wire interface mode. See *$\overline{CS}$ Mode* for more details. |
| GND | 5 | Power | Device ground. This pin is a common ground for both analog power supply (+VA) and digital I/O supply (+VBD). |
| +IN | 3 | Analog Input | Noninverting analog signal input |
| –IN | 4 | Analog Input | Inverting analog signal input. This input is limited to ±0.1 V and is typically grounded at the input decoupling capacitor. |
| REFIN | 1 | Analog Input | Reference (positive) input. Decouple to GND with a 0.1-µF bypass capacitor and a 10-µF storage capacitor. |
| SCLK | 8 | Input | Serial I/O clock input. Data (on the SDO output are synchronized with this clock. |
| SDO | 7 | Output | Serial data output |
| SDI | 9 | Input | Serial data input. The SDI level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode. See *$\overline{CS}$ Mode* for more details. |
| +VA | 2 | Power | Analog power supply. Decouple to GND. |
| +VBD | 10 | Power | Digital I/O power supply. Decouple to GND. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| +IN pin voltage | –0.3 | $+V_A$ + 0.3 | V |
| +IN pin current | | ±130 | mA |
| –IN pin voltage | –0.3 | 0.3 | V |
| –IN pin current | | ±130 | mA |
| +VA to AGND | –0.3 | 7 | V |
| +VBD to BDGND | –0.3 | 7 | V |
| Digital input voltage to GND | –0.3 | $+V_{BD}$ + 0.3 | V |
| Digital output to GND | –0.3 | $+V_{BD}$ + 0.3 | V |
| Maximum VSSOP reflow temperature(2) | | 260 | °C |
| Maximum VSON reflow temperature(2) | | 260 | °C |
| Operating free-air temperature, $T_A$ | –40 | 85 | °C |
| Junction temperature, $T_{J(MAX)}$ | | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The device is rated to MSL2 260°C, as per the JSTD-020 specification.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $+V_A$ | Analog power-supply voltage | 4.5 | 5 | 5.5 | V |
| $+V_{BD}$ | Digital I/O-supply voltage | 2.375 | 3.3 | 5.5 | V |
| $V_{REF}$ | Reference voltage | 2.25 | 4.096 | $+V_A$ + 0.1 | V |
| $T_A$ | Operating temperature | –40 | | 85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | ADS8319 | | UNIT |
|---|---|---|---|---|
| | | DGS (VSSOP) | DRC (VSON) | |
| | | 10 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 107.5 | 87.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.8 | 31.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 24.2 | 25.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.6 | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 24.4 | 29.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

$T_A$ = –40°C to 85°C, $+V_A$ = 5 V, $+V_{BD}$ = 5 V to 2.375 V, $V_{REF}$ = 4 V, and $f_{SAMPLE}$ = 500 kHz, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | | |
| | Full-scale input span(1) | +IN – (–IN) | | 0 | | $V_{REF}$ | V |
| | Operating input | +IN | | –0.1 | | $V_{REF}$ + 0.1 | V |
| | | –IN | | –0.1 | | 0.1 | |
| | Input capacitance | | | | 59 | | pF |
| | Input leakage current | During acquisition | | | 1000 | | pA |
| **SYSTEM PERFORMANCE** | | | | | | | |
| | Resolution | | | | 16 | | Bits |
| | No missing codes | | | 16 | | | Bits |
| INL | Integral linearity(2) | ADS8319I | | –2.5 | ±1.2 | 2.5 | LSB(3) |
| | | ADS8319IB | | –1.5 | ±1 | 1.5 | |
| DNL | Differential linearity | At 16-bit level | ADS8319I | –1 | ±0.65 | 1.5 | LSB |
| | | | ADS8319IB | –1 | ±0.5 | 1 | |
| $E_O$ | Offset error(4) | | | –1.5 | ±0.3 | 1.5 | mV |
| $E_G$ | Gain error | | | –0.03 | ±0.0045 | 0.03 | %FSR |
| CMRR | Common-mode rejection ratio | With common-mode input signal = 200 $mV_{PP}$ at 500 kHz | | | 78 | | dB |
| PSRR | Power-supply rejection ratio | At FFF0h output code | | | 80 | | dB |
| | Transition noise | | | | 0.5 | | LSB |
| **SAMPLING DYNAMICS** | | | | | | | |
| $t_{CONV}$ | Conversion time | $+V_{BD}$ = 5 V | | | | 1400 | ns |
| | | $+V_{BD}$ = 3 V | | | | 1400 | |
| | Acquisition time | $+V_{BD}$ = 5 V | | 600 | | | ns |
| | | $+V_{BD}$ = 3 V | | 600 | | | |
| | Maximum throughput rate with or without latency | | | | | 0.5 | MHz |
| | Aperture delay | | | | 2.5 | | ns |
| | Aperture jitter, RMS | | | | 6 | | ps |
| | Step response | Settling to 16-bit accuracy | | | 600 | | ns |
| | Overvoltage recovery | Settling to 16-bit accuracy | | | 600 | | ns |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| THD | Total harmonic distortion(5) | $V_{IN}$ 0.4 dB below FS at 1 kHz, $V_{REF}$ = 5 V | | | –111 | | dB |
| | | $V_{IN}$ 0.4 dB below FS at 10 kHz, $V_{REF}$ = 5 V | | | –106 | | |
| | | $V_{IN}$ 0.4 dB below FS at 100 kHz, $V_{REF}$ = 5 V | | | –89 | | |
| SNR | Signal-to-noise ratio | ADS8319IB, $V_{IN}$ 0.4 dB below FS at 1 kHz, $V_{REF}$ = 5 V | | 92 | | | dB |
| | | $V_{IN}$ 0.4 dB below FS at 1 kHz, $V_{REF}$ = 5 V | | | 93.9 | | |
| | | $V_{IN}$ 0.4 dB below FS at 10 kHz, $V_{REF}$ = 5 V | | | 93.6 | | |
| | | $V_{IN}$ 0.4 dB below FS at 100 kHz, $V_{REF}$ = 5 V | | | 92.2 | | |
| SINAD | Signal-to-noise + distortion | $V_{IN}$ 0.4 dB below FS at 1 kHz, $V_{REF}$ = 5 V | | | 93.8 | | dB |
| | | $V_{IN}$ 0.4 dB below FS at 10 kHz, $V_{REF}$ = 5 V | | | 93.4 | | |
| | | $V_{IN}$ 0.4 dB below FS at 100 kHz, $V_{REF}$ = 5 V | | | 87.4 | | |

(1) Ideal input span, does not include gain or offset error.
(2) This parameter is endpoint INL, not best fit.
(3) LSB means least significant bit.
(4) Measured relative to actual measured reference.
(5) Calculated on the first nine harmonics of the input frequency.

## Electrical Characteristics (continued)

$T_A$ = –40°C to 85°C, $+V_A$ = 5 V, $+V_{BD}$ = 5 V to 2.375 V, $V_{REF}$ = 4 V, and $f_{SAMPLE}$ = 500 kHz, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SFDR | Spurious-free dynamic range | $V_{IN}$ 0.4 dB below FS at 1 kHz, $V_{REF}$ = 5 V | | 113 | | dB |
| | | $V_{IN}$ 0.4 dB below FS at 10 kHz, $V_{REF}$ = 5 V | | 107 | | |
| | | $V_{IN}$ 0.4 dB below FS at 100 kHz, $V_{REF}$ = 5 V | | 90 | | |
| | –3-dB small-signal bandwidth | | | 15 | | MHz |
| **EXTERNAL REFERENCE INPUT** | | | | | | |
| $V_{REF}$ | Reference input | | 2.25 | 4.096 | $+V_A$ + 0.1 | V |
| | Reference input current (6) | During conversion | | 250 | | µA |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| | Power-supply voltage | +VBD | 2.375 | 3.3 | 5.5 | V |
| | | +VA | 4.5 | 5 | 5.5 | |
| | Supply current | +VA, 500-kHz sample rate | | 3.6 | 4.5 | mA |
| $P_{VA}$ | Power dissipation | $+V_A$ = 5 V, 500-kHz sample rate | | 18 | 22.5 | mW |
| $IVA_{pd}$ | Device power-down current (7) | $+V_A$ = 5 V | | 50 | 300 | nA |
| **LOGIC FAMILY CMOS** | | | | | | |
| $V_{IH}$ | Input HIGH logic level | $I_{IH}$ = 5 µA | +(0.7 × $V_{BD}$) | | $+V_{BD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW logic level | $I_{IL}$ = 5 µA | –0.3 | | +(0.3 × $V_{BD}$) | |
| $V_{OH}$ | Output HIGH logic level | $I_{OH}$ = 2 TTL loads | $+V_{BD}$ – 0.3 | | $+V_{BD}$ | |
| $V_{OL}$ | Output LOW logic level | $I_{OL}$ = 2 TTL loads | 0 | | 0.4 | |

(6) Can vary by ±20%.
(7) The device automatically enters a power-down state at the end of every conversion and remains in a power-down state during the acquisition phase.

## 7.6 Timing Requirements: +VBD ≥ 4.5 V

All specifications are typical at –40°C to 85°C, $+V_A$ = 5 V, and $+V_{BD}$ ≥ 4.5 V, unless otherwise noted.

| | | REFERENCE FIGURE | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **SAMPLING AND CONVERSION RELATED** | | | | | |
| $t_{ACQ}$ | Acquisition time | Figure 50, Figure 52, Figure 53, Figure 55 | 600 | | ns |
| $t_{cnv}$ | Conversion time | | | 1400 | ns |
| $t_{cyc}$ | Time between conversions | | 2000 | | ns |
| $t_1$ | Pulse duration, CONVST high | Figure 50, Figure 52 | 10 | | ns |
| $t_6$ | Pulse duration, CONVST low | Figure 53, Figure 55, Figure 58 | 20 | | ns |
| **I/O RELATED** | | | | | |
| $t_{clk}$ | SCLK period | Figure 50, Figure 52, Figure 53, Figure 55, Figure 58, Figure 60 | 20 | | ns |
| $t_{clkl}$ | SCLK low time | | 9 | | ns |
| $t_{clkh}$ | SCLK high time | | 9 | | ns |
| $t_2$ | SCLK falling edge to data remains valid | | 5 | | ns |
| $t_3$ | SCLK falling edge to next data valid delay | | | 16 | ns |
| $t_{en}$ | Enable time, CONVST or SDI low to MSB valid | Figure 50, Figure 53 | | 15 | ns |
| $t_{dis}$ | Disable time, CONVST or SDI high or last SCLK falling edge to SDO 3-state ($\overline{CS}$ mode) | Figure 50, Figure 52, Figure 53, Figure 55 | | 12 | ns |
| $t_4$ | Setup time, SDI valid to CONVST rising edge | Figure 53, Figure 55 | 5 | | ns |
| $t_5$ | Hold time, SDI valid from CONVST rising edge | | 5 | | ns |
| $t_7$ | Setup time, SCLK valid to CONVST rising edge | Figure 58 | 5 | | ns |
| $t_8$ | Hold time, SCLK valid from CONVST rising edge | | 5 | | ns |

## 7.7 Timing Requirements: 4.5 V > +VBD ≥ 2.375 V

All specifications are typical at –40°C to 85°C, $+V_A$ = 5 V, and +4.5 V > $+V_{BD}$ ≥ 2.375 V, unless otherwise noted.

| | | REFERENCE FIGURE | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **SAMPLING AND CONVERSION RELATED** | | | | | |
| $t_{ACQ}$ | Acquisition time | Figure 50, Figure 52, Figure 53, Figure 55 | 600 | | ns |
| $t_{cnv}$ | Conversion time | | | 1400 | ns |
| $t_{cyc}$ | Time between conversions | | 2000 | | ns |
| $t_1$ | Pulse width CONVST high | Figure 50, Figure 52 | 10 | | ns |
| $t_6$ | Pulse width CONVST low | Figure 53, Figure 55, Figure 58 | 20 | | ns |
| **I/O RELATED** | | | | | |
| $t_{clk}$ | SCLK period | Figure 50, Figure 52, Figure 53, Figure 55, Figure 58, Figure 60 | 30 | | ns |
| $t_{clkl}$ | SCLK low time | | 13 | | ns |
| $t_{clkh}$ | SCLK high time | | 13 | | ns |
| $t_2$ | SCLK falling edge to data remains valid | | 5 | | ns |
| $t_3$ | SCLK falling edge to next data valid delay | | | 24 | ns |
| $t_{en}$ | CONVST or SDI low to MSB valid | Figure 50, Figure 53 | | 22 | ns |
| $t_{dis}$ | CONVST or SDI high or last SCLK falling edge to SDO 3-state ($\overline{CS}$ mode) | Figure 50, Figure 52, Figure 53, Figure 55 | | 15 | ns |
| $t_4$ | SDI valid setup time to CONVST rising edge | Figure 53, Figure 55 | 5 | | ns |
| $t_5$ | SDI valid hold time from CONVST rising edge | | 5 | | ns |
| $t_7$ | SCLK valid setup time to CONVST rising edge | Figure 58 | 5 | | ns |
| $t_8$ | SCLK valid hold time from CONVST rising edge | | 5 | | ns |

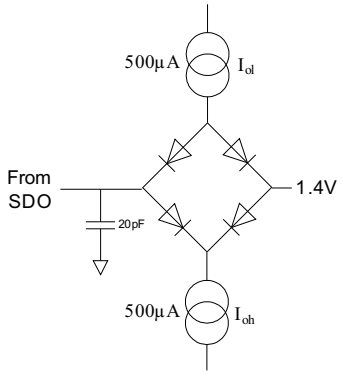



**Figure 1. Load Circuit for Digital Interface Timing**

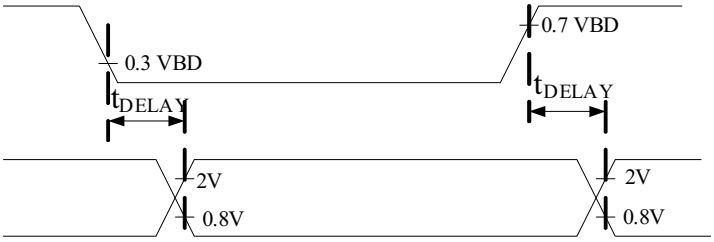



**Figure 2. Voltage Levels for Timing**

## 7.8 Typical Characteristics

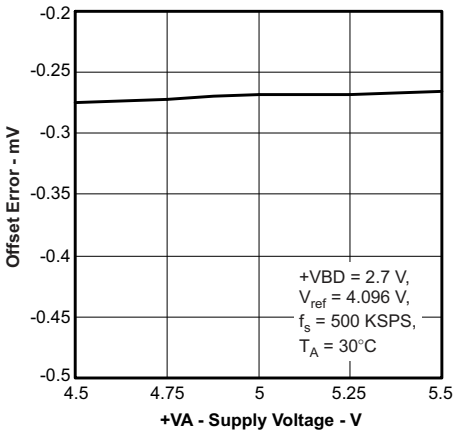



**Figure 3. Offset Error vs Supply Voltage**

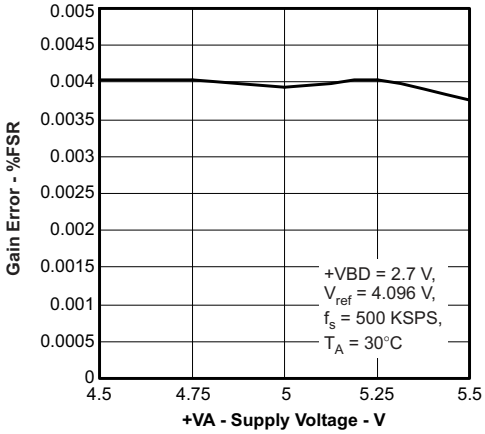



**Figure 4. Gain Error vs Supply Voltage**

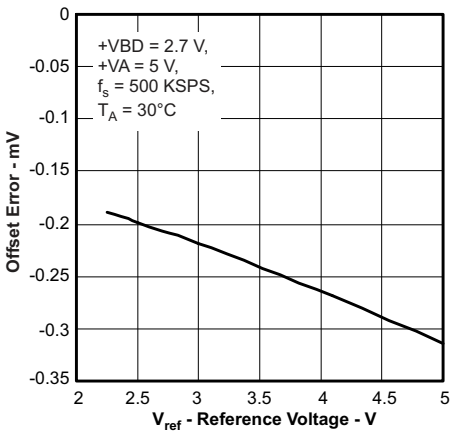



**Figure 5. Offset Error vs Reference Voltage**

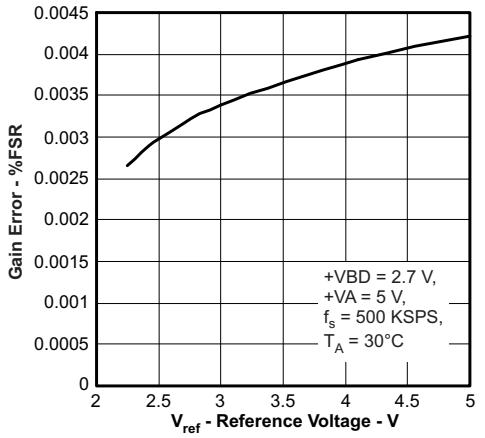



**Figure 6. Gain Error vs Reference Voltage**

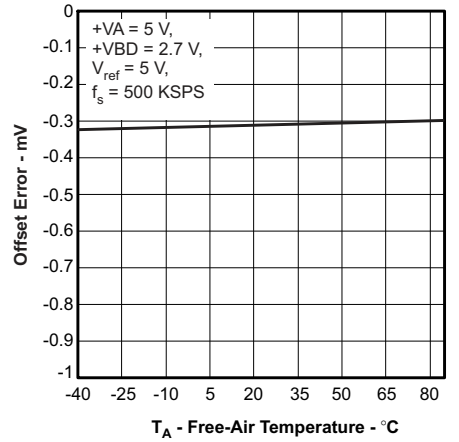



**Figure 7. Offset Error vs Free-Air Temperature**

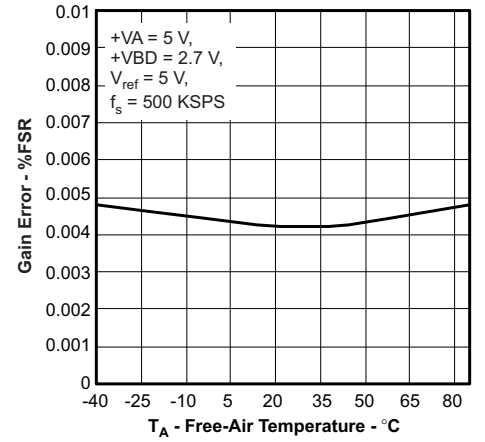



**Figure 8. Gain Error vs Free-Air Temperature**

## Typical Characteristics (continued)

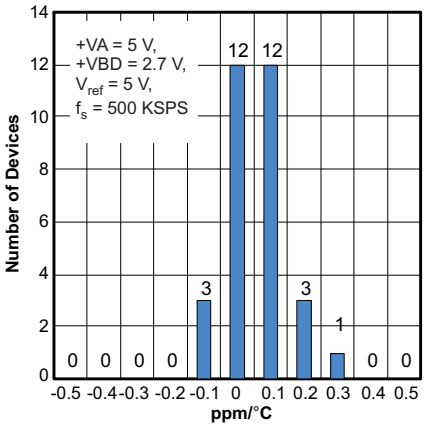



**Figure 9. Gain Error Drift Histogram**

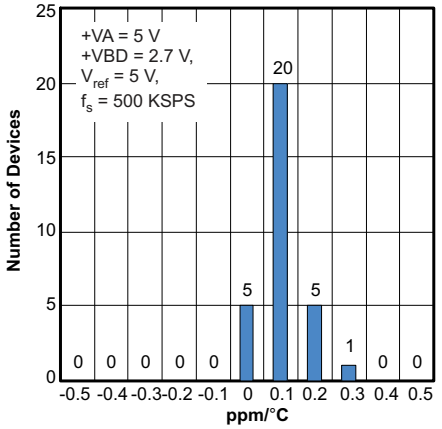



**Figure 10. Offset Error Drift Histogram**

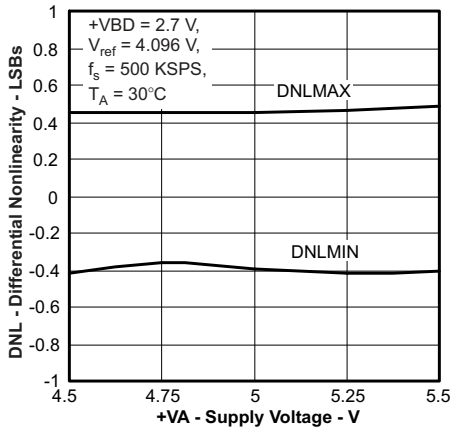



**Figure 11. Differential Nonlinearity vs Supply Voltage**

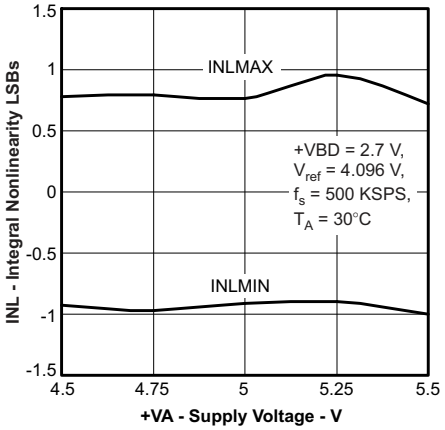



**Figure 12. Integral Nonlinearity vs Supply Voltage**

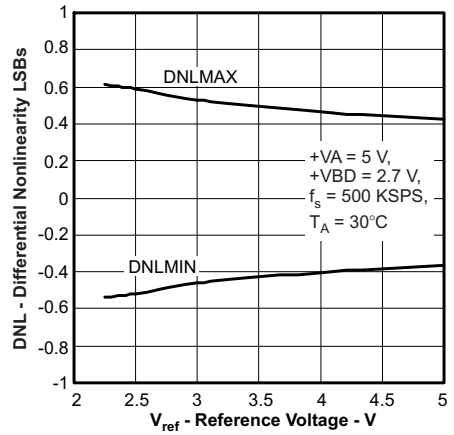



**Figure 13. Differential Nonlinearity vs Reference Voltage**

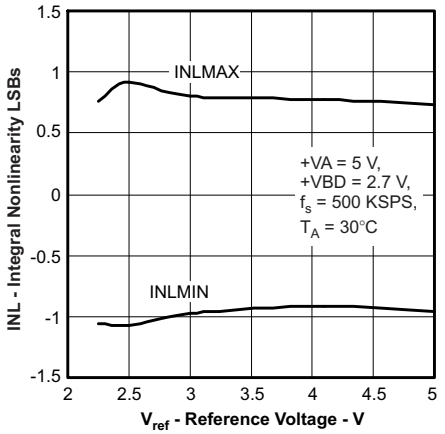



**Figure 14. Integral Nonlinearity vs Reference Voltage**

## Typical Characteristics (continued)

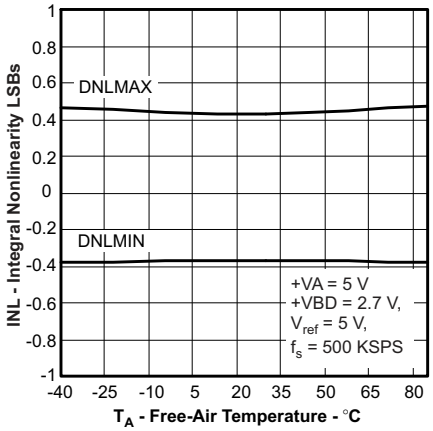



**Figure 15. Differential Nonlinearity vs Free-Air Temperature**

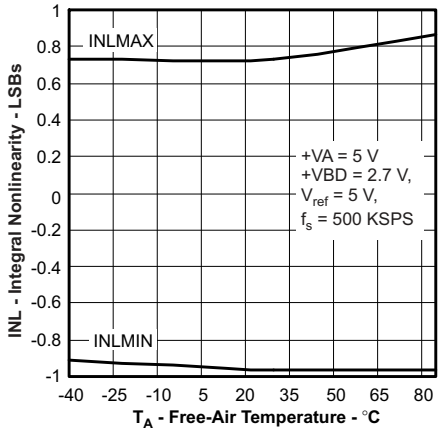



**Figure 16. Integral Nonlinearity vs Free-Air Temperature**

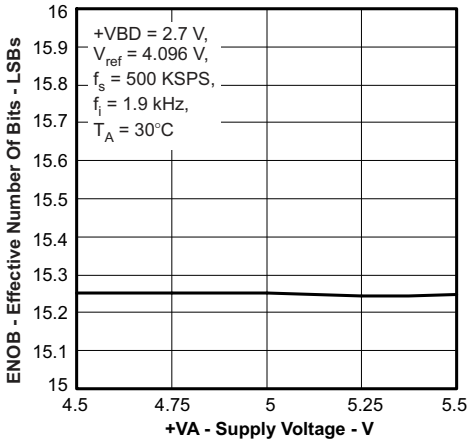



**Figure 17. Effective Number of Bits vs Supply Voltage**

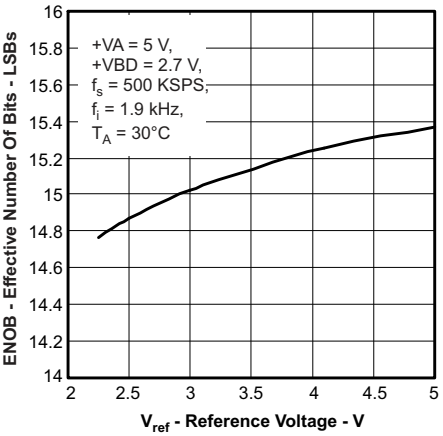



**Figure 18. Effective Number of Bits vs Reference Voltage**

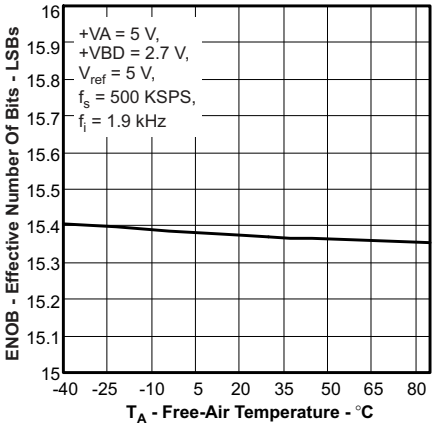



**Figure 19. Effective Number of Bits vs Free-Air Temperature**

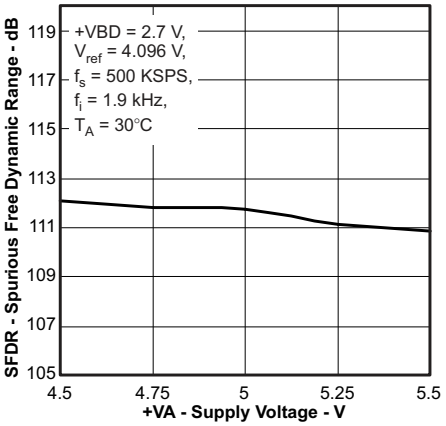



**Figure 20. Spurious-Free Dynamic Range vs Supply Voltage**

## Typical Characteristics (continued)

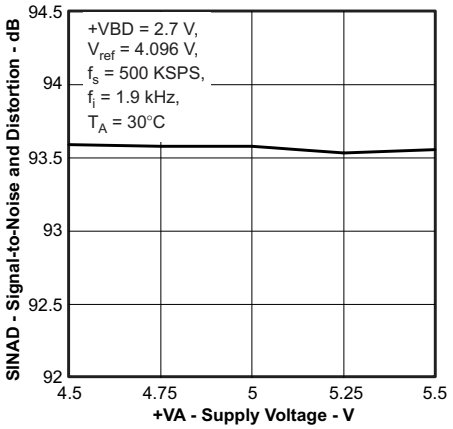



**Figure 21. Signal-to-Noise + Distortion vs Supply Voltage**

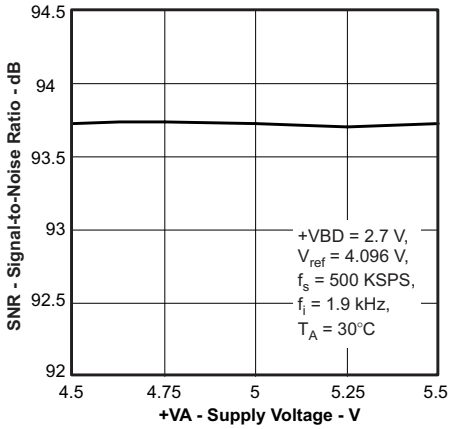



**Figure 22. Signal-to-Noise Ratio vs Supply Voltage**

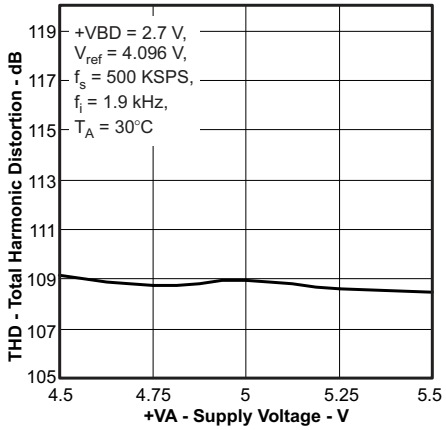



**Figure 23. Total Harmonic Distortion vs Supply Voltage**

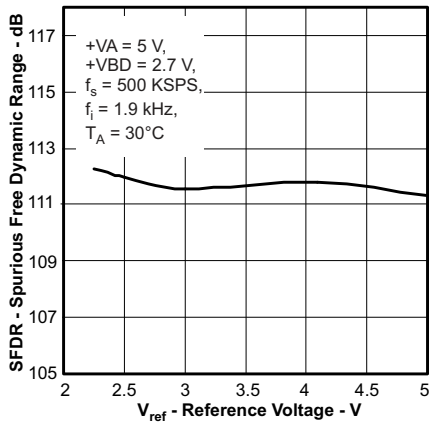



**Figure 24. Spurious-Free Dynamic Range vs Reference Voltage**

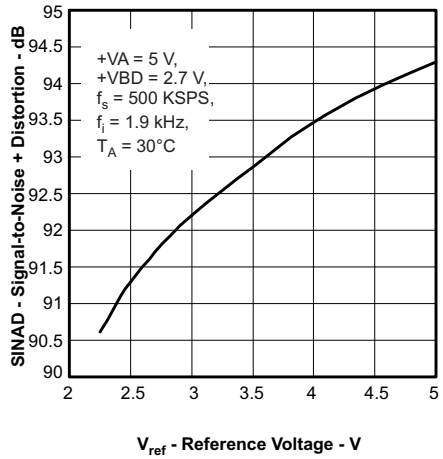



**Figure 25. Signal-to-Noise + Distortion vs Reference Voltage**

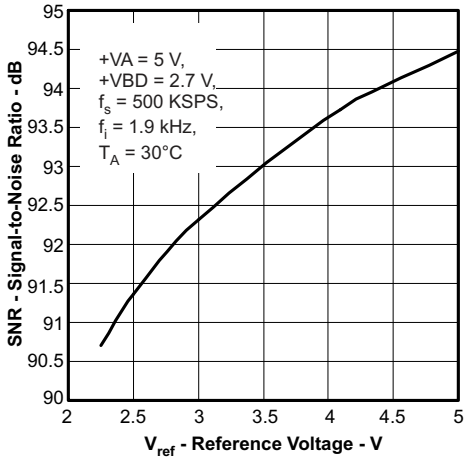



**Figure 26. Signal-to-Noise Ratio vs Reference Voltage**

## Typical Characteristics (continued)

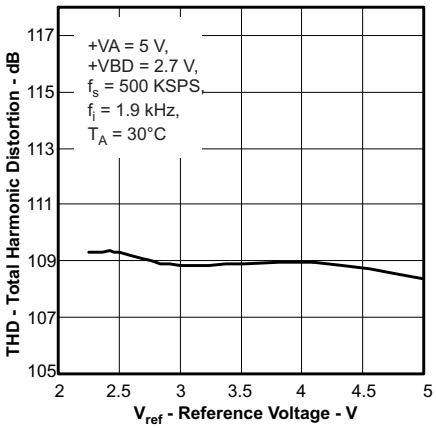



**Figure 27. Total Harmonic Distortion vs Reference Voltage**

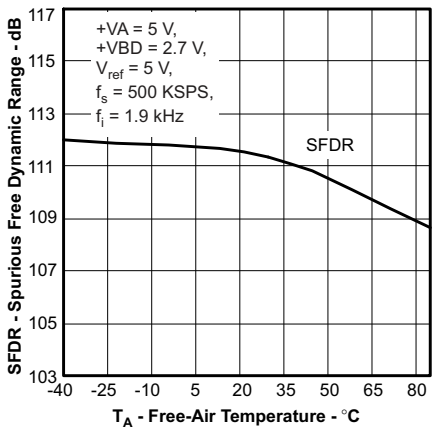



**Figure 28. Spurious-Free Dynamic Range vs Free-Air Temperature**

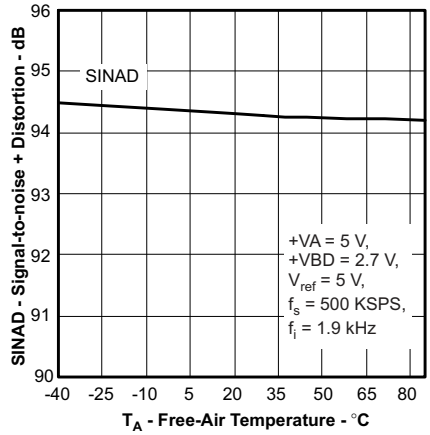



**Figure 29. Signal-to-Noise + Distortion vs Free-Air Temperature**

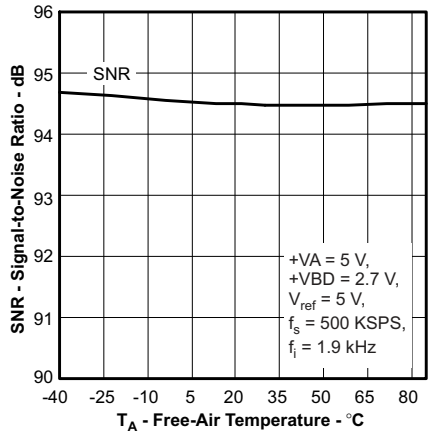



**Figure 30. Signal-to-Noise Ratio vs Free-Air Temperature**

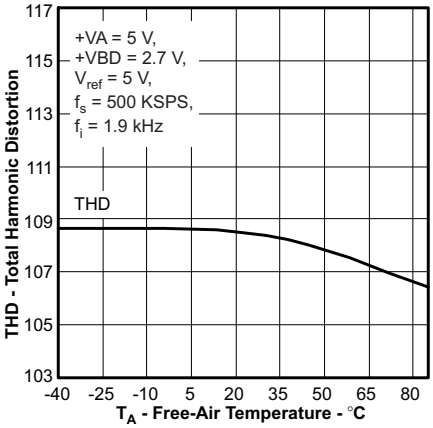



**Figure 31. Total Harmonic Distortion vs Free-Air Temperature**

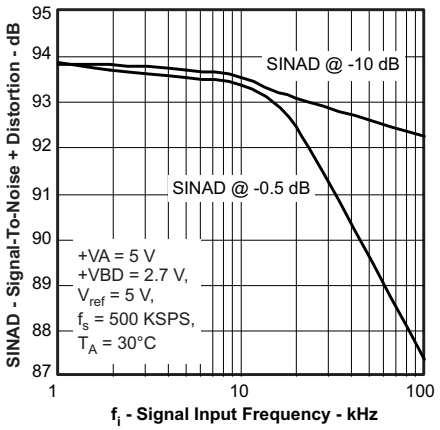



**Figure 32. Signal-to-Noise + Distortion vs Signal Input Frequency**

## Typical Characteristics (continued)

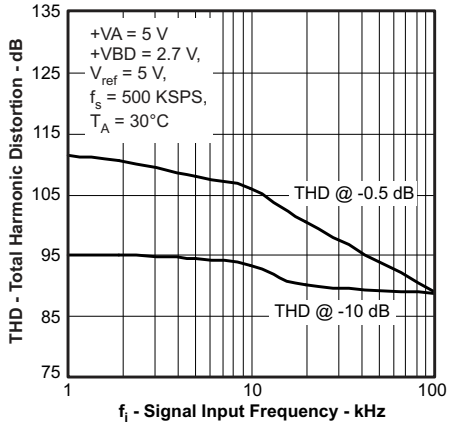



**Figure 33. Total Harmonic Distortion vs Signal Input Frequency**

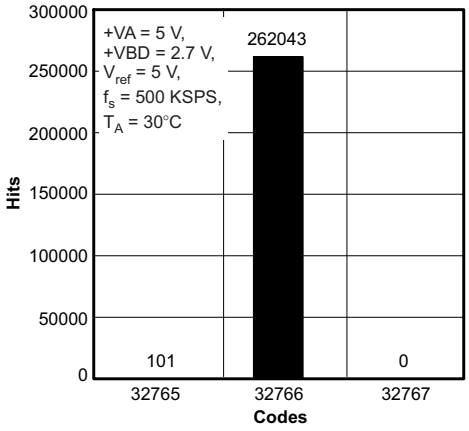



**Figure 34. DC Histogram of ADC Close to Center Code**

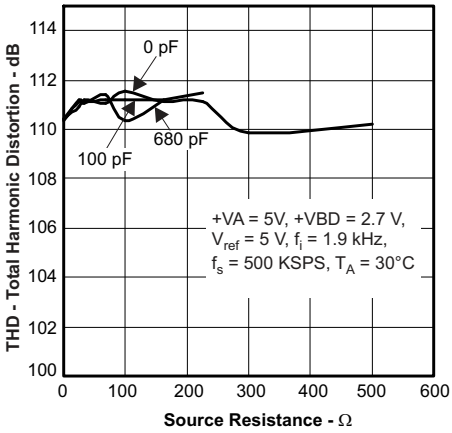



**Figure 35. Total Harmonic Distortion vs Source Resistance**

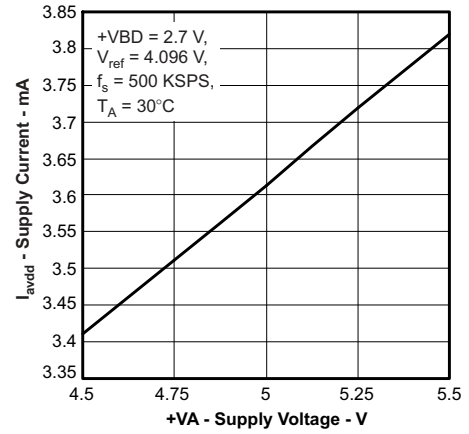



**Figure 36. Supply Current vs Supply Voltage**

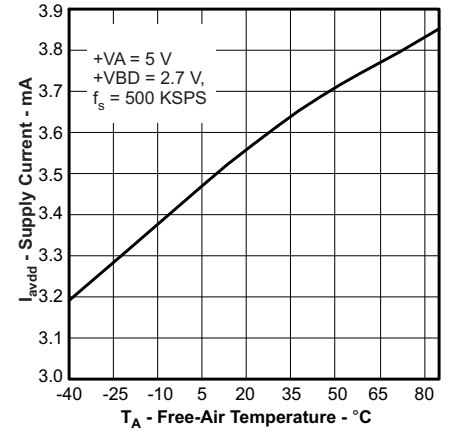



**Figure 37. Supply Current vs Free-Air Temperature**

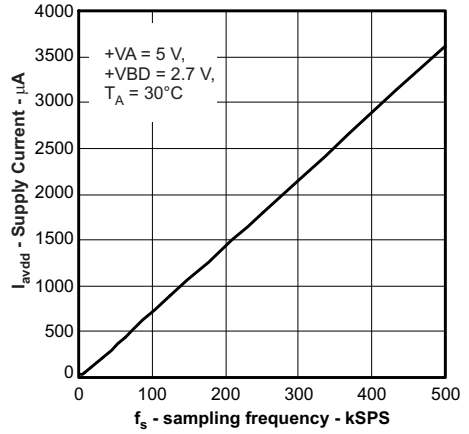



**Figure 38. Supply Current vs Sampling Frequency**

## Typical Characteristics (continued)

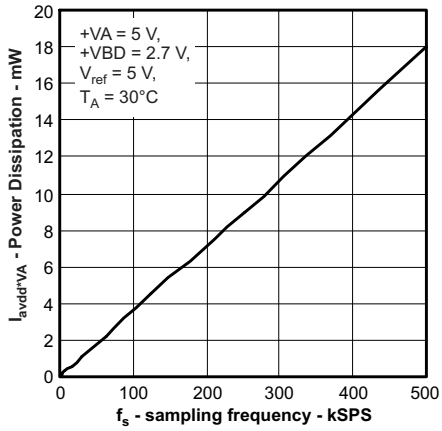



**Figure 39. Power Dissipation vs Sampling Frequency**

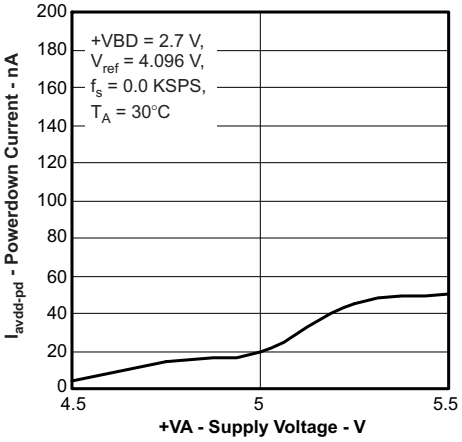



**Figure 40. Power-Down Current vs Supply Voltage**

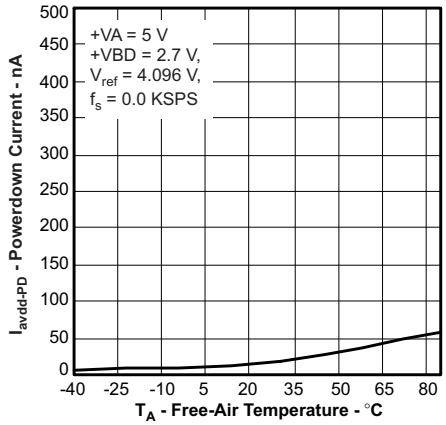



**Figure 41. Power-Down Current vs Free-Air Temperature**

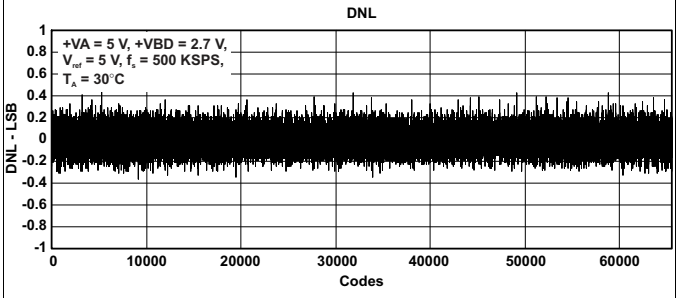



**Figure 42. DNL**

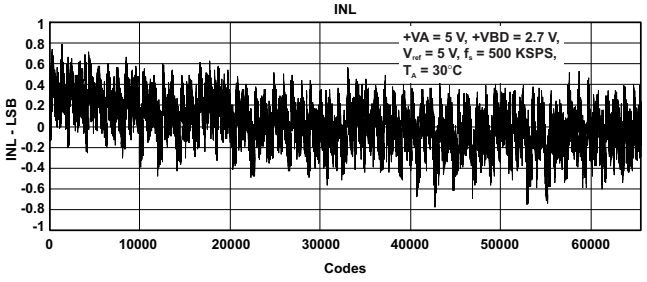



**Figure 43. INL**

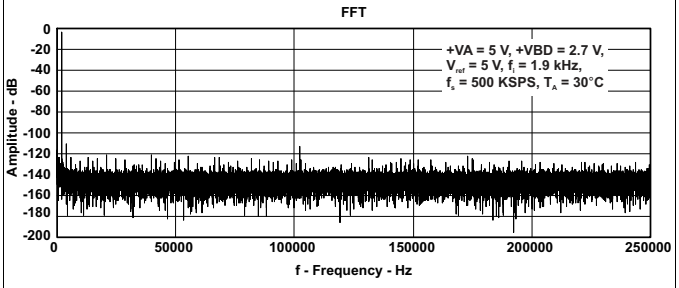



**Figure 44. FFT**

# 8 Detailed Description

## 8.1 Overview

The ADS8319 is a high-speed, low-power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample and hold function.

The ADS8319 is a single channel device. The analog input is provided to two input pins: +IN and –IN where –IN is a pseudo differential input and is limited to ±0.1 V. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both +IN and –IN inputs are disconnected from any internal function.

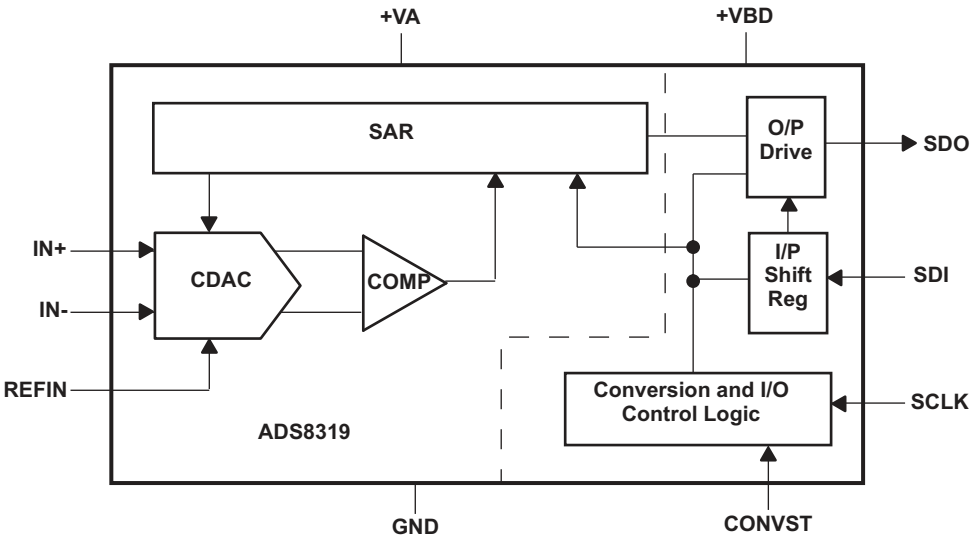
The ADS8319 has an internal clock that is used to run the conversion, and hence the conversion requires a fixed amount of time. After a conversion is completed, the device reconnects the sampling capacitors to the +IN and –IN pins, and the device is in the acquisition phase. During this phase the device is powered down and conversion data can be read.

The device digital output is available in SPI compatible format. It easily interfaces with microprocessors, DSPs, or FPGAs.

This is a low pin count device; however, it offers six different options for the interface. They can be grossly classified as *$\overline{CS}$ mode* (3 or 4-wire interface) and *daisy chain mode*. In both modes it can either be with or without a *busy indicator*, where the busy indicator is a bit preceeding the 16-bit serial data.

The *3-wire interface $\overline{CS}$ mode* is useful for applications which require galvanic isolation on-board, where as *4-wire interface $\overline{CS}$ mode* makes it easy to control an individual device while having multiple devices on-board. The *daisy chain mode* is provided to hook multiple devices in a chain like a shift register and is useful to reduce component count and the number of signal traces on the board.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Analog Input

When the converter samples the input, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on +IN is limited to GND – 0.1 V to $V_{REF}$ + 0.1 V and on –IN it is limited to GND – 0.1 to GND + 0.1 V; where as the differential signal is [(+IN) – (–IN)]. This allows the input to reject small signals which are common to both the +IN and –IN inputs.

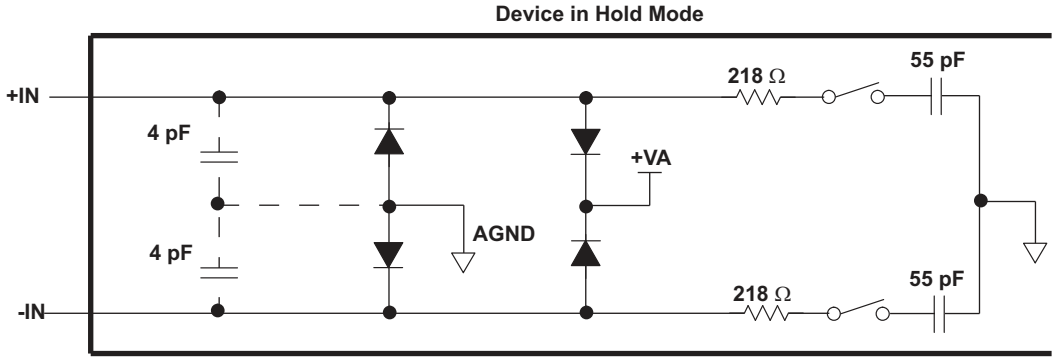



**Figure 45. Input Equivalent Circuit**

The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS8319 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (59 pF) to a 18-bit settling level within the minimum acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Take care regarding the absolute analog input voltage. To maintain linearity of the converter, the +IN and –IN inputs and the span [(+IN) – (–IN)] must be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.

Ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in an offset error, gain error, and linearity error which change with temperature and input voltage. Typically the –IN input is grounded at the input decoupling capacitor.

### 8.3.2 Driver Amplifier Choice

The analog input to the converter must be driven with a low noise op-amp like the THS4031 or OPA211. TI recommends a 5-Ω resitor and a 1-nF capacitor as a RC filter at the input pins to low-pass filter the noise from the source. The input to the converter is a unipolar input voltage from 0 V to $V_{REF}$. The minimum –3-dB bandwidth of the driving operational amplifier can be calculated with Equation 1.

$$f_{-3\ dB} = (\ln(2) \times (n + 2)) / (2\pi \times t_{ACQ}) \quad (1)$$

where

- n is equal to 16, the resolution of the ADC (in the case of the ADS8319)

When $t_{ACQ}$ = 600 ns (minimum acquisition time), the minimum bandwidth of the driving circuit is approximately 3 MHz (including RC following the driver OPA). The bandwidth can be relaxed if the acquisition time is increased by the application.

Typically a low noise OPA with ten times or higher bandwidth is selected. The driving circuit bandwidth is adjusted (to the required value) with a RC following the OPA. TI recommends the OPA211 or THS4031 for driving high-resolution high-speed ADCs.

### 8.3.3 Driver Amplifier Configurations

It is better to use a unity gain, noninverting buffer configuration. As explained before a RC following the OPA limits the input circuit bandwidth just enough for 16-bit settling. Higher bandwidth reduces the settling time (beyond what is required) but increases the noise in the ADC sampled signal, and hence the ADC output.

## Feature Description (continued)

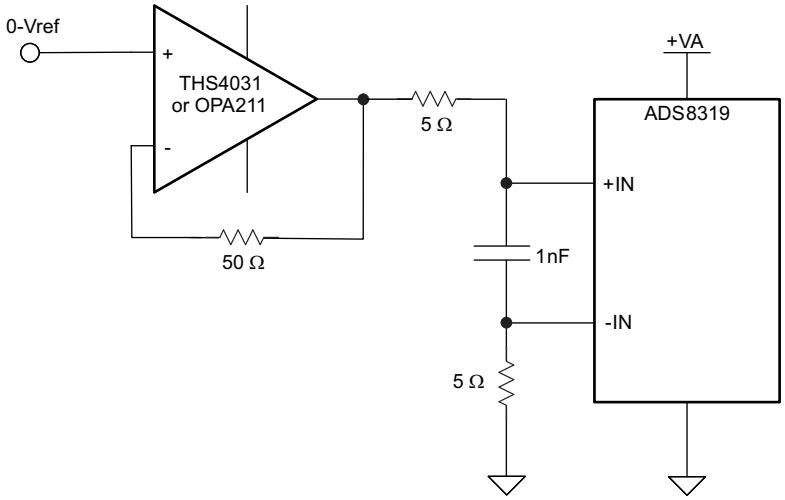





**Figure 46. Input Drive Configuration**

### 8.3.4 Reference

The ADS8319 can operate with an external reference from 2.25 V to $+V_A$ + 0.1 V. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5040 or REF5050 can be used to drive this pin. A ceramic decoupling capacitor is required between the REF+ and GND pins of the converter, as shown in Figure 47. The capacitor must be placed as close as possible to the pins of the device.

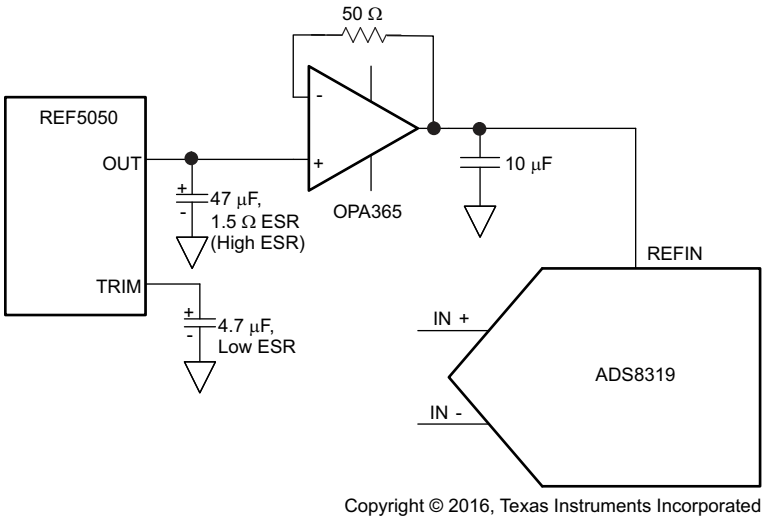





**Figure 47. External Reference Driving Circuit**

## Feature Description (continued)

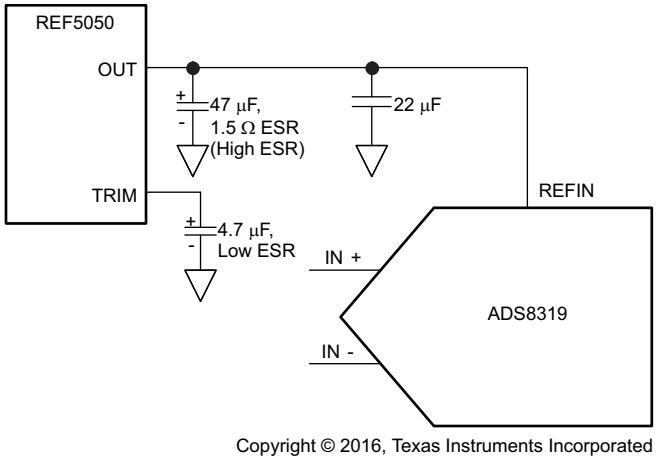





**Figure 48. Direct External Reference Driving Circuit**

### 8.3.5 Power Saving

The ADS8319 has an auto power-down feature. The device powers down at the end of every conversion. The input signal is acquired on sampling capacitors while the device is in the power-down state, and at the same time the conversion results are available for reading. The device powers up by itself on the start of the conversion. As discussed before, the conversion runs on an internal clock and takes a fixed time. As a result, device power consumption is directly proportional to the speed of operation.

### 8.3.6 Digital Output

The device digital output is SPI compatible, see *$\overline{CS}$ Mode* for more information. Table 1 lists the output codes corresponding to various analog input voltages.

**Table 1. Output Codes**

| DESCRIPTION | ANALOG VALUE (V) | DIGITAL OUTPUT STRAIGHT BINARY(1) | |
|---|---|---|---|
| | | BINARY CODE | HEX CODE |
| Positive full scale | $+V_{REF}$ – 1 LSB | 1111 1111 1111 1111 | FFFF |
| Midscale | $V_{REF}$ / 2 | 1000 0000 0000 0000 | 8000 |
| Midscale – 1 LSB | $V_{REF}$ / 2 – 1 LSB | 0111 1111 1111 1111 | 7FFF |
| Zero | 0 | 0000 0000 0000 0000 | 0000 |

(1) Output codes apply for Full-scale = $V_{REF}$ and Least-significant bit (LSB) = $V_{REF}$ / 65536

### 8.3.7 SCLK Input

The device uses SCLK for serial data output. Data is read after the conversion is over and the device is in the acquisition phase. It is possible to use a free running SCLK for the device, but TI recommends stopping the clock during a conversion, as the clock edges can couple with the internal analog circuit and can affect conversion results.

## 8.4 Device Functional Modes

### 8.4.1 $\overline{CS}$ Mode

*$\overline{CS}$ Mode* is selected if SDI is high at the rising edge of CONVST. As indicated before there are four different interface options available in this mode, namely *3-wire $\overline{CS}$ mode without busy indicator*, *3-wire $\overline{CS}$ mode with busy indicator*, *4-wire $\overline{CS}$ mode without busy indicator*, and *4-wire $\overline{CS}$ mode with busy indicator*.

## Device Functional Modes (continued)

### 8.4.1.1 3-Wire $\overline{CS}$ Mode Without Busy Indicator

The three-wire interface option in $\overline{CS}$ mode is selected if SDI is tied to +VBD, as shown in Figure 49. In the three-wire interface option, CONVST acts like $\overline{CS}$. The device samples the input signal and enters the conversion phase on the rising edge of CONVST, at the same time SDO goes to 3-state; see Figure 50. Conversion is done with the internal clock and it continues irrespective of the state of CONVST. As a result it is possible to bring CONVST (acting as $\overline{CS}$) low after the start of the conversion to select other devices on the board. But it is absolutely necessary that CONVST is high again before the minimum conversion time ($t_{cnv}$) is elapsed. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

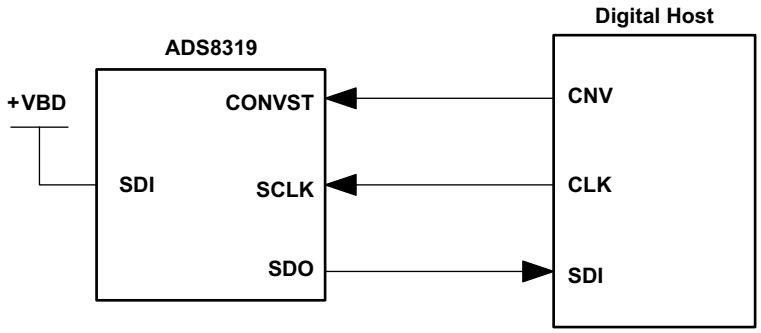





**Figure 49. Connection Diagram, 3-Wire $\overline{CS}$ Mode Without Busy Indicator (SDI = 1)**

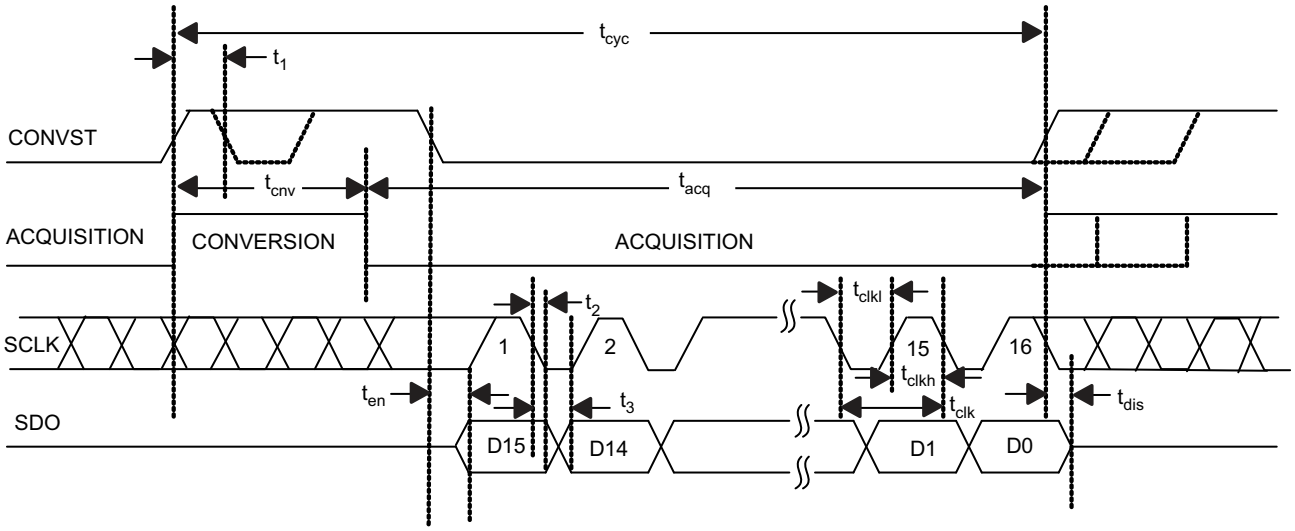



**Figure 50. Interface Timing Diagram, 3-Wire $\overline{CS}$ Mode Without Busy Indicator (SDI = 1)**

When the conversion is over, the device enters the acquisition phase and powers down. On the falling edge of CONVST, SDO comes out of three state, and the device outputs the MSB of the data. After this, the device outputs the next lower data bits on every falling edge of SCLK. SDO goes to 3-state after the 16$^{th}$ falling edge of SCLK or CONVST high, whichever occurs first. A minimum of 15 falling edges of SCLK must occur during the low period of CONVST.

## Device Functional Modes (continued)

### 8.4.1.2 3-Wire $\overline{CS}$ Mode With Busy Indicator

The three-wire interface option in $\overline{CS}$ mode is selected if SDI is tied to +VBD, as shown in Figure 51. In the three-wire interface option, CONVST acts like $\overline{CS}$. The device samples the input signal and enters the conversion phase on the rising edge of CONVST, at the same time SDO goes to 3-state; see Figure 52. Conversion is done with the internal clock and it continues irrespective of the state of CONVST. As a result it is possible to toggle CONVST (acting as $\overline{CS}$) after the start of the conversion to select other devices on the board. But it is absolutely necessary that CONVST is low again before the minimum conversion time ($t_{cnv}$) is elapsed and continues to stay low until the end of maximum conversion time. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.

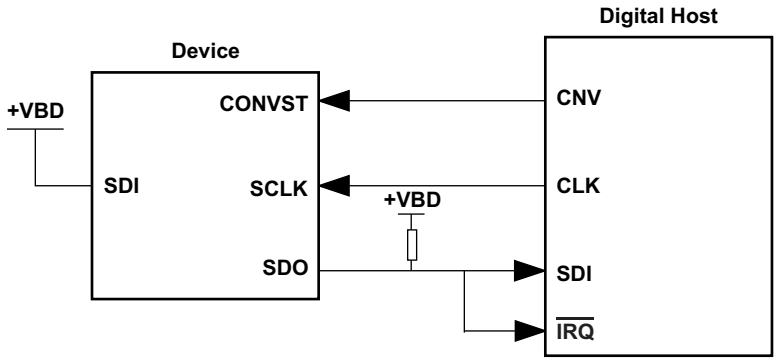



**Figure 51. Connection Diagram, 3-Wire $\overline{CS}$ Mode With Busy Indicator**

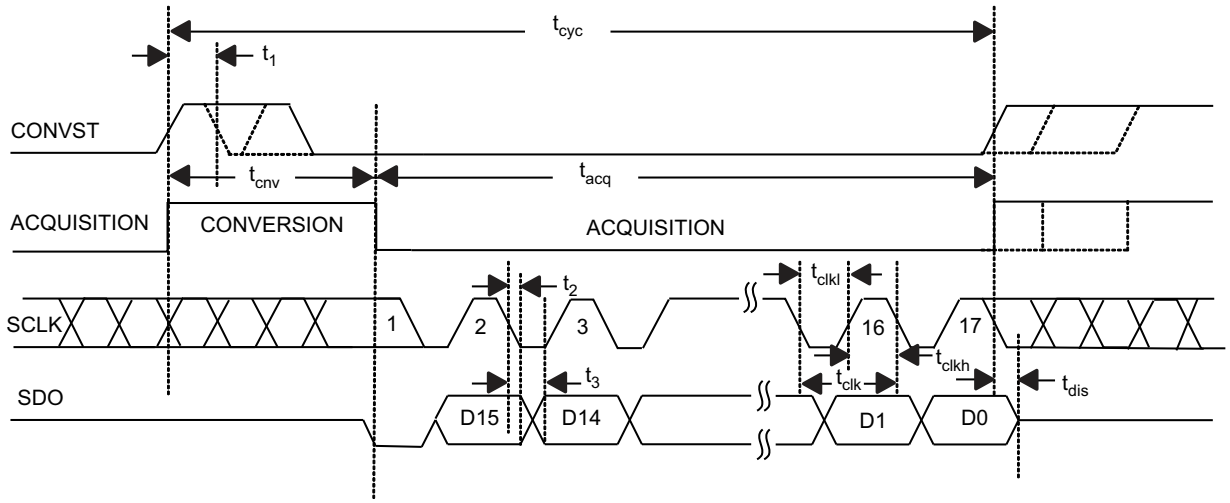



**Figure 52. Interface Timing Diagram, 3-Wire $\overline{CS}$ Mode With Busy Indicator (SDI = 1)**

When the conversion is over, the device enters the acquisition phase and powers down, and the device forces SDO out of three state and outputs a busy indicator bit (low level). The device outputs the MSB of data on the first falling edge of SCLK after the conversion is over and continues to output the next lower data bits on every subsequent falling edge of SCLK. SDO goes to three state after the 17$^{th}$ falling edge of SCLK or CONVST high, whichever occurs first. A minimum of 16 falling edges of SCLK must occur during the low period of CONVST.

## Device Functional Modes (continued)

### 8.4.1.3 4-Wire $\overline{CS}$ Mode Without Busy Indicator

As mentioned before for selecting *$\overline{CS}$ mode* it is necessary that SDI is high at the time of the CONVST rising edge. Unlike in *three-wire interface option*, SDI is controlled by digital host and acts like $\overline{CS}$. As shown in Figure 53, SDI goes to a high level before the rising edge of CONVST. The rising edge of CONVST while SDI is high selects $\overline{CS}$ mode, forces SDO to three state, samples the input signal, and the device enters the conversion phase. In the 4-wire interface option CONVST must be at a high level from the start of the conversion until all of the data bits are read. Conversion is done with the internal clock and it continues irrespective of the state of SDI. As a result it is possible to bring SDI (acting as $\overline{CS}$) low to select other devices on the board. But it is absolutely necessary that SDI is high again before the minimum conversion time ($t_{cnv}$) is elapsed.

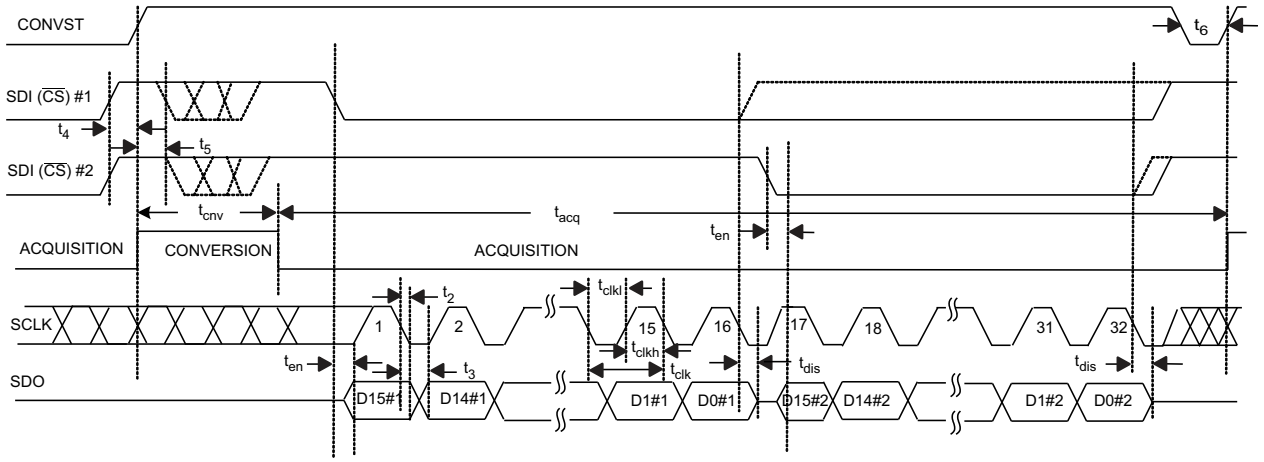



**Figure 53. Interface Timing Diagram, 4-Wire $\overline{CS}$ Mode Without Busy Indicator**

When the conversion is over, the device enters the acquisition phase and powers down. SDI falling edge can occur after the maximum conversion time ($t_{cnv}$). It is necessary that SDI be high at the end of the conversion, so that the device does not generate a *busy indicator*. The falling edge of SDI brings SDO out of 3-state and the device outputs the MSB of the data. Subsequent to this the device outputs the next lower data bits on every falling edge of SCLK. SDO goes to three state after the 16$^{th}$ falling edge of SCLK or SDI ($\overline{CS}$) high, whichever occurs first. As shown in Figure 54, it is possible to hook multiple devices on the same data bus. In this case the second device SDI (acting as $\overline{CS}$) can go low after the first device data is read and device 1 SDO is in three state.

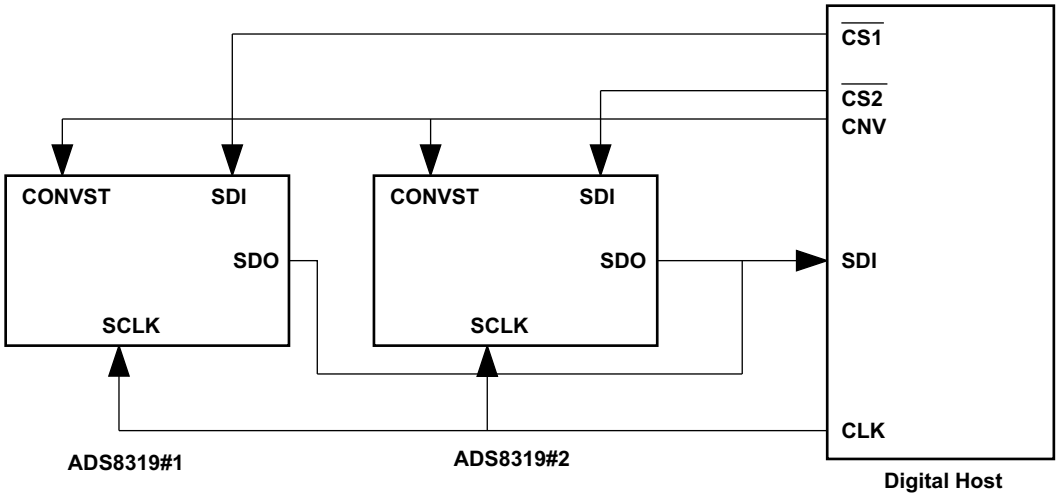





**Figure 54. Connection Diagram, 4-Wire $\overline{CS}$ Mode Without Busy Indicator**

## Device Functional Modes (continued)

Ensure that CONVST and SDI are not low together at any time during the cycle.

### 8.4.1.4 4-Wire $\overline{CS}$ Mode With Busy Indicator

As mentioned before for selecting $\overline{CS}$ *mode* it is necessary that SDI is high at the time of the CONVST rising edge. Unlike in the *three-wire interface option*, SDI is controlled by the digital host and acts like $\overline{CS}$. SDI goes to a high level before the rising edge of CONVST; see Figure 55. The rising edge of CONVST while SDI is high selects $\overline{CS}$ mode, forces SDO to three state, samples the input signal, and the device enters the conversion phase. In the 4-wire interface option CONVST must be at a high level from the start of the conversion until all of the data bits are read. Conversion is done with the internal clock and it continues irrespective of the state of SDI. As a result it is possible to toggle SDI (acting as $\overline{CS}$) to select other devices on the board. But it is absolutely necessary that SDI is low before the minimum conversion time ($t_{cnv}$) is elapsed and continues to stay low until the end of the maximum conversion time. A low level on the SDI input at the end of a conversion ensures the device generates a busy indicator.

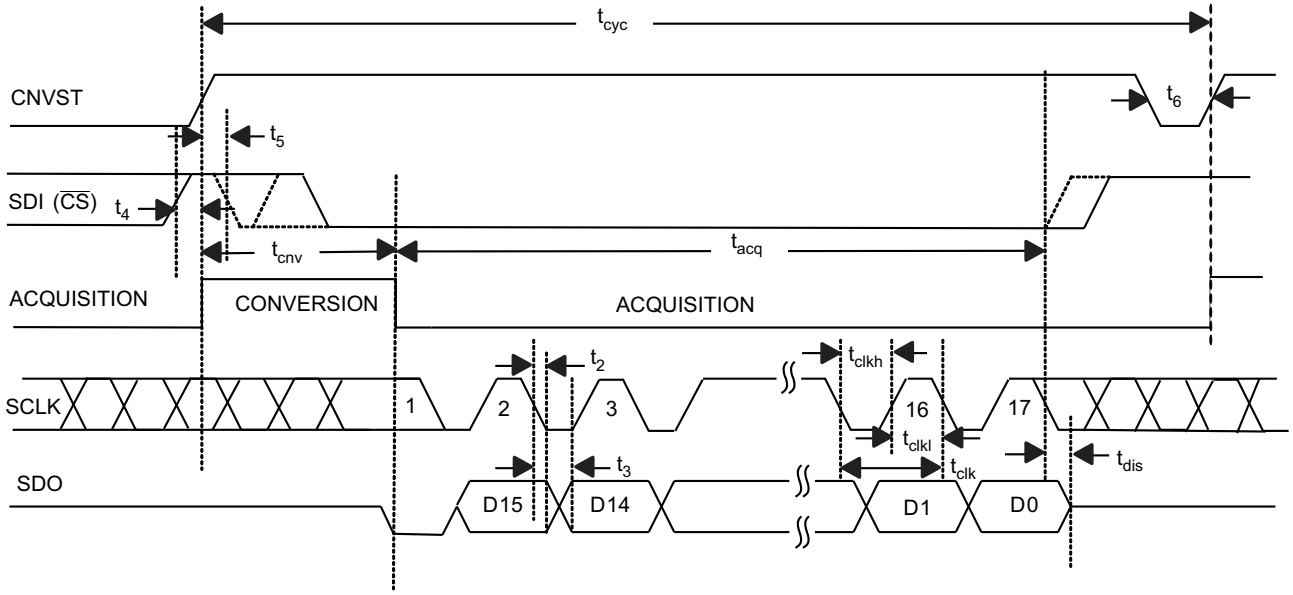



**Figure 55. Interface Timing Diagram, 4-Wire $\overline{CS}$ Mode With Busy Indicator**

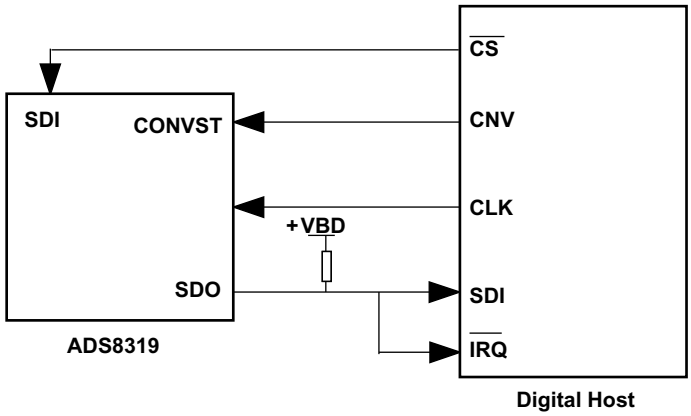





**Figure 56. Connection Diagram, 4-Wire $\overline{CS}$ Mode With Busy Indicator**

## Device Functional Modes (continued)

When the conversion is over, the device enters the acquisition phase and powers down, forces SDO out of three state, and outputs a busy indicator bit (low level). The device outputs the MSB of the data on the first falling edge of SCLK after the conversion is over and continues to output the next lower data bits on every falling edge of SCLK. SDO goes to three state after the 17$^{th}$ falling edge of SCLK or SDI ($\overline{CS}$) high, whichever occurs first.

Ensure that CONVST and SDI are not low together at any time during the cycle.

### 8.4.2 Daisy-Chain Mode

Daisy chain mode is selected if SDI is low at the time of CONVST rising edge. This mode is useful to reduce wiring and hardware like digital isolators in the applications where multiple (ADC) devices are used. In this mode all of the devices are connected in a chain (SDO of one device connected to the SDI of the next device) and data transfer is analogous to a shift register.

Like $\overline{CS}$ mode even this mode offers operation with or without a busy indicator.

#### *8.4.2.1 Daisy-Chain Mode Without Busy Indicator*

Figure 57 shows the connection diagram. SDI for device 1 is tied to ground, SDO of device 1 goes to SDI of device 2, and so on. SDO of the last device in the chain goes to the digital host. CONVST for all of the devices in the chain are tied together. In this mode there is no $\overline{CS}$ signal. The device SDO is driven low when SDI low selects daisy chain mode and the device samples the analog input and enters the conversion phase. It is necessary that SCLK is low at the rising edge of CONVST so that the device does not generate a busy indicator at the end of the conversion. In this mode CONVST continues to be high from the start of the conversion until all of the data bits are read. Once started, conversion continues irrespective of the state of SCLK.

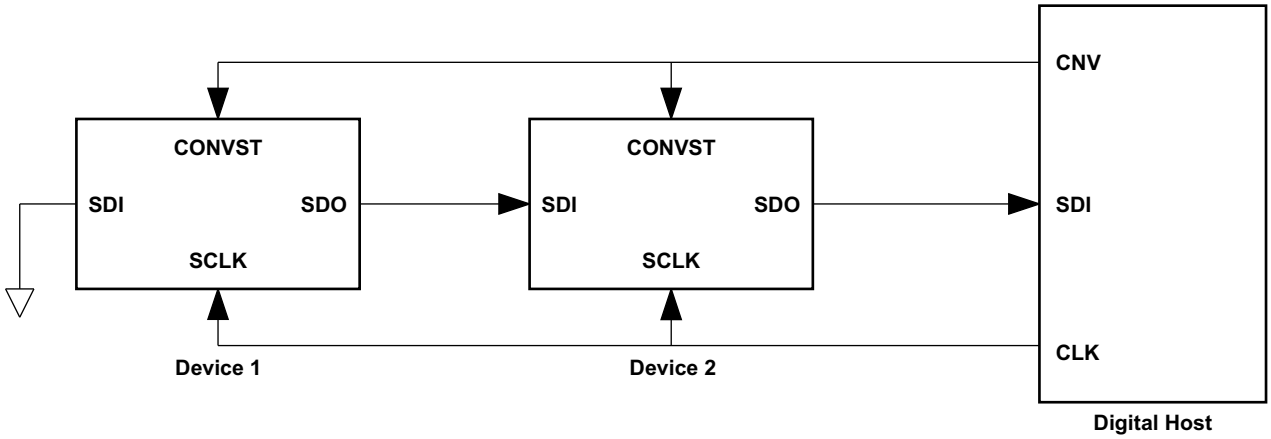



**Figure 57. Connection Diagram, Daisy-Chain Mode Without Busy Indicator (SDI = 0)**

## Device Functional Modes (continued)

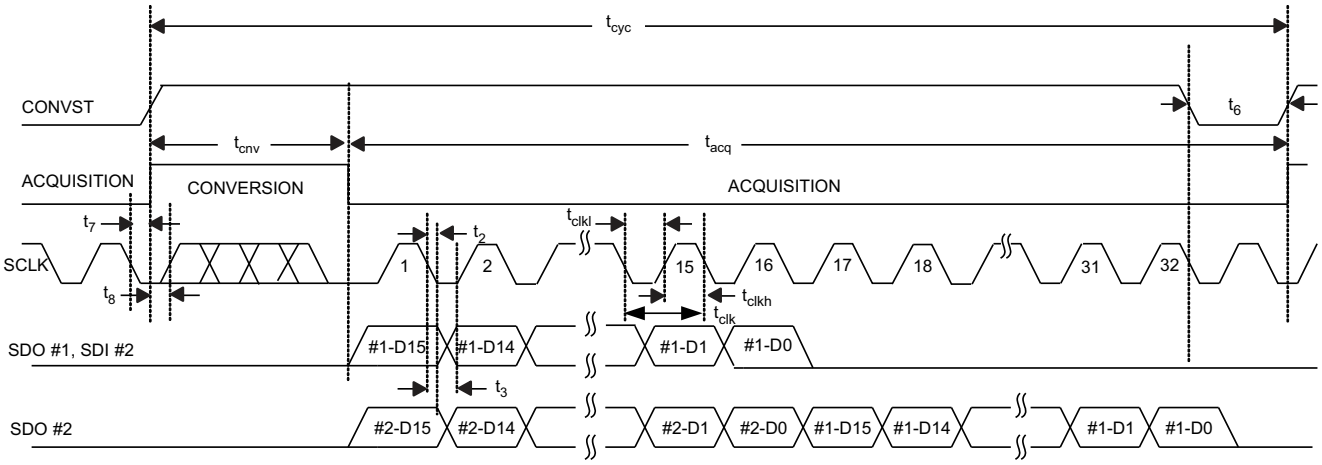



**Figure 58. Interface Timing Diagram, Daisy-Chain Mode Without Busy Indicator**

At the end of the conversion, every device in the chain initiates output of its conversion data starting with the MSB bit. Further the next lower data bit is output on every falling edge of SCLK. While every device outputs its data on the SDO pin, it also receives previous device data on the SDI pin (other than device #1) and stores it in the shift register. The device latches incoming data on every falling edge of SCLK. SDO of the first device in the chain goes low after the 16th falling edge of SCLK. All subsequent devices in the chain output the stored data from the previous device in MSB first format immediately following their own data word.

It requires 16 × N clocks to read data for N devices in the chain.

### *8.4.2.2 Daisy-Chain Mode With Busy Indicator*

Figure 59 shows the connection diagram. SDI for device 1 is wired to its CONVST and CONVST for all the devices in the chain are wired together. SDO of device 1 goes to $\overline{\text{SDI}}$ of device 2, and so on. SDO of the last device in the chain goes to the digital host. In this mode there is no $\overline{\text{CS}}$ signal. On the rising edge of CONVST, all of the device in the chain sample the analog input and enter the conversion phase. For the first device, SDI and CONVST are wired together, and the setup time of SDI to rising edge of CONVST is adjusted so that the device still enters chain mode even though SDI and CONVST rise together. It is necessary that SCLK is high at the rising edge of CONVST so that the device generates a busy indicator at the end of the conversion. In this mode, CONVST continues to be high from the start of the conversion until all of the data bits are read. Once started, conversion continues irrespective of the state of SCLK.

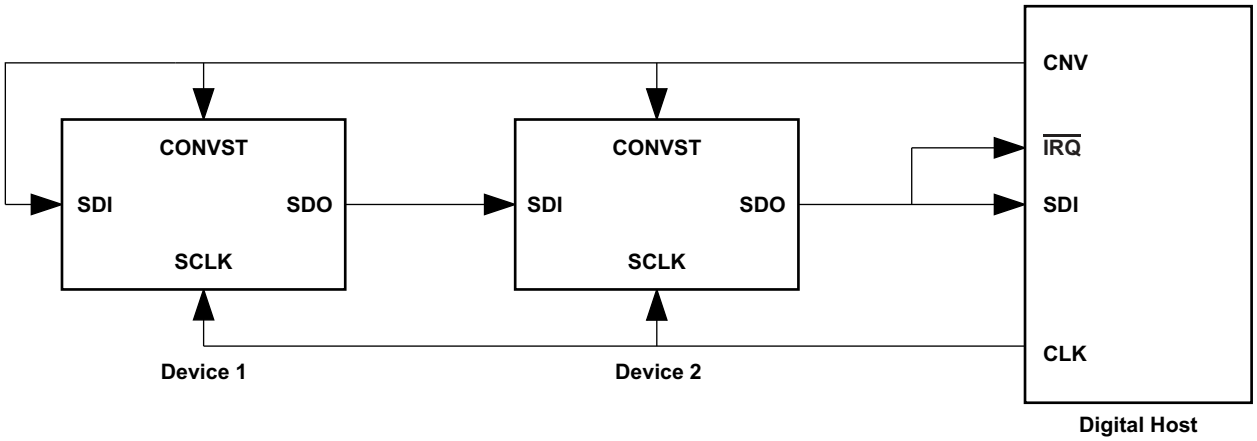



**Figure 59. Connection Diagram, Daisy-Mode With Busy Indicator (SDI = 0)**

## Device Functional Modes (continued)

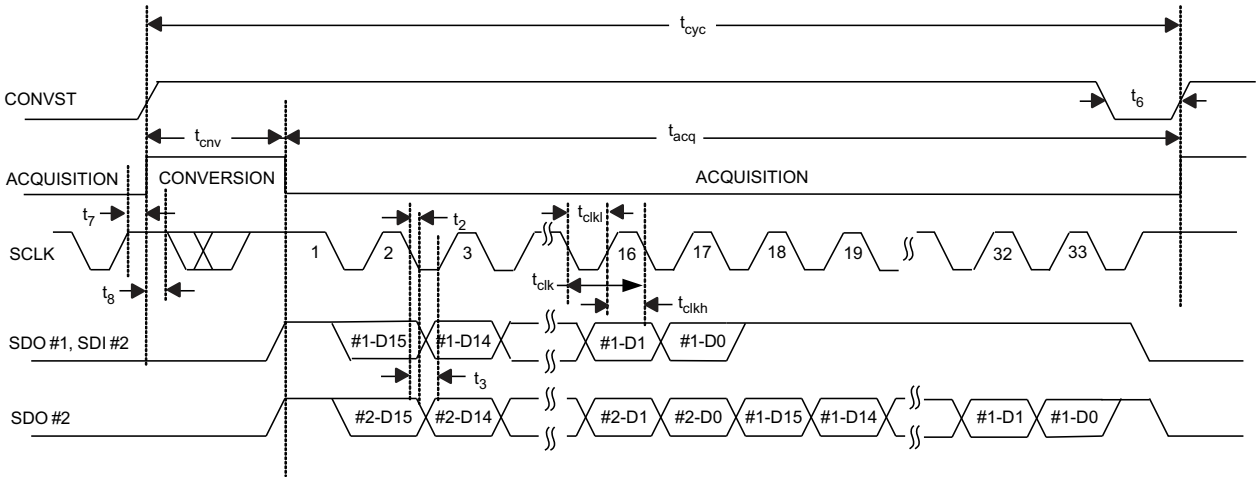



**Figure 60. Interface Timing Diagram, Daisy-Chain Mode With Busy Indicator**

At the end of the conversion, all the devices in the chain generate busy indicators. On the first falling edge of SCLK following the busy indicator bit, all of the devices in the chain output their conversion data starting with the MSB bit. After this the next lower data bit is output on every falling edge of SCLK. While every device outputs its data on the SDO pin, it also receives the previous device data on the SDI pin (except for device 1) and stores it in the shift register. Each device latches incoming data on every falling edge of SCLK. SDO of the first device in the chain goes high after the 17$^{th}$ falling edge of SCLK. All subsequent devices in the chain output the stored data from the pervious device in MSB first format immediately following their own data word. It requires 16 × N + 1 clock pulses to read data for N devices in the chain.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

To maximize the performance of data acquisition (DAQ) system based on a high precision, successive approximation register (SAR), analog-to-digital converter (ADC), the input driver and the reference driver circuits must be designed properly and must be optimized. This section details some general principles for designing these circuits, followed by an application circuit designed using the ADS8319.

## 9.2 Typical Application

This section describes a typical application circuit using the ADS8319. For simplicity, the power-supply circuit and decoupling capacitors are not shown in this circuit diagram.

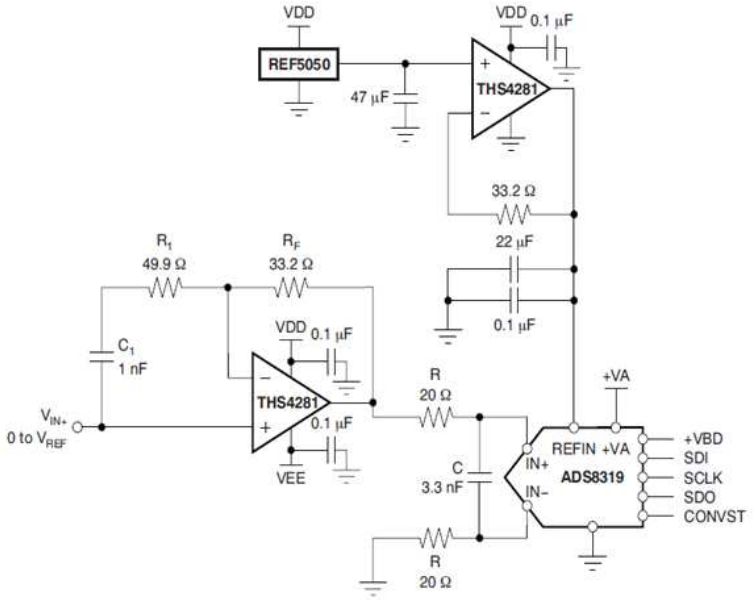





**Figure 61. Unipolar Single-Ended Input DAQ System**

### 9.2.1 Design Requirements

This application circuit for ADS8319 (as shown in Figure 61) is designed to achieve the key specific performance at a maximum specified throughput of 500 kSPS below:

- SNR > 92 dB
- THD < 111 dB
- Lower power consumption

### 9.2.2 Detailed Design Procedure

The reference driver circuit illustrated in Figure 61 generates 5-V DC using a single supply. This circuit is suitable to drive the reference at sampling rates of up to 500 kSPS. To keep the noise low and maximize the dynamic range, a high-precision, low-noise REF5050 voltage reference is used in this DAQ system

## Typical Application (continued)

For the input driver, the distortion of the amplifier must be at least 10 dB less than the ADC distortion. The low-power feature of ADS8319 makes it suitable for a low power DAQ system design. The THS4281 (low-power, high-speed voltage-feedback operational amplifier) is a perfect choice for input and reference driver of ADS8319 to offer a very low quiescent current (less than 1 mA) across the supply and temperature and drive large capacitive loads that regulate the voltage at the input and reference input pins of the ADC, its high bandwidth (40 MHz, specified at gain of 2) can make the signal settle quickly, also the Rail-to-Rail input and output feature can maximize the dynamic range of ADC as a driver.

Finally, the components of the balanced low-pass RC filter are chosen such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

For detailed design information, see *Low Power Input and Reference Driver Circuit for Reference Driver Circuit for ADS8318 and ADS8319* (SBOA118).

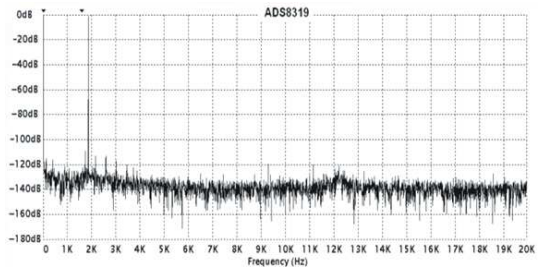
### 9.2.3 Application Curves

This section presents the performance results obtained on several devices for the driver and shown in Figure 62 through Figure 64.

Table 2 summarizes the test results obtained for the circuit shown in Figure 61.

**Table 2. Performance Results for ADS8319 DAQ System**

| PARAMETER | ADS8319 DATA SHEET LIMITS | ADS8319 WITH THS4031 | ADS8319 WITH THS4281 |
|---|---|---|---|
| $DNL_{MAX}$ | < 1.5 | 0.54 | 0.65 |
| $DNL_{Min}$ | > –1 | –0.5 | –0.53 |
| $INL_{MAX}$ | < 2.5 | 0.62 | 0.83 |
| $INL_{MIN}$ | > –2.5 | –0.95 | –0.65 |
| SNR | >92 dB | 93.9 dB | 92.5 dB |
| THD | –111 (typical) | –113 dB | –113 dB |
| SFDR | 113 (typical) | 115 dB | 115 dB |
| SINAD | 93.8 (typical) | 93.8 dB | 92.4 dB |
| Circuit power consumption | — | 205.6 mW | 38.44 mW |




1.9-kHz input signal

**Figure 62. FFT**

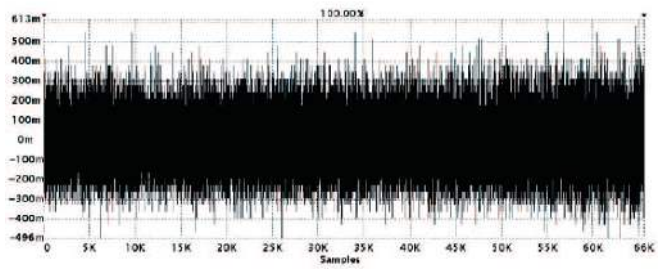



**Figure 63. Typical DNL Graph**

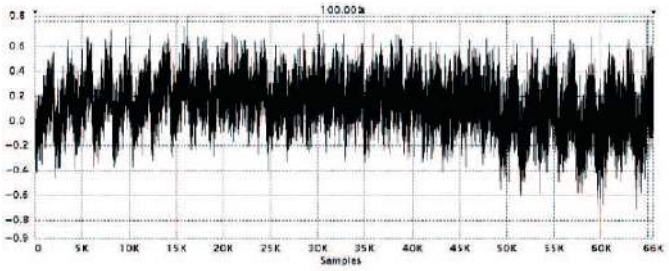



**Figure 64. Typical INL Graph**

## 10 Power Supply Recommendations

The ADS8319 is designed to operate using an analog supply voltage from 4.5 V to 5.5 V and a digital supply voltage from 2.375 V to 5.5 V. Both supplies must be well regulated. The analog supply must always be greater than or equal to the digital supply. A 1-µF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

## 11 Layout

### 11.1 Layout Guidelines

Figure 65 shows one of the board layouts as an example when using ADS8319 in a circuit.

- TI recommends a printed-circuit board (PCB) with at least four layers, and keeping all critical components on the top layer.
- Analog input signals and the reference input signals must be kept away from noise sources. Crossing digital lines with the analog signal path must be avoided. The analog input and the reference signals are routed on to the left side of the board and the digital connections are routed on the right side of the device.
- Due to the dynamic currents that occur during conversion and data transfer, each supply pin (AVDD and DVDD) must have a decoupling capacitor that keeps the supply voltage stable. TI recommends using one 1-µF ceramic capacitor at each supply pin.
- A layout that interconnects the converter and accompanying capacitors with the low inductance path is critical for achieving optimal performance. Using 15-mil vias to interconnect components to a solid analog ground plane at the subsequent inner layer minimizes stray inductance. Avoid placing vias between the supply pin and the decoupling capacitor. Any inductance between the supply capacitor and the supply pin of the converter must be kept to less than 5 nH by placing the capacitor within 0.2 inches from the supply or input pins of the ADS8319 and by using 20-mil traces, as shown in Figure 65.
- Dynamic currents are also present at the REFIN pin during the conversion phase. Therefore, good decoupling is critical to achieve optimal performance. The inductance between the reference capacitor and the REFIN pin must be kept to less than 2 nH by placing the capacitor within 0.1 inches from the REFIN pin and by using 20-mil traces.
- TI recommends a single 10-µF, X7R-grade, 0805-size ceramic capacitor with at least a 10-V rating for good performance over temperature range.
- A small, 0.1-Ω to 0.47-Ω, 0603-size resistor placed in series with the reference capacitor keeps the overall impedance low and constant, especially at very high frequencies.
- Avoid using additional lower value capacitors because the interactions between multiple capacitors can affect the ADC performance at higher sampling rates.
- Place the RC filters immediately next to the input pins. Among surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

## 11.2 Layout Example

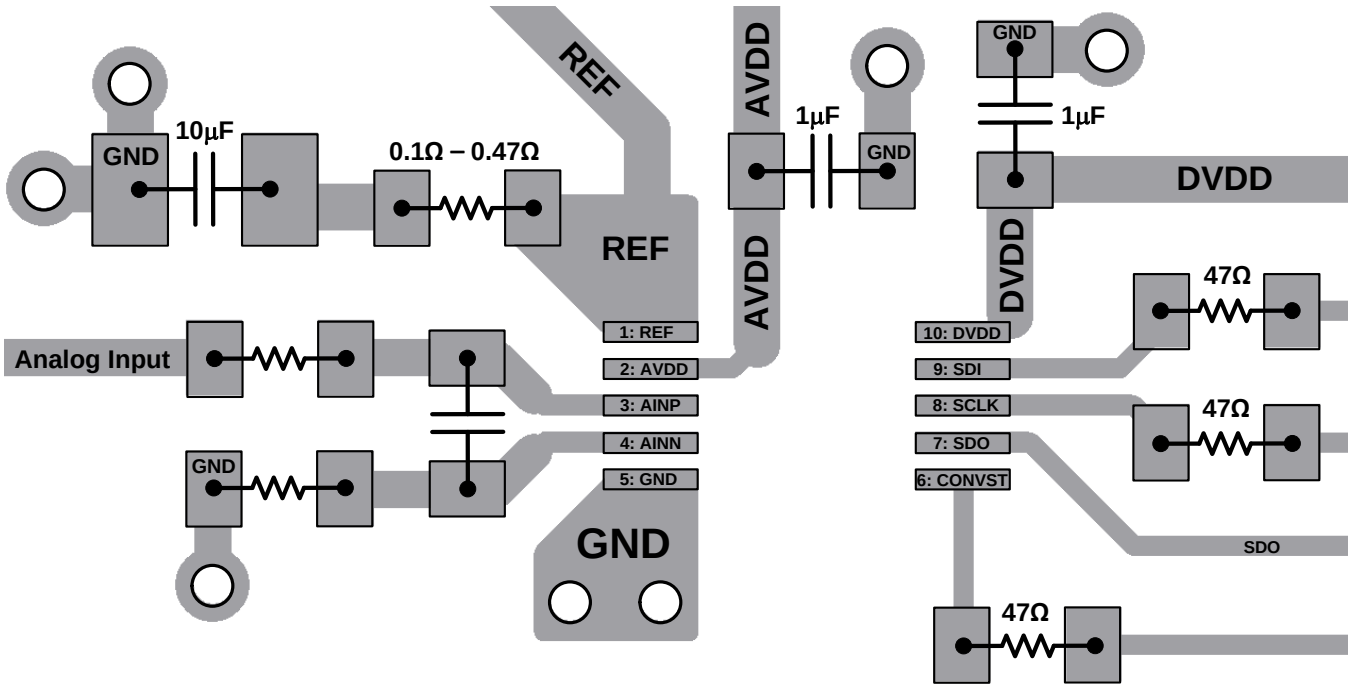



**Figure 65. Board Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Low Power Input and Reference Driver Circuit for Reference Driver Circuit for ADS8318 and ADS8319* (SBOA118)

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8319IBDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 85 | CEN | Samples |
| ADS8319IBDGST | ACTIVE | VSSOP | DGS | 10 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 85 | CEN | Samples |
| ADS8319IBDRCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | Call TI | Level-3-260C-168 HR | -40 to 85 | CEP | Samples |
| ADS8319IBDRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | Call TI | Level-3-260C-168 HR | -40 to 85 | CEP | Samples |
| ADS8319IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 85 | CEN | Samples |
| ADS8319IDGST | ACTIVE | VSSOP | DGS | 10 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 85 | CEN | Samples |
| ADS8319IDRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | Call TI | Level-3-260C-168 HR | -40 to 85 | CEP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

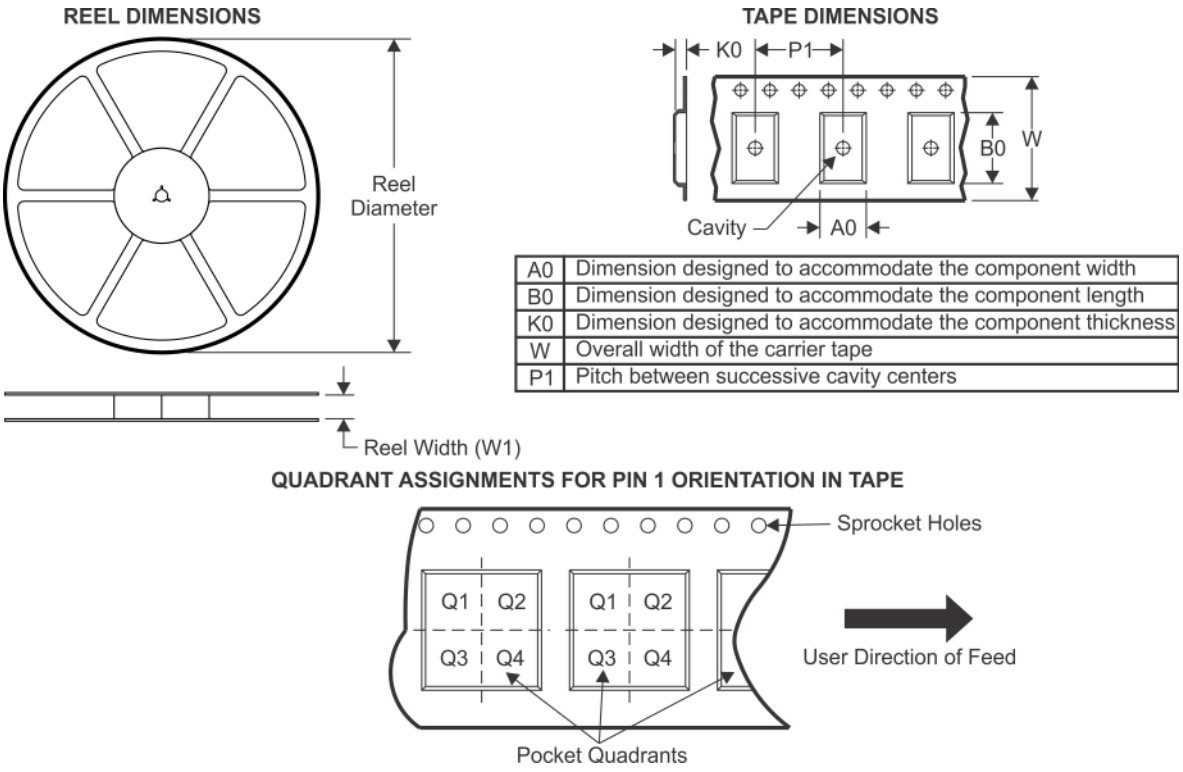
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

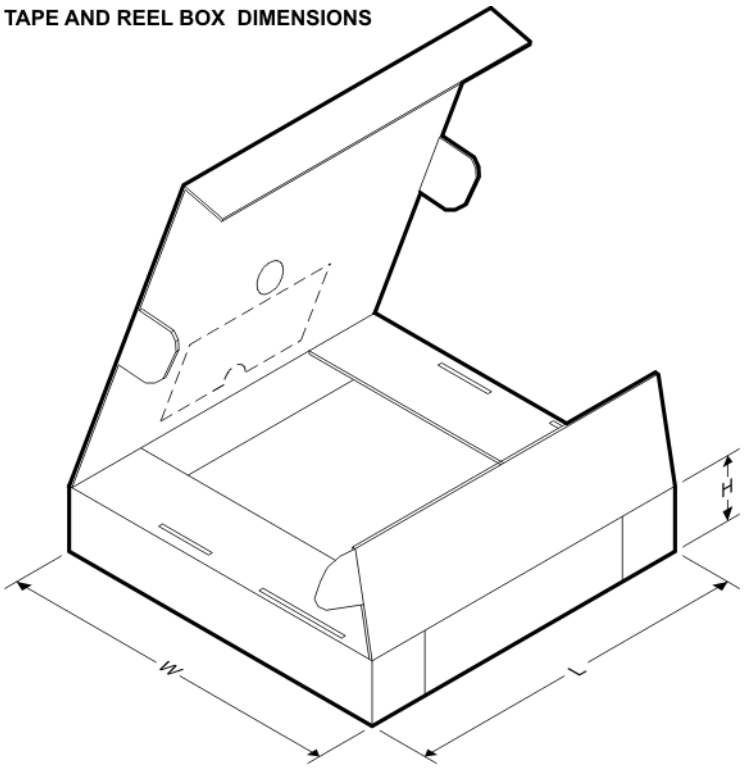



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8319IBDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| ADS8319IBDRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| ADS8319IDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

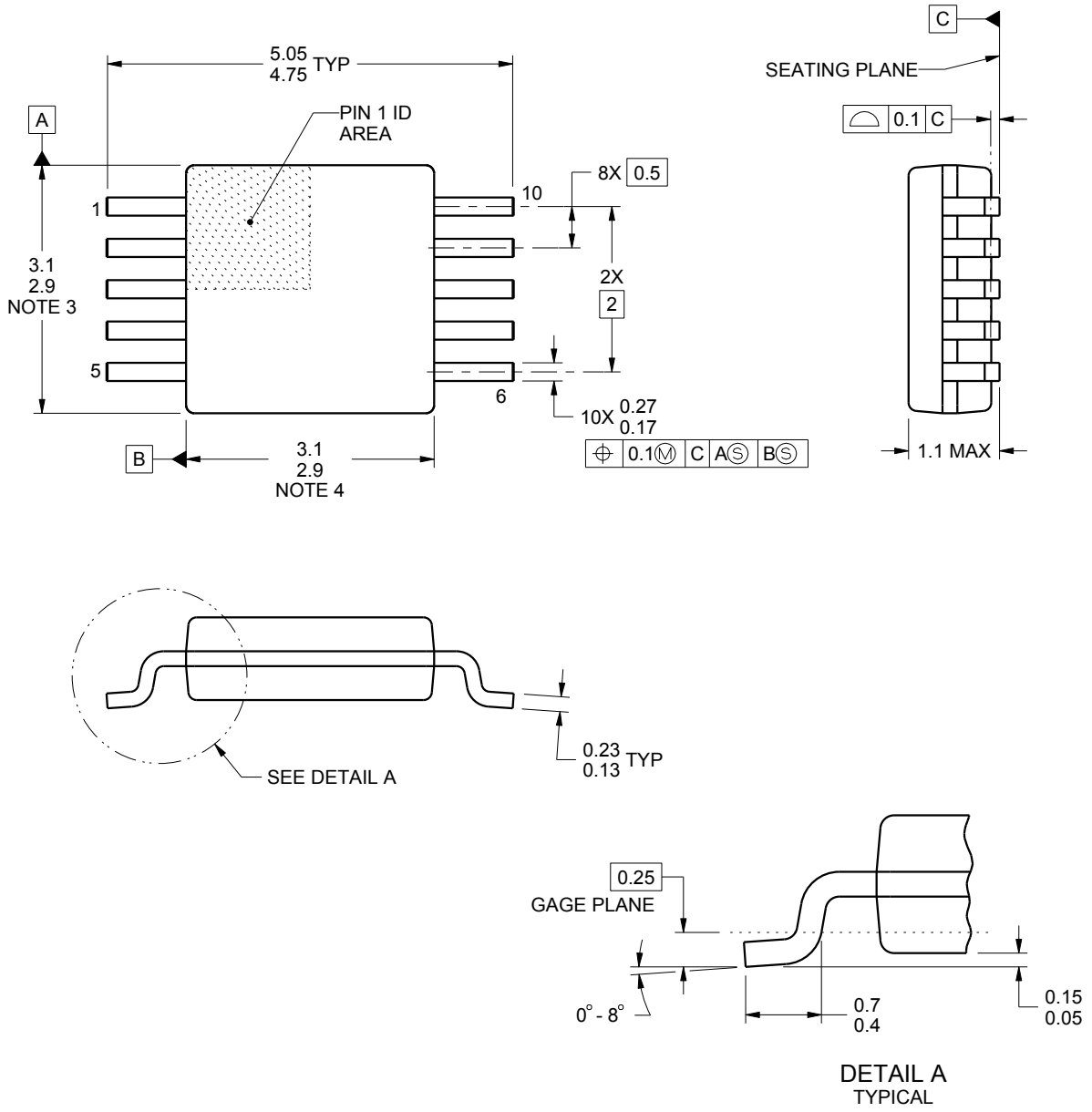
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS8319IBDGSR | VSSOP | DGS | 10 | 2500 | 350.0 | 350.0 | 43.0 |
| ADS8319IBDRCR | VSON | DRC | 10 | 3000 | 350.0 | 350.0 | 43.0 |
| ADS8319IDGSR | VSSOP | DGS | 10 | 2500 | 350.0 | 350.0 | 43.0 |

# PACKAGE OUTLINE

## DGS0010A

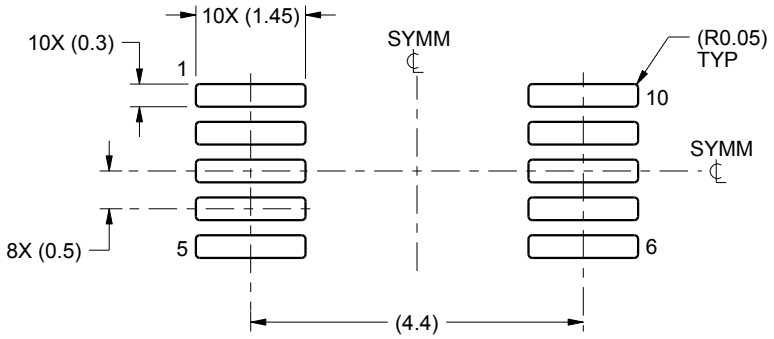
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

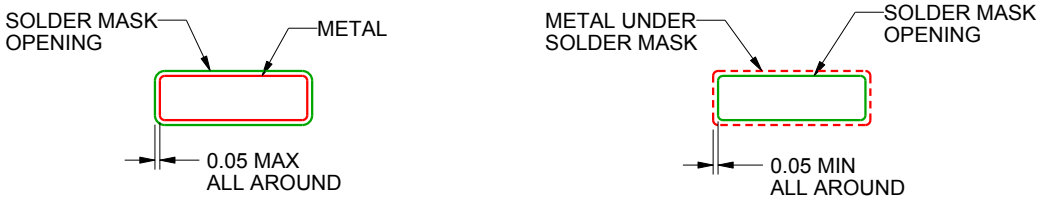



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

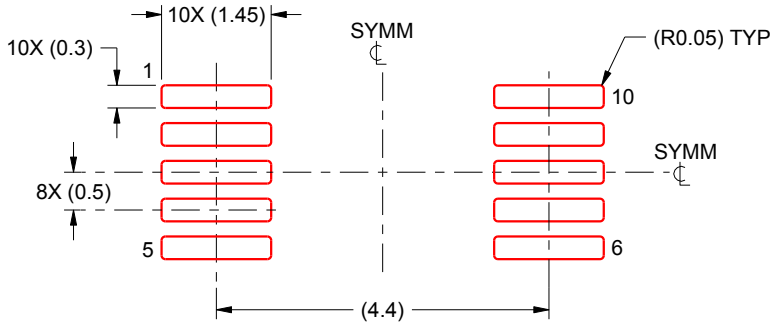



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

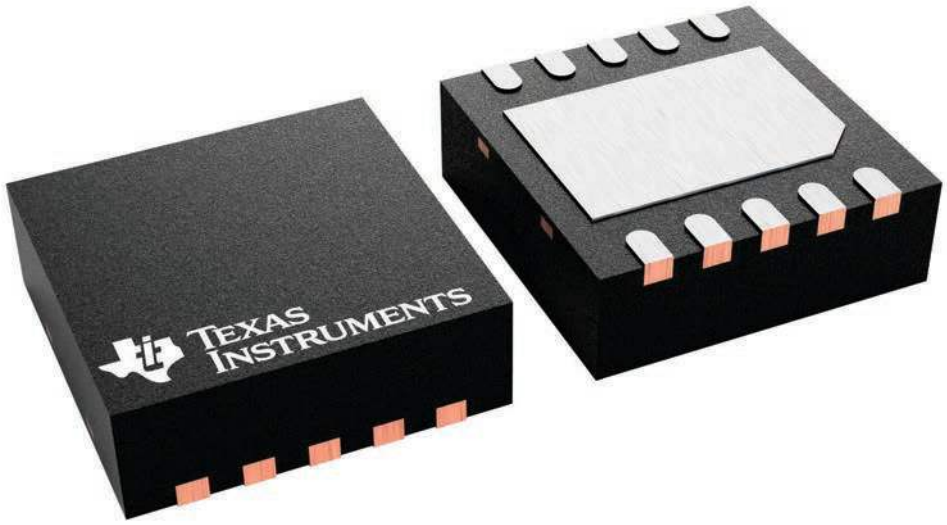
## DRC 10

## VSON - 1 mm max height

**3 x 3, 0.5 mm pitch**

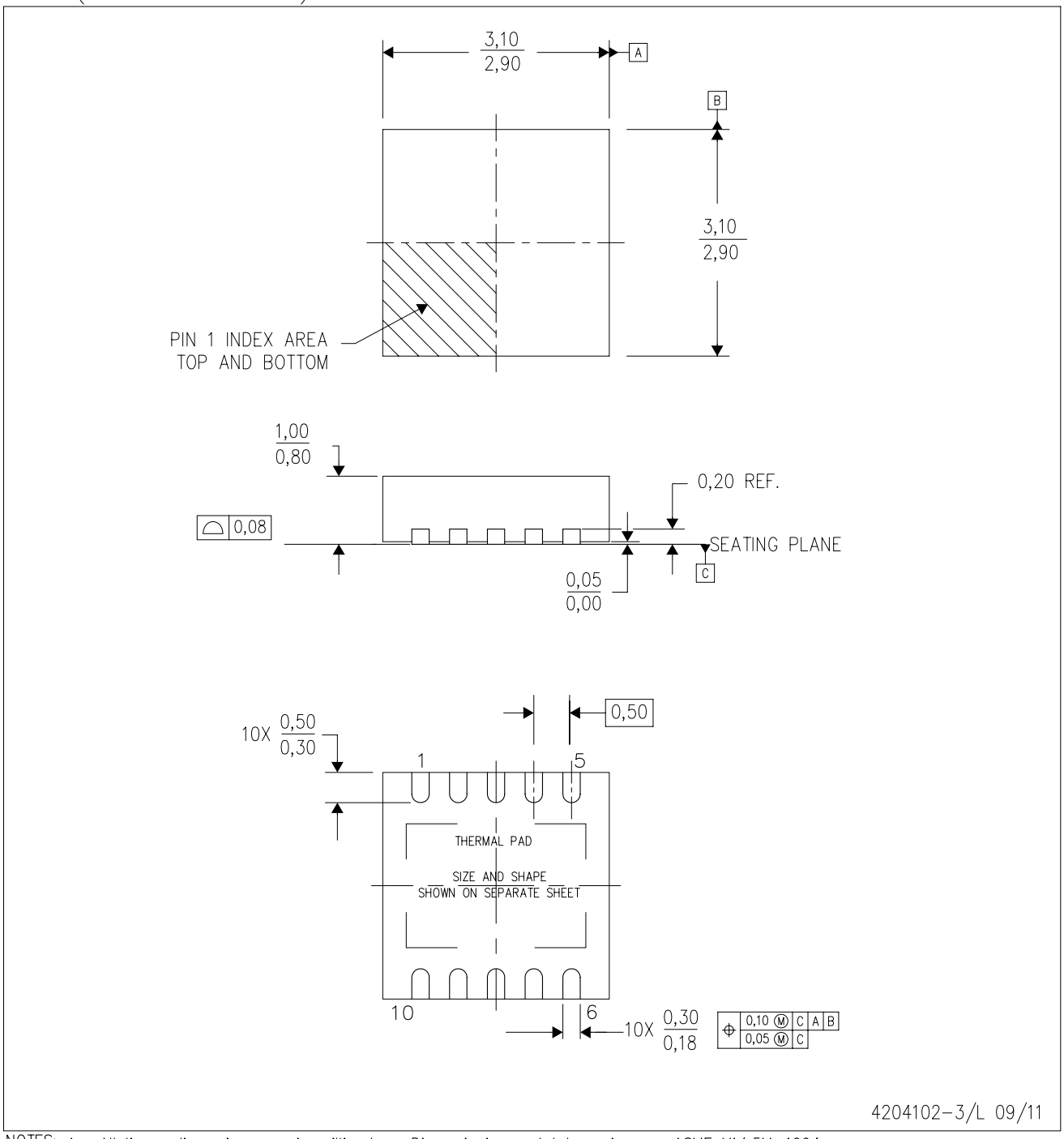
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4226193/A

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



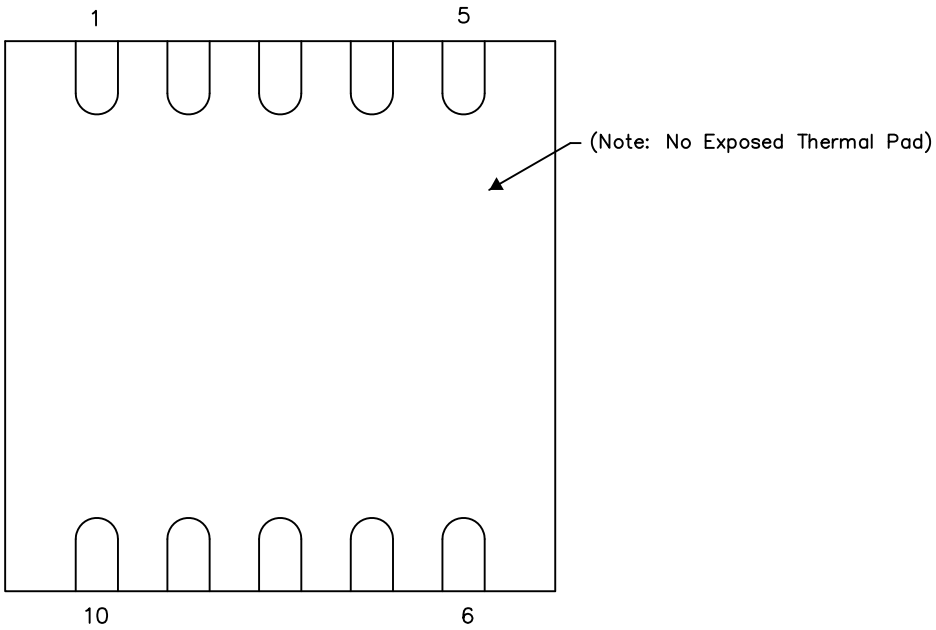

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This version of the package has no exposed thermal pad. This must be accounted for when estimating thermal performance.

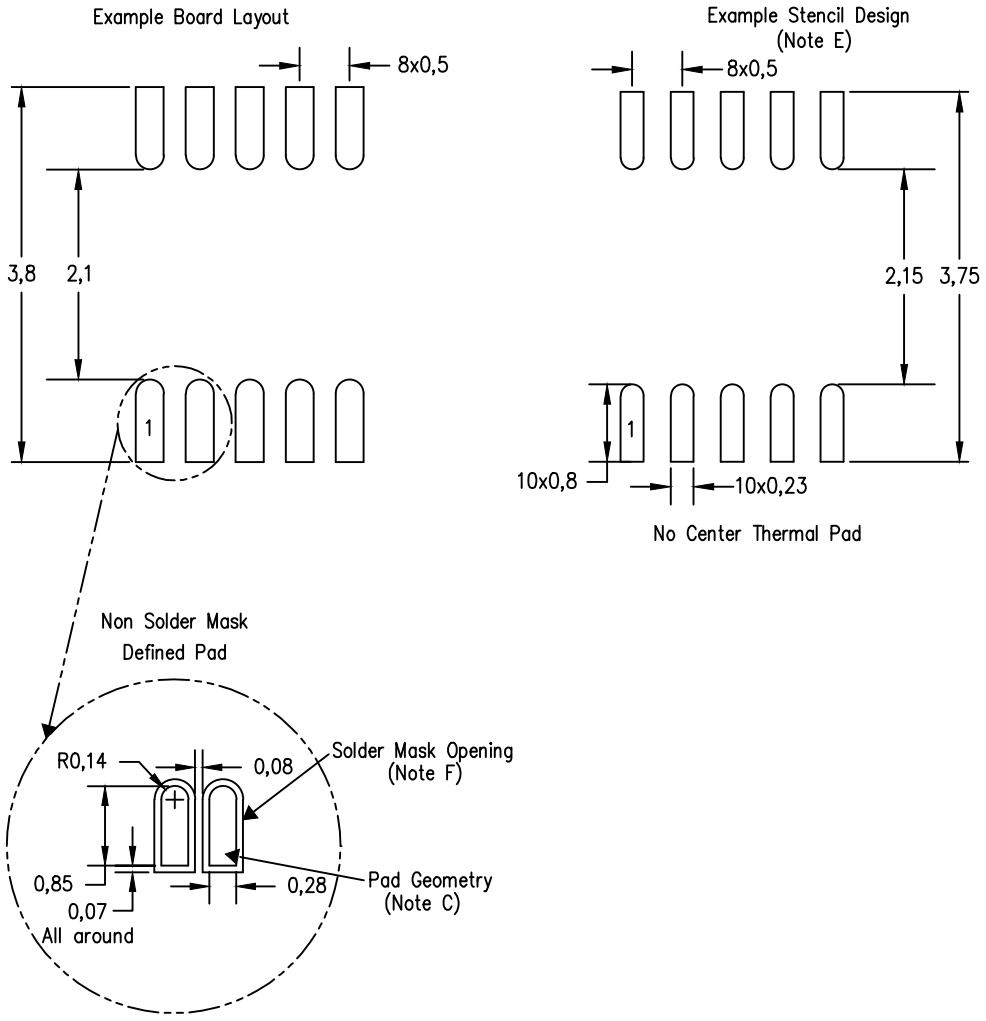
For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.




Bottom View

4206565–5/Y 08/15

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package does not have a center thermal pad. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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