

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

74ALVCH16952

16-bit registered transceiver; 3-state

Rev. 02 — 27 April 2006

Product data sheet

1. General description

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock ($nCPAB$ and $nCPBA$) provided that the clock enable ($nCEAB$ and $nCEBA$) is LOW. The data is then present at the output buffers, but is only accessible when the output enable input ($nOEAB$ and $nOEBA$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

2. Features

- CMOS low-power consumption
- Multibyte flow-through pinout architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standard JESD8-B

3. Quick reference data

Table 1. Quick reference data

$GND = 0 V$; $T_{amb} = 25\text{ }^{\circ}C$; $t_r = t_f = 2.5\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	propagation delay					
t_{PLH}	$nCPBA$ to nAn ; $nCPAB$ to nBn	$V_{CC} = 3.3\text{ V}$; $C_L = 50\text{ pF}$	-	3.2	-	ns
		$V_{CC} = 2.5\text{ V}$; $C_L = 30\text{ pF}$	-	3.2	-	ns
f_{max}	maximum input clock frequency	$V_{CC} = 3.3\text{ V}$	-	350	-	MHz
C_i	input capacitance		-	3.0	-	pF
C_{PD}	power dissipation capacitance	per buffer; $V_i = GND$ to V_{CC}	[1]	30	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

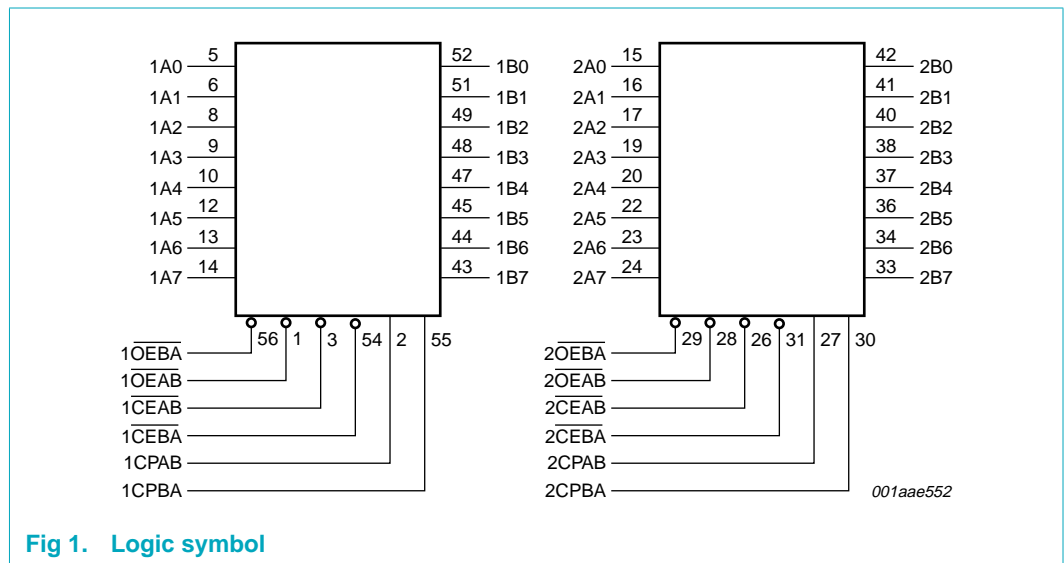
PHILIPS

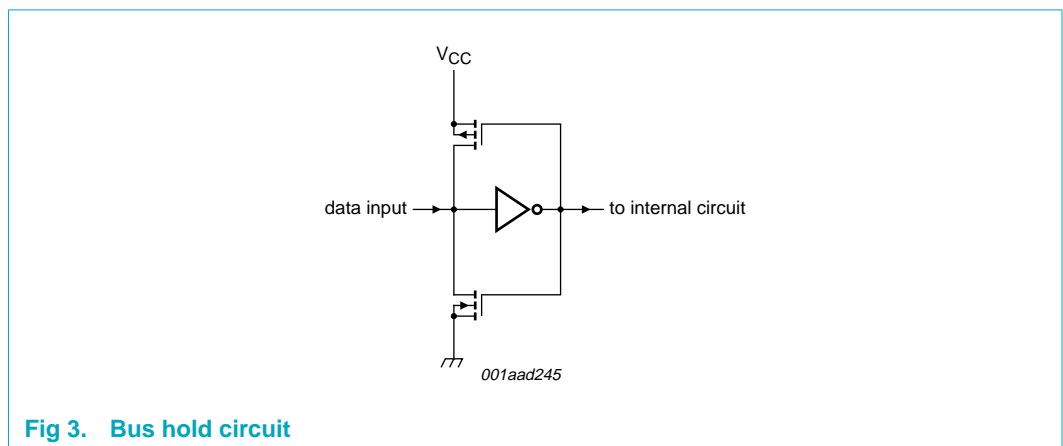
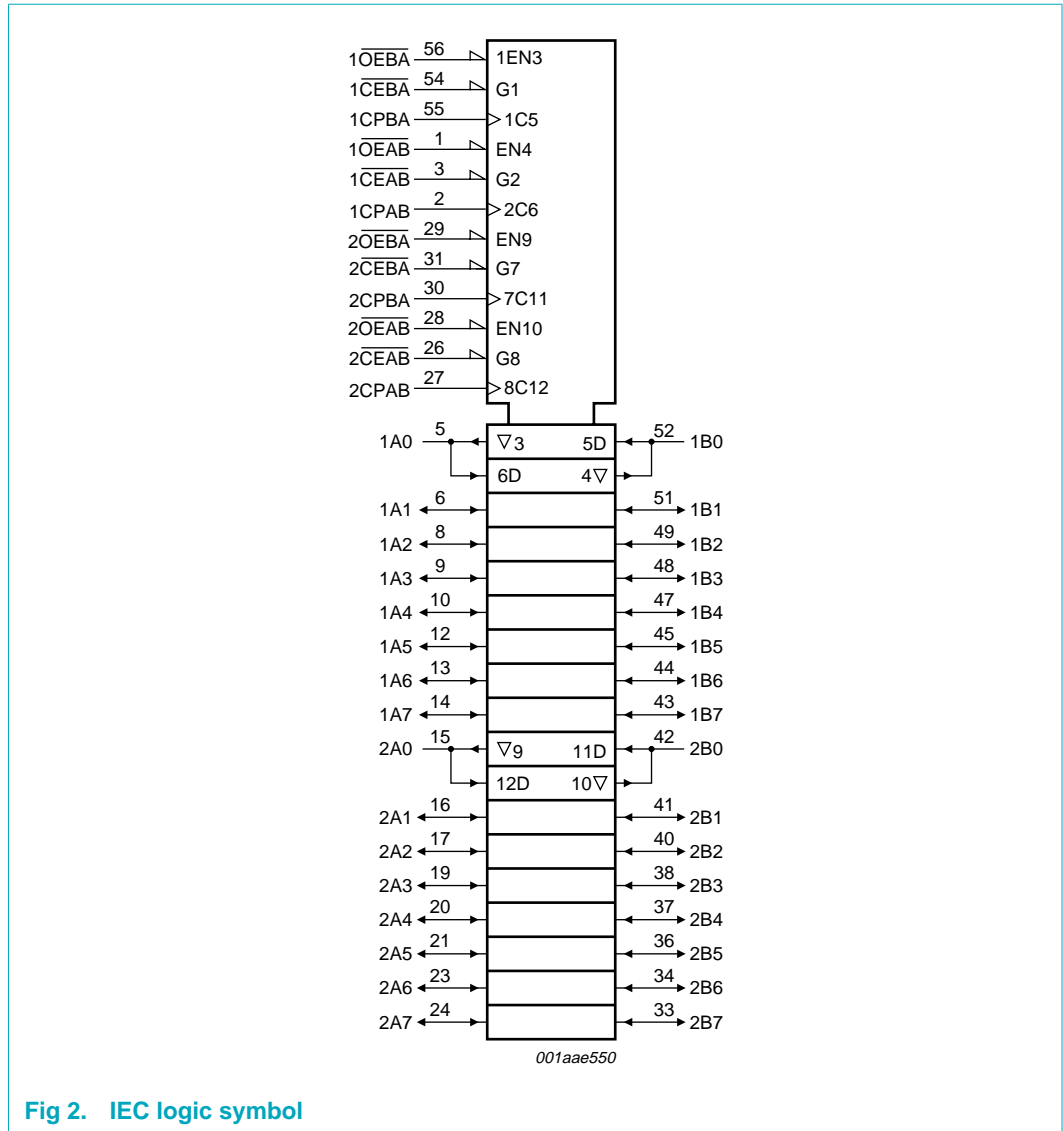
4. Ordering information

Table 2. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram





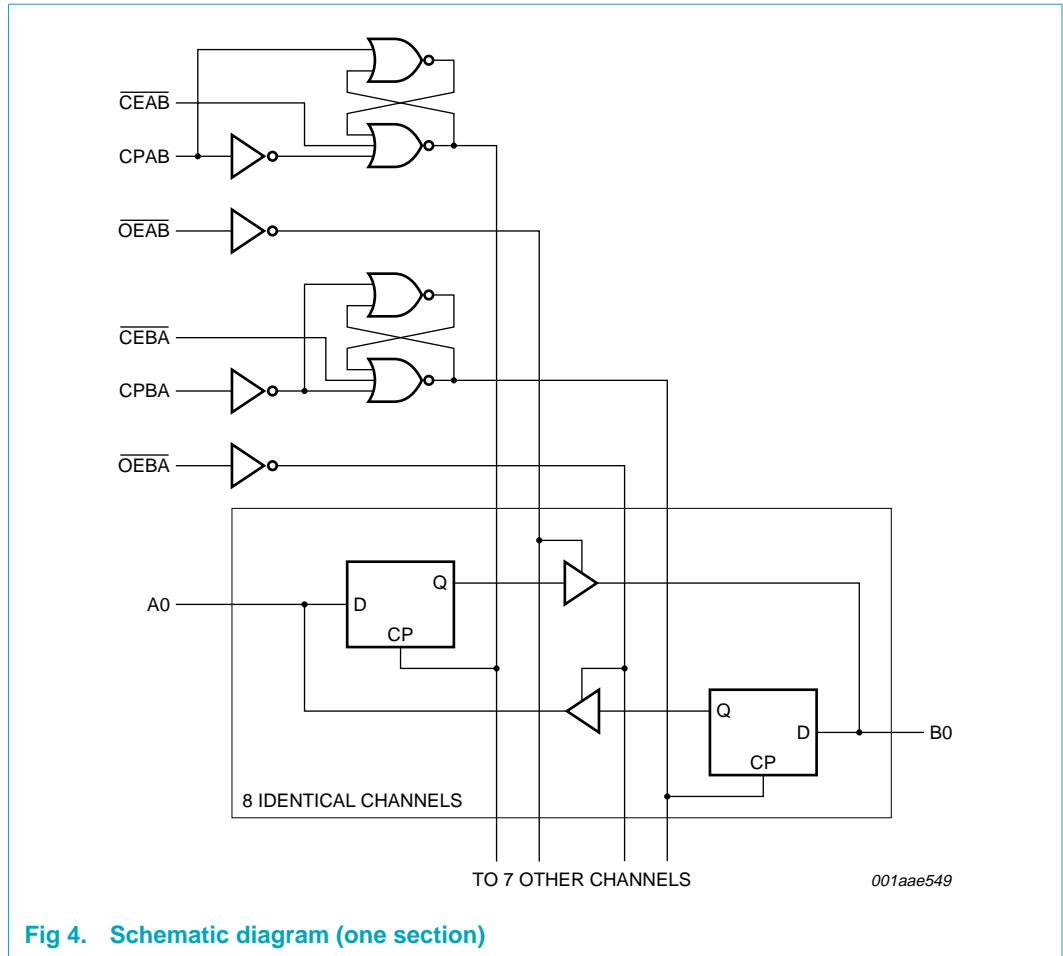
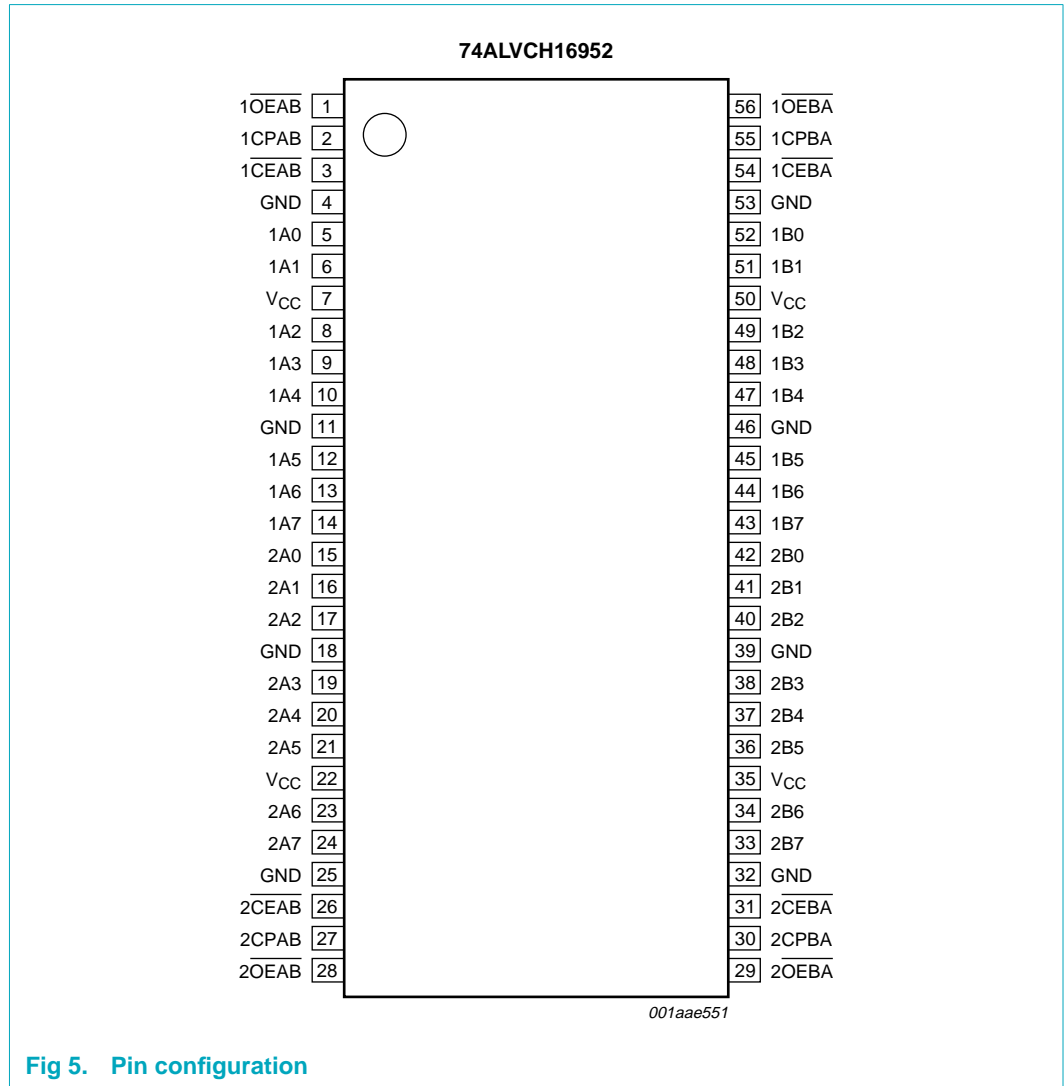


Fig 4. Schematic diagram (one section)

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1OEAB	1	output enable input (active LOW)
1CPAB	2	clock pulse input (active rising edge)
1CEAB	3	clock enable input (active LOW)
GND	4	ground (0 V)
1A0	5	data input or output 1A0
1A1	6	data input or output 1A1
V _{CC}	7	supply voltage

Table 3. Pin description ...continued

Symbol	Pin	Description
1A2	8	data input or output 1A2
1A3	9	data input or output 1A3
1A4	10	data input or output 1A4
GND	11	ground (0 V)
1A5	12	data input or output 1A5
1A6	13	data input or output 1A6
1A7	14	data input or output 1A7
2A0	15	data input or output 2A0
2A1	16	data input or output 2A1
2A2	17	data input or output 2A2
GND	18	ground (0 V)
2A3	19	data input or output 2A3
2A4	20	data input or output 2A4
2A5	21	data input or output 2A5
V _{CC}	22	supply voltage
2A6	23	data input or output 2A6
2A7	24	data input or output 2A7
GND	25	ground (0 V)
$\overline{2CEAB}$	26	clock enable input (active LOW)
2CPAB	27	clock pulse input (active rising edge)
$\overline{2OEAB}$	28	output enable input (active LOW)
$\overline{2OEB\overline{A}}$	29	output enable input (active LOW)
2CPBA	30	clock pulse input (active rising edge)
$\overline{2CEB\overline{A}}$	31	clock enable input (active LOW)
GND	32	ground (0 V)
2B7	33	data input or output 2B7
2B6	34	data input or output 2B6
V _{CC}	35	supply voltage
2B5	36	data input or output 2B5
2B4	37	data input or output 2B4
2B3	38	data input or output 2B3
GND	39	ground (0 V)
2B2	40	data input or output 2B2
2B1	41	data input or output 2B1
2B0	42	data input/output 2B0
1B7	43	data input or output 1B7
1B6	44	data input or output 1B6
1B5	45	data input or output 1B5
GND	46	ground (0 V)
1B4	47	data input or output 1B4
1B3	48	data input or output 1B3

Table 3. Pin description ...continued

Symbol	Pin	Description
1B2	49	data input or output 1B2
V _{CC}	50	supply voltage
1B1	51	data input or output 1B1
1B0	52	data input or output 1B0
GND	53	ground (0 V)
1 $\overline{\text{CEBA}}$	54	clock enable input (active LOW)
1CPBA	55	clock pulse input (active rising edge)
1 $\overline{\text{OEBA}}$	56	output enable input (active LOW)

7. Functional description

7.1 Function table

Table 4. Function table^{[1][2]}

Operating mode	Control			Input	Internal	Output
	n $\overline{\text{OEAB}}$	n $\overline{\text{CEAB}}$	nCPAB	nAn	nQn	nBn
Hold	L	H	X	X	NC	NC
Load and output enable	L	L	↑	L	L	L
				H	H	H
Load and output disable	H	L	↑	L	L	Z
				H	H	Z

[1] A-to-B data flow is shown; B-to-A data flow is similar, but uses signals n $\overline{\text{OEBA}}$, n $\overline{\text{CEBA}}$ and nCPBA

[2] H = HIGH voltage level;
 L = LOW voltage level;
 ↑ = LOW-to-HIGH transition;
 X = don't care;
 Z = high impedance OFF-state;
 NC = no change.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	control pins	[1] -0.5	+4.6	V
		data inputs	[1] -0.5	$V_{CC} + 0.5$	V
V_O	output voltage		[1] -0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	quiescent supply current		-	100	mA
I_{GND}	ground current		-	-100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	600	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 55 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	$C_L = 30$ pF	[1] 2.3	-	2.7	V
		$C_L = 50$ pF	[1] 3.0	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free-air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

[1] Maximum speed performance.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C^[1]						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _{OH} = -100 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _{OH} = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _{OH} = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _{OH} = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I _{OH} = -12 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.09	-	V
		I _{OH} = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _{OL} = 100 µA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _{OL} = 6 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _{OL} = 12 mA; V _{CC} = 2.3 V	-	0.15	0.70	V
		I _{OL} = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _{OL} = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V
I _{LI}	input leakage current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND	-	0.1	5	µA
I _{OZ}	off-state output current	V _{CC} = 2.7 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	0.1	10	µA
I _{CC}	quiescent supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	40	µA
ΔI _{CC}	additional quiescent supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	150	750	µA
I _{BHL}	bus hold LOW sustaining current	V _{CC} = 2.3 V; V _I = 0.7 V	[2] 45	-	-	µA
		V _{CC} = 3.0 V; V _I = 0.8 V	[2] 75	150	-	µA
I _{BHH}	bus hold HIGH sustaining current	V _{CC} = 2.3 V; V _I = 1.7 V	[2] -45	-	-	µA
		V _{CC} = 3.0 V; V _I = 2.0 V	[2] -75	-175	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V	[2] 500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V	[2] -500	-	-	µA
C _i	input capacitance		-	3.0	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Valid for data inputs of bus hold parts.

11. Dynamic characteristics

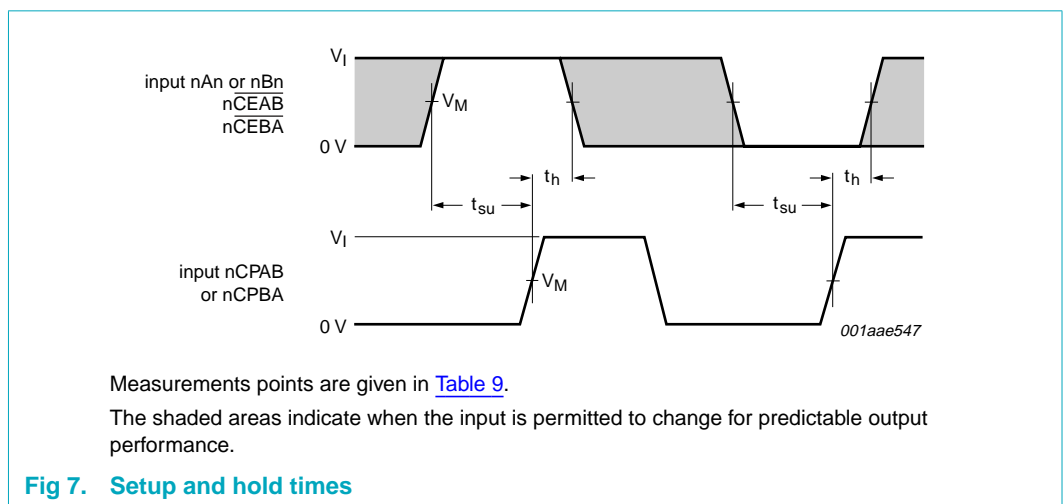
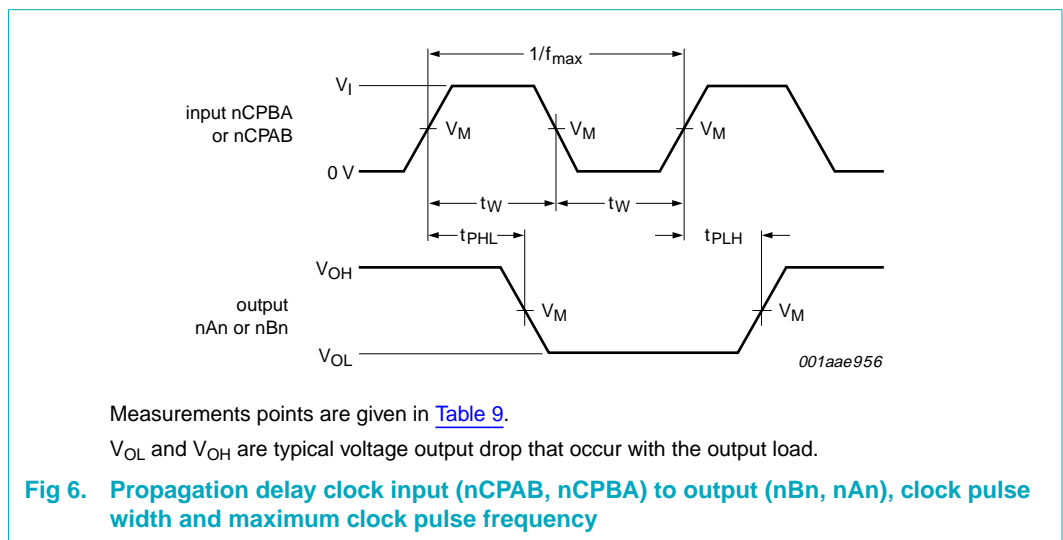
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$[1]							
t_{PHL} , t_{PLH}	propagation delay nCPBA to nAn; nCPAB to nBn	see Figure 6					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.2	4.1	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	-	4.6	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.2	3.9	ns	
t_{PZH} , t_{PZL}	3-state output enable time \overline{nOEBA} to nAn; \overline{nOEAB} to nBn	see Figure 8					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	-	5.4	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	-	5.3	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	-	4.4	ns	
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{nOEBA} to nAn; \overline{nOEAB} to nBn	see Figure 8					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	-	5.3	ns	
		$V_{CC} = 2.7\text{ V}$	1.4	-	4.4	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.1	-	4.0	ns	
t_W	pulse width HIGH or LOW nCPAB; nCPBA	see Figure 6					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	3.3	-	-	ns	
		$V_{CC} = 2.7\text{ V}$	3.3	-	-	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.3	-	-	ns	
t_{su}	setup time nAn to nCPAB or nBn to nCPBA	see Figure 7					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	ns	
		$V_{CC} = 2.7\text{ V}$	1.9	-	-	ns	
			$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	-	ns
	nCEAB to nCPAB or \overline{nCEBA} to nCPBA	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.2	-	-	ns	
		$V_{CC} = 2.7\text{ V}$	1.0	-	-	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$		1.0	-	-	ns		
t_h	hold time nAn to nCPAB or nBn to nCPBA	see Figure 7					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.6	-	-	ns	
		$V_{CC} = 2.7\text{ V}$	0.6	-	-	ns	
			$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.8	-	-	ns
	nCEAB to nCPAB or \overline{nCEBA} to nCPBA	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.1	-	-	ns	
		$V_{CC} = 2.7\text{ V}$	0.9	-	-	ns	
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$		1.1	-	-	ns		
f_{max}	maximum clock pulse frequency	see Figure 6					
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	150	350	-	MHz	
		$V_{CC} = 2.7\text{ V}$	150	350	-	MHz	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	150	350	-	MHz	
C_{PD}	power dissipation capacitance	per buffer; $V_1 = \text{GND to }V_{CC}$	[2]	-	30	pF	

- [1] Typical values are measured at nominal supply voltage and at $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



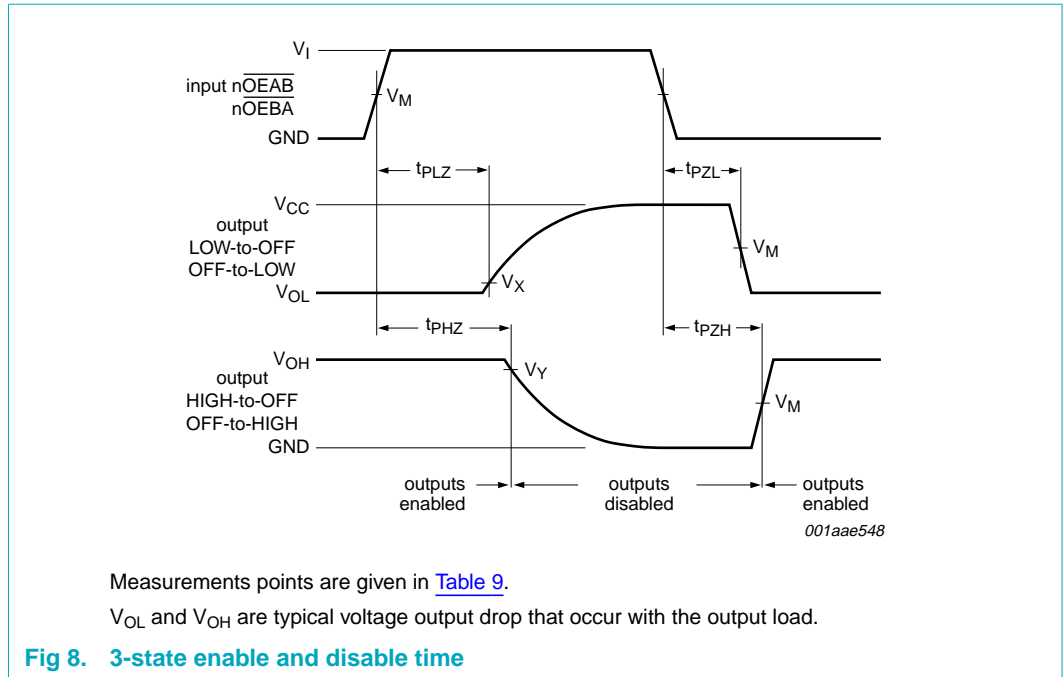


Table 9. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	0.5 V	0.5 V	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

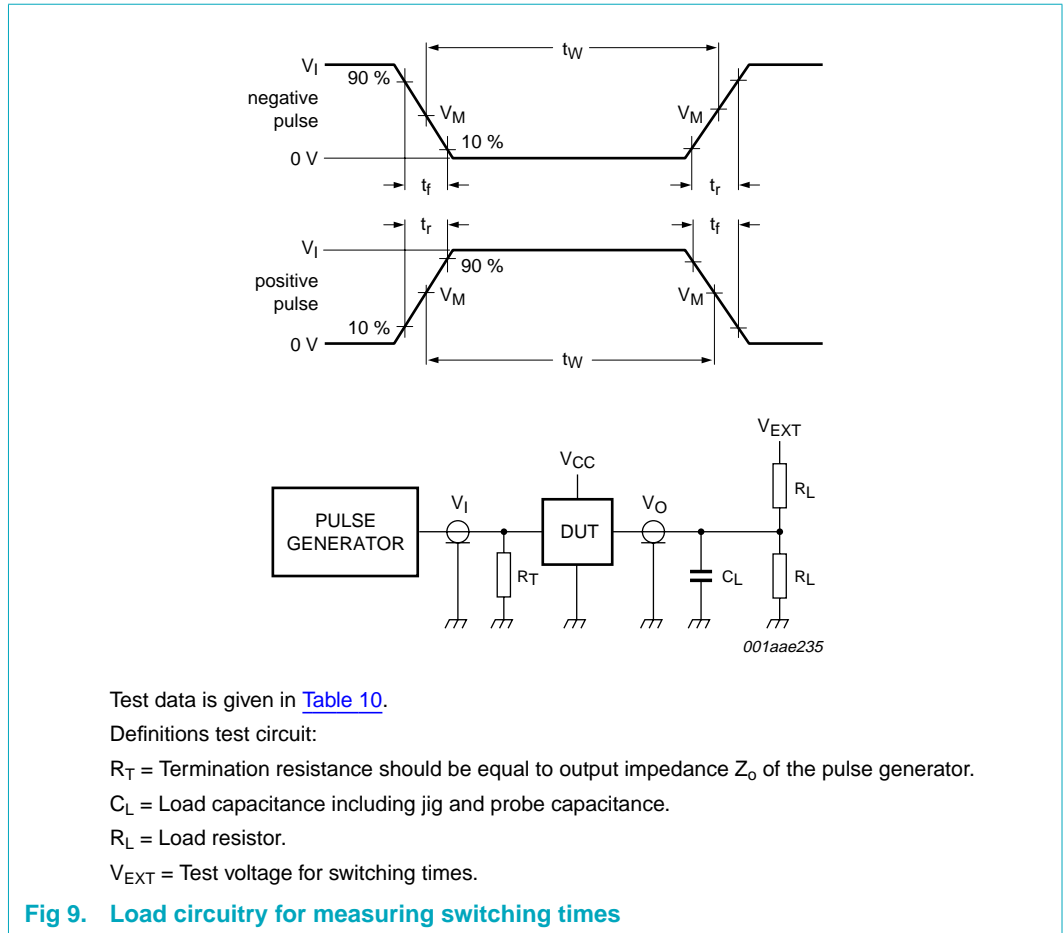


Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

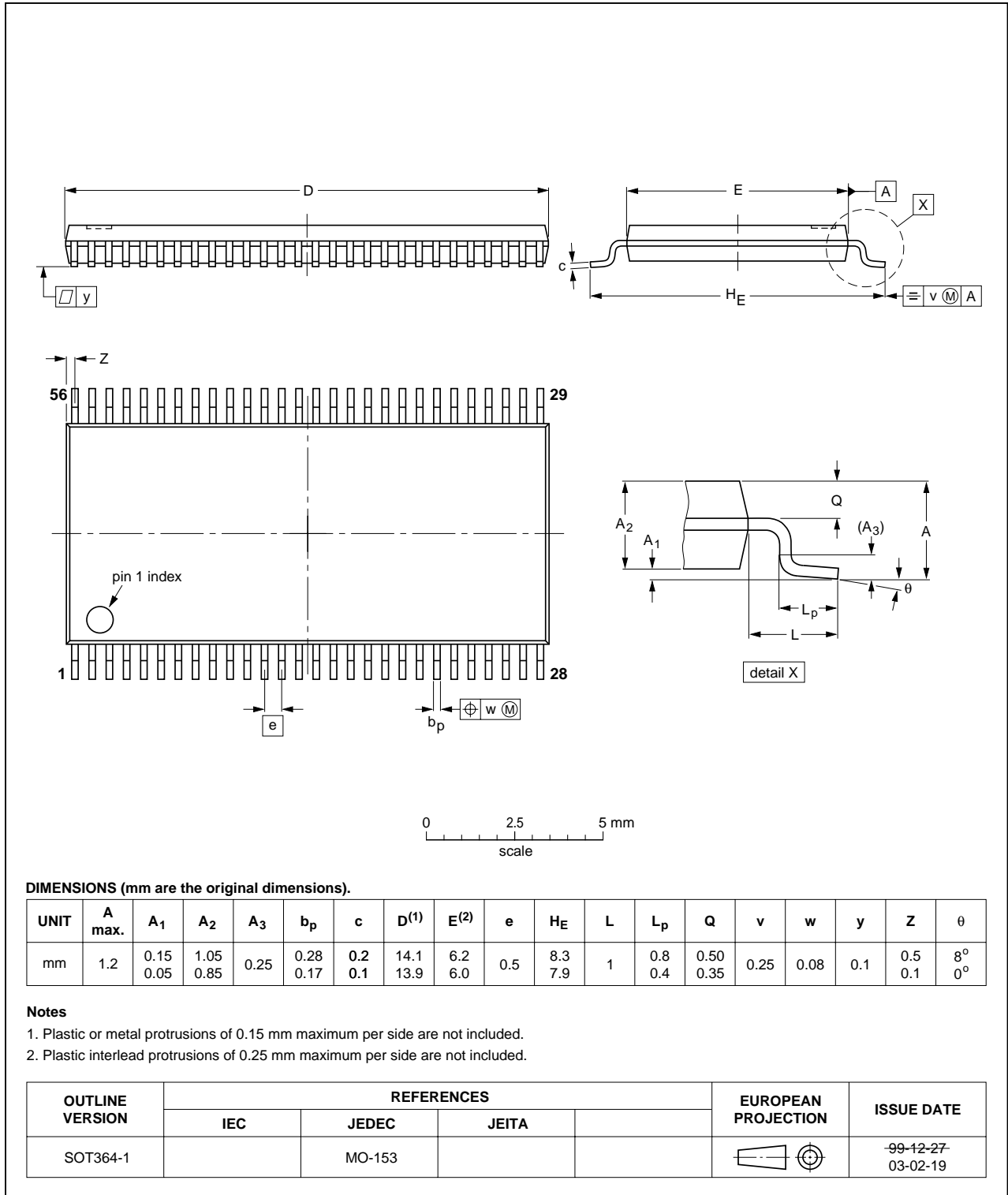


Fig 10. Package outline SOT364-1 (TSSOP56)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16952_2	20060427	Product data sheet	-	74ALVCH16952_1
Modifications:		<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips SemiconductorsThe symbol of pin numbers 15, 16, 17, 19, 20, 21, 23 and 24 is rectified		
74ALVCH16952_1 (9397 750 04563)	19980901	Preliminary specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Philips Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Philips Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, Philips Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — Philips Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Philips Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a Philips Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Philips Semiconductors accepts no liability for inclusion and/or use of Philips Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — Philips Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.semiconductors.philips.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Philips Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

18. Contents

1	General description	1
2	Features	1
3	Quick reference data	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	5
6.1	Pinning	5
6.2	Pin description	5
7	Functional description	7
7.1	Function table	7
8	Limiting values	8
9	Recommended operating conditions	8
10	Static characteristics	9
11	Dynamic characteristics	10
12	Waveforms	11
13	Package outline	14
14	Abbreviations	15
15	Revision history	15
16	Legal information	16
16.1	Data sheet status	16
16.2	Definitions	16
16.3	Disclaimers	16
16.4	Trademarks	16
17	Contact information	16
18	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© Koninklijke Philips Electronics N.V. 2006. All rights reserved.

For more information, please visit: <http://www.semiconductors.philips.com>.

For sales office addresses, email to: sales.addresses@www.semiconductors.philips.com.

Date of release: 27 April 2006

Document identifier: 74ALVCH16952_2