

### Features

- Low  $C_{RES} / C_{IES}$  ratio (no cross conduction susceptibility)
- High frequency operation

### Applications

- High frequency inverters, UPS
- Motor drivers
- HF, SMPS and PFC in both hard switch and resonant topologies
- Welding
- Induction heating

### Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

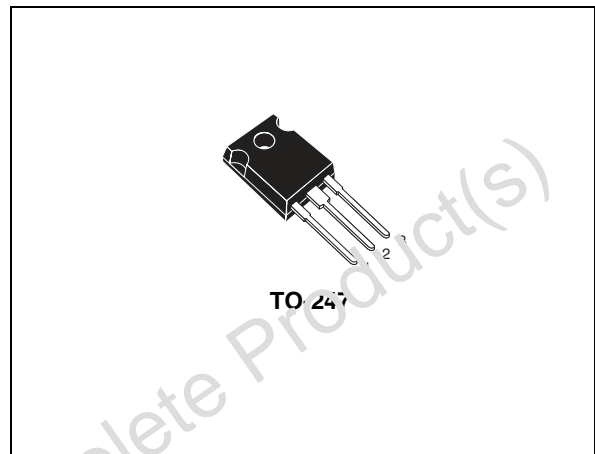


Figure 1. Internal schematic diagram

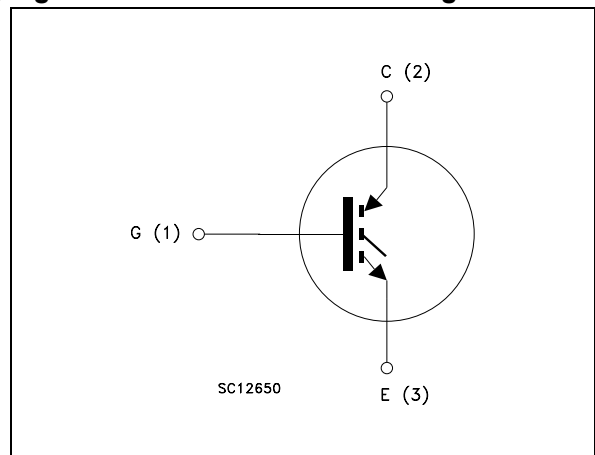


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW40NC60W	GW40NC60W	TO-247	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{GE} = 0$ )	600	V
$I_C^{(1)}$	Collector current (continuous) at 25 °C	70	A
$I_C^{(1)}$	Collector current (continuous) at 100 °C	40	A
$I_{CL}^{(2)}$	Turn-off latching current	230	A
$I_{CP}^{(3)}$	Pulsed collector current	230	A
$V_{GE}$	Gate-emitter voltage	±20	V
$P_{TOT}$	Total dissipation at $T_C = 25$ °C	250	W
$T_j$	Operating junction temperature	-55 to 150	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C) \cdot I_C}$$

2.  $V_{clamp} = 80\%(V_{CES})$ ,  $T_j = 150$  °C,  $R_G = 10$  Ω,  $V_{GE} = 15$  V

3. Pulse width limited by max. junction temperature allowed

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	°C/W

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage ( $V_{GE} = 0$ )	$I_C = 1\text{ mA}$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$ , $I_C = 30\text{ A}$ $V_{GE} = 15\text{ V}$ , $I_C = 30\text{ A}$ , $T_C = 125\text{ °C}$		2.1 1.9	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$ , $I_C = 250\mu\text{A}$	3.75		5.75	V
$I_{CES}$	Collector-emitter cut-off current ( $V_{GE} = 0$ )	$V_{GE} = 600\text{ V}$ $V_{GE} = 600\text{ V}$ , $T_C = 125\text{ °C}$			500 5	$\mu\text{A}$ mA
$I_{GES}$	Gate-emitter cut-off current ( $V_{CE} = 0$ )	$V_{GE} = \pm 20\text{ V}$			$\pm 100$	nA
$g_{fs}$	Forward transconductance	$V_{CE} = 15\text{ V}$ , $I_C = 30\text{ A}$		20		S

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$	Input capacitance	$V_{CE} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GE} = 0$		2900		pF
$C_{oes}$	Output capacitance			298		pF
$C_{res}$	Reverse transfer capacitance			59		pF
$Q_g$	Total gate charge	$V_{CE} = 390\text{ V}$ , $I_C = 30\text{ A}$ ,		126		nC
$Q_{ge}$	Gate-emitter charge	$V_{GE} = 15\text{ V}$		16		nC
$Q_{jc}$	Gate-collector charge	(see Figure 17)		46		nC

**Table 6. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}, I_C = 30\text{ A}$		33		ns
$t_r$	Current rise time	$R_G = 10\ \Omega, V_{GE} = 15\text{ V}$		12		ns
$(di/dt)_{on}$	Turn-on current slope	(see Figure 16)		2600		A/ $\mu$ s
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}, I_C = 30\text{ A}$		32		ns
$t_r$	Current rise time	$R_G = 10\ \Omega, V_{GE} = 15\text{ V},$		14		ns
$(di/dt)_{on}$	Turn-on current slope	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)		2300		A/ $\mu$ s
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390\text{ V}, I_C = 30\text{ A},$		26		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\ \Omega, V_{GE} = 15\text{ V}$		168		ns
$t_f$	Current fall time	(see Figure 16)		36		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390\text{ V}, I_C = 30\text{ A},$		54		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\ \Omega, V_{GE} = 15\text{ V}$		213		ns
$t_f$	Current fall time	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)		67		ns

**Table 7. Switching energy (inductive load)**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390\text{ V}, I_C = 30\text{ A}$		302		$\mu$ J
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\ \Omega, V_{GE} = 15\text{ V}$		349		$\mu$ J
$E_{ts}$	Total switching losses	(see Figure 16)		651		$\mu$ J
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390\text{ V}, I_C = 30\text{ A}$		553		$\mu$ J
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\ \Omega, V_{GE} = 15\text{ V},$		750		$\mu$ J
$E_{ts}$	Total switching losses	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)		1303		$\mu$ J

$E_{on}^{(1)}$  is the turn-on losses when a typical diode is used in the test circuit in figure 2  $E_{on}$  include diode recovery energy. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & diode are at the same temperature (25 °C and 125 °C)

2. Turn-off losses include also the tail of the collector current

## 2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

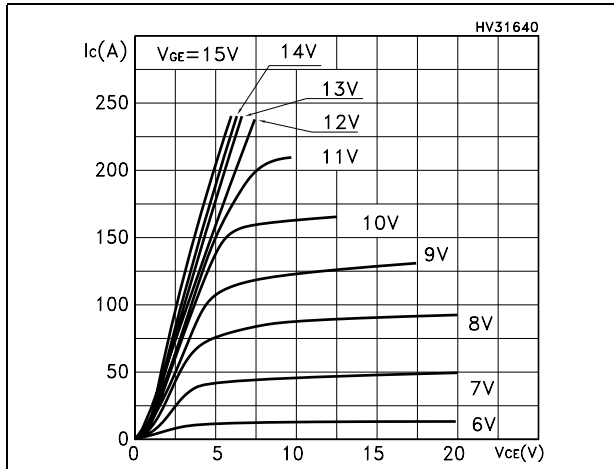


Figure 3. Transfer characteristics

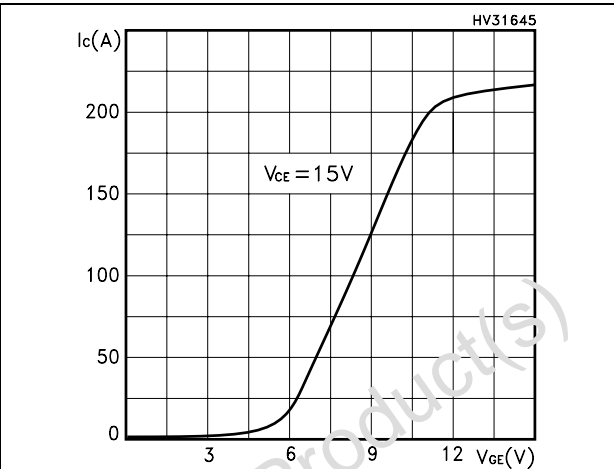


Figure 4. Transconductance

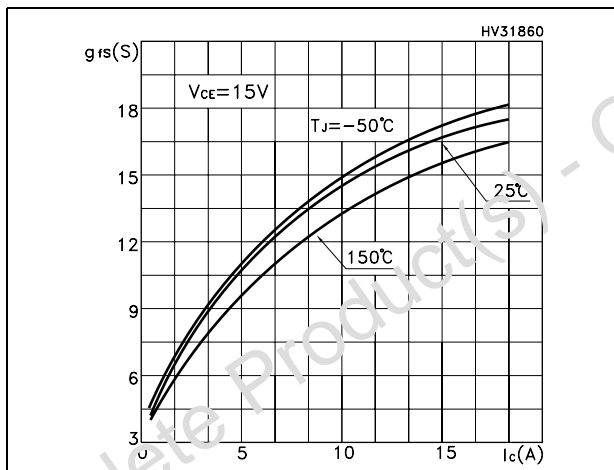


Figure 5. Collector-emitter on voltage vs temperature

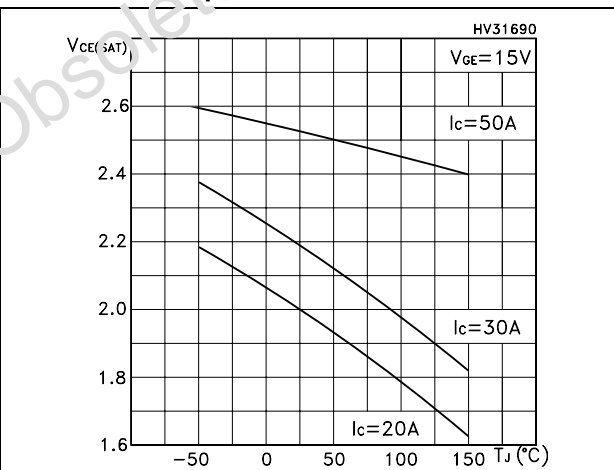


Figure 6. Collector-emitter on voltage vs collector current

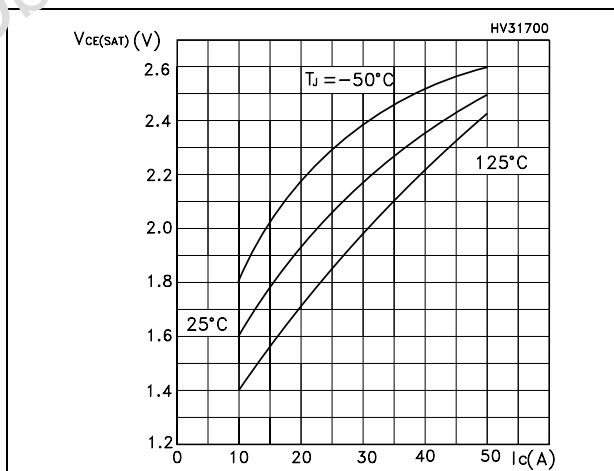


Figure 7. Normalized gate threshold vs temperature

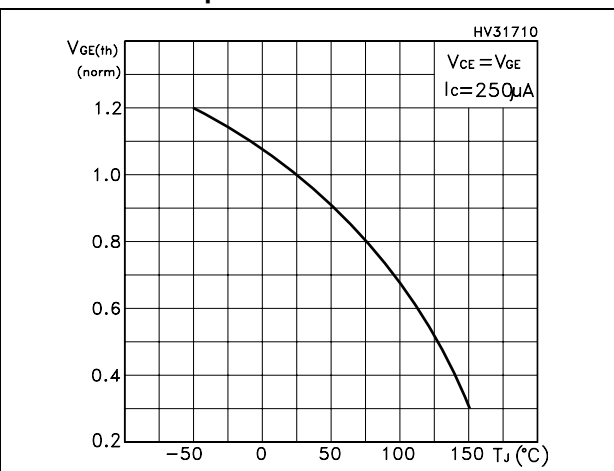


Figure 8. Normalized breakdown voltage vs temperature

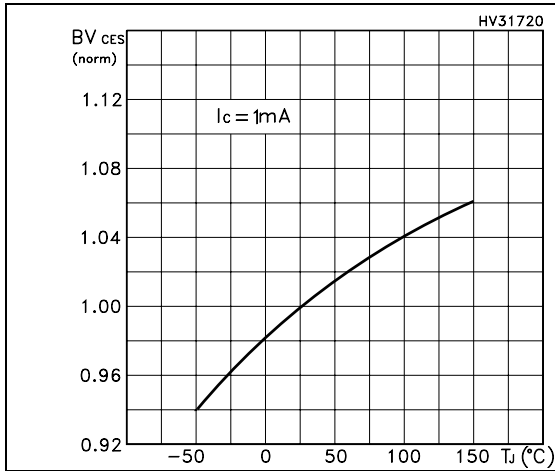


Figure 9. Gate charge vs gate-emitter voltage

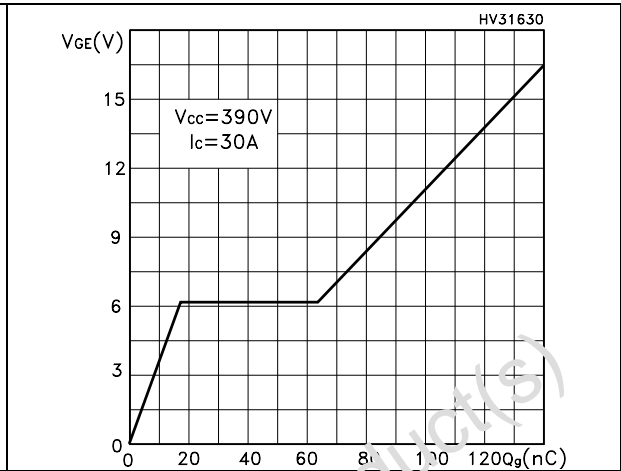


Figure 10. Capacitance variations

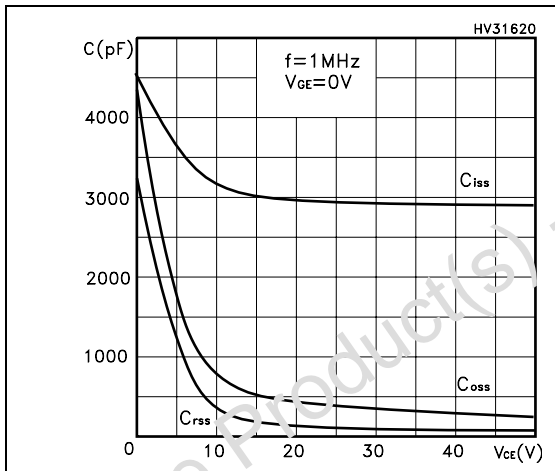


Figure 11. Switching losses vs temperature

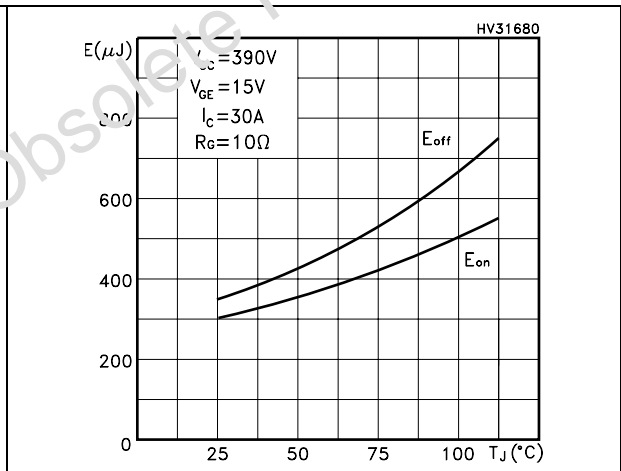


Figure 12. Switching losses vs gate resistance

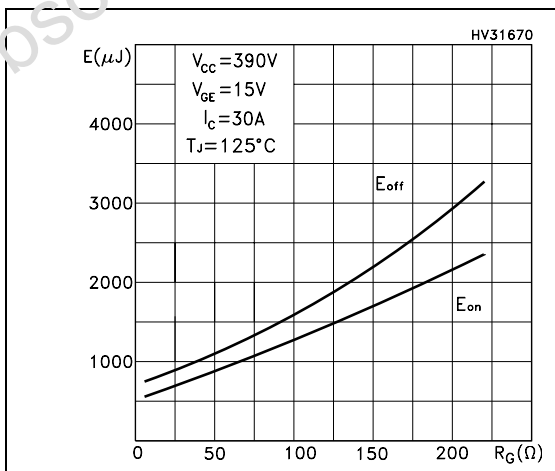


Figure 13. Switching losses vs collector current

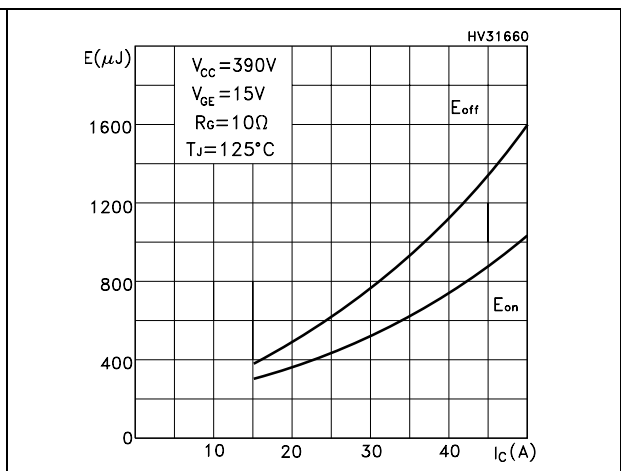


Figure 14. Thermal impedance

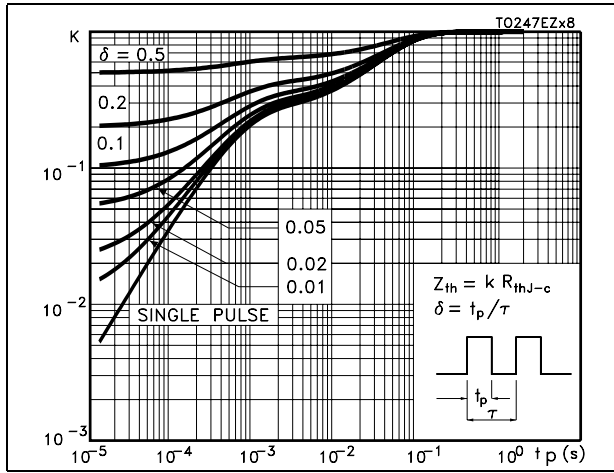
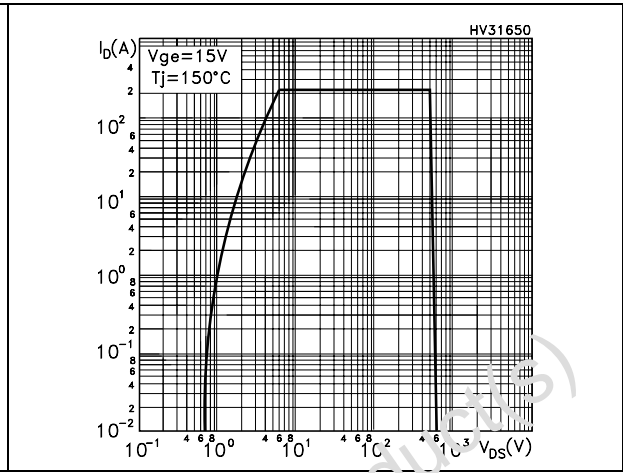


Figure 15. Turn-off SOA



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### 3 Test circuit

Figure 16. Test circuit for inductive load switching

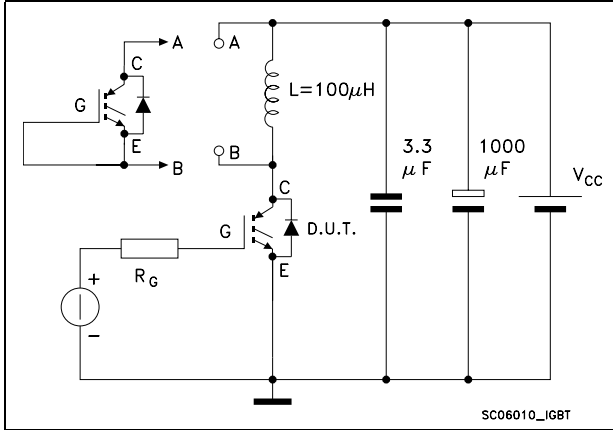


Figure 17. Gate charge test circuit

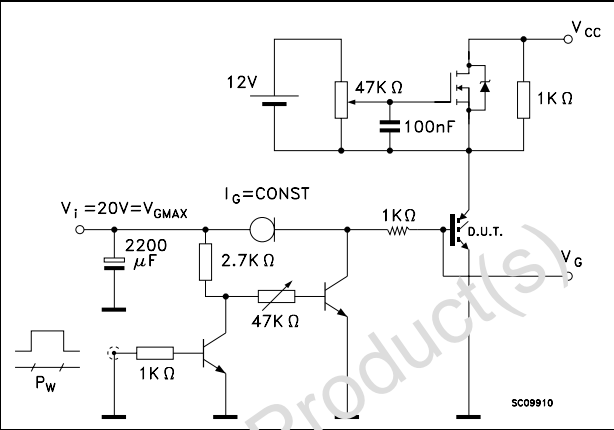
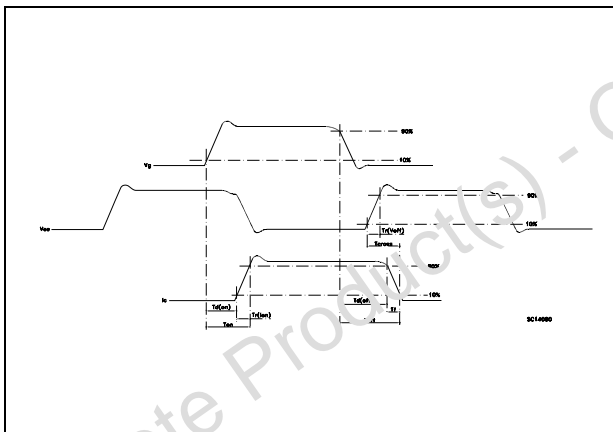


Figure 18. Switching waveforms



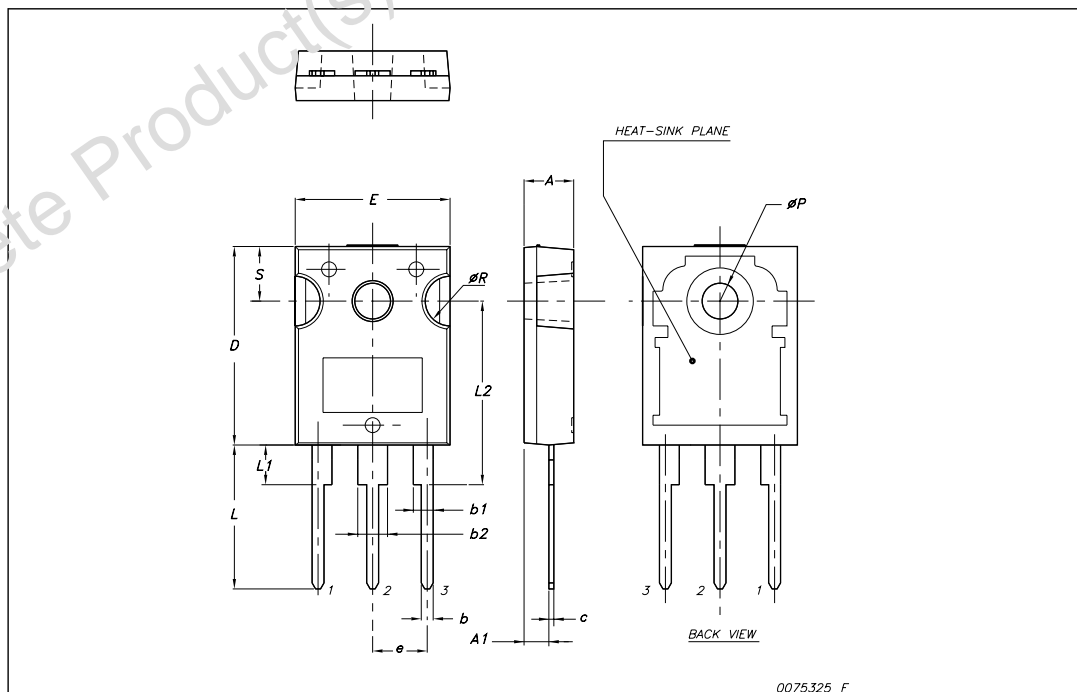
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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## TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
09-Jul-2008	1	First release

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