

CTS100LVEL11

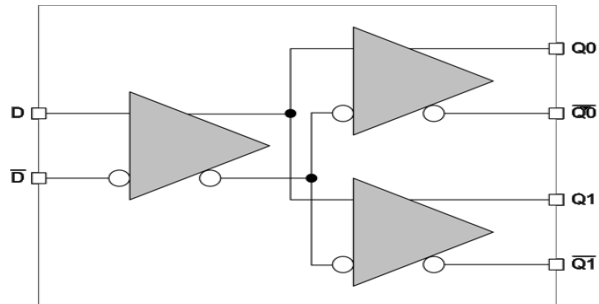
LVPECL 1:2 Differential Fan-out Buffer
MLP8, MSOP8, SOIC8

Not recommended for new designs

FEATURES

- 265ps Propagation Delay
- 5ps Skew Between Outputs
- Internal Input Pull-Down Resistors
- Direct Replace for ON Semi MC100LVEL11 and MC100EL11
- RoHS Compliant Pb Free Packages

BLOCK DIAGRAM



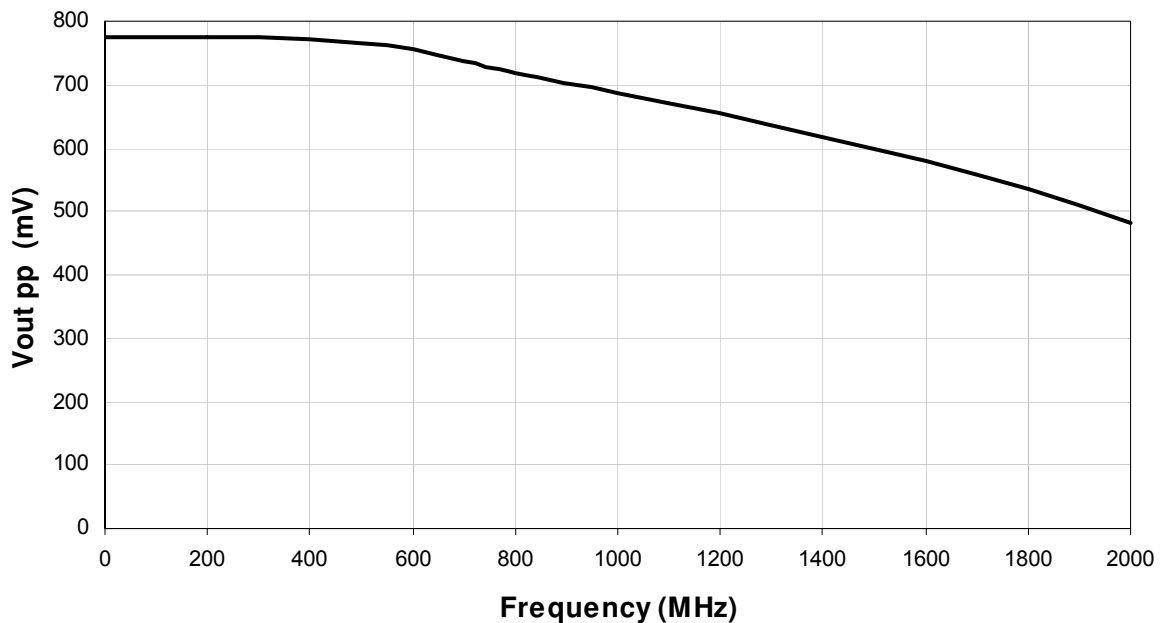
DESCRIPTION

The CTS100LVEL11 is a differential 1:2 fan-out gate. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the CTS100LVEL11 is ideally suited for those applications that require the ultimate in AC performance.

The differential inputs of the CTS100LVEL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open, the Q outputs will go LOW.

The CTS100LVEL11 is a direct replacement for the ON Semi MC100LVEL11 and MC100EL11.

ENGINEERING NOTES



Typical Output Swing

ELECTRICAL SPECIFICATIONS
Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	$V_{EE} = 0V$	0 to +8.0	V
V_I	PECL Input Voltage	$V_{EE} = 0V$	0 to +6.0	V
V_{EE}	ECL Power Supply	$V_{CC} = 0V$	-8.0 to 0	V
V_I	ECL Input Voltage	$V_{CC} = 0V$	-6.0 to 0	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
ESD_{HBM}	Human Body Model		2500	V
ESD_{MM}	Machine Model		200	V
ESD_{CDM}	Charged Device Model		2500	V

ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ¹	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ¹	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
I_{IL}	Input LOW Current	-150			-150			-150			-150			µA
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		22	31		23	31		24	31		28	34	mA

¹ Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

LVPECL DC Characteristics (VEE = GND, VCC = +3.3V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ¹	2215	2295	2420	2275	2345	2420	2275	2345	2420	2275	2345	2420	mV
V _{OL}	Output LOW Voltage ¹	1470	1605	1745	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V _{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	1490		1825	mV
I _{IL}	Input LOW Current	-150			-150			-150			-150			μA
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{EE}	Power Supply Current		22	31		23	31		24	31		28	34	mA

¹ Each output is terminated through a 50Ω resistor to V_{CC} -2V.

PECL DC Characteristics (VEE = GND, VCC = +5.0V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ¹	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V _{OL}	Output LOW Voltage ¹	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V _{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	3190		3525	mV
I _{IL}	Input LOW Current	-150			-150			-150			-150			μA
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{EE}	Power Supply Current		22	31		23	31		24	31		28	34	mA

¹ Each output is terminated through a 50Ω resistor to V_{CC} -2V.

AC Characteristics [V_{EE} = -3.0V to -5.5V, V_{CC} = GND or V_{EE} = GND, V_{CC} = +3.0V to +5.0V]

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} /t _{PHL}	Propagation Delay to Output	135	260	335	185	260	335	190	265	340	215	310	365	ps
t _{SKEW}	Duty Cycle Skew ¹		5			5	20		5	20		5	20	ps
	Within Device Skew ²		5			5	20		5	20		5	20	ps
V _{PP}	Minimum Input Swing ³	150			150			150			150			mV
V _{CMR}	Common Mode Range ⁴	V _{EE} +1.2		V _{CC} -0.2	V _{EE} +1.2		V _{CC} -0.2	V _{EE} +1.2		V _{CC} -0.2	V _{EE} +1.2		V _{CC} -0.2	V
t _R /t _F	Output Rise/Fall Times Q (20%-80%)	100		260	100		260	100		260	100		260	ps

¹ Within-device skew defined as identical transitions on similar paths through a device.

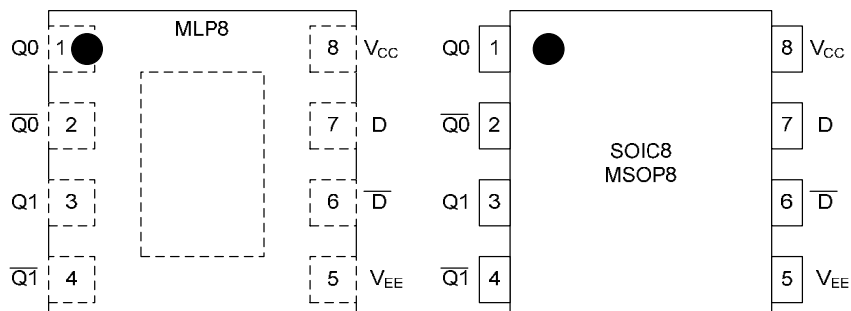
² Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

³ V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters guaranteed. The device has a DC gain of 40.

The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min) and 1V.

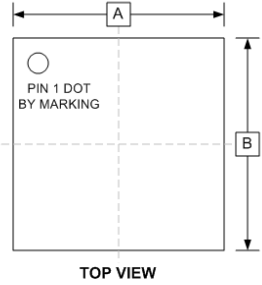
Pin Description and Configuration
Pin Assignments

Pin	Name	Type	Function
1	Q0	Input	Data Input
2	$\overline{Q0}$	Input	Data Input
3	Q1	Input	Data Input
4	$\overline{Q1}$	Output	Data Input
5	V _{EE}	Power	Negative Supply
6	\overline{D}	Output	Data Output
7	D	Output	Data Output
8	V _{CC}	Power	Positive Supply

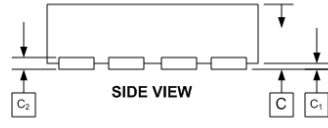
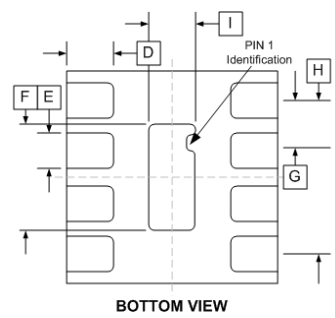

Pin Configuration for MLP8 & SOIC8/MSOP8

For MLP8, leave center bottom pad open or connect to V_{EE}

PACKAGE DIMENSIONS

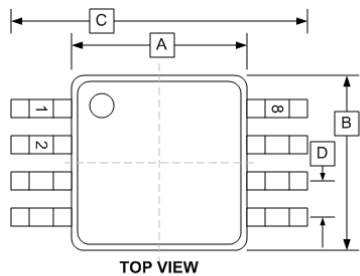
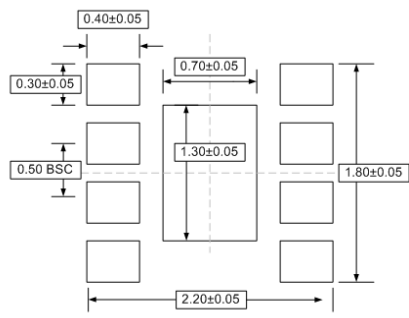


MLP8 (N)

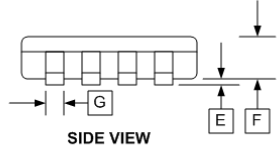
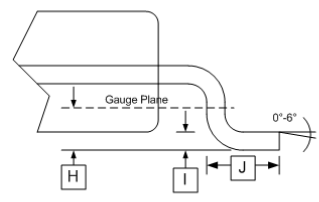


MILLIMETERS		
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C ₁	0.00	0.05
C ₂	0.203	Ref.
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500	BSC
H	1.500	REF
I	0.60±0.050	

PCB LAND PATTERN/FOOTPRINT

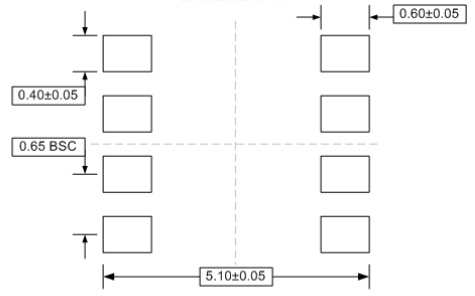


MSOP8 (T)



INCHES		
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256	TYP
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

PCB LAND PATTERN/FOOTPRINT
Dimensions in mm

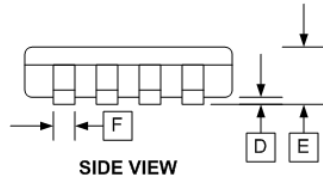
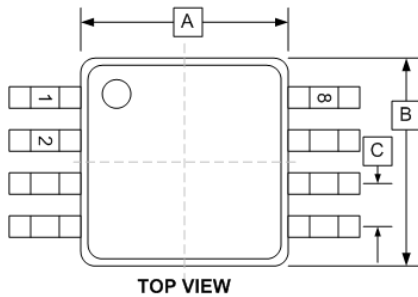


CTS100LVEL11

LVPECL 1:2 Differential Fan-out Buffer
MLP8, MSOP8, SOIC8

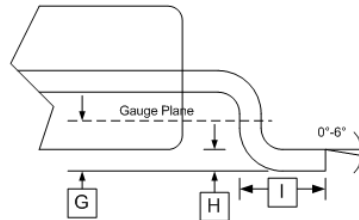
Not recommended for new designs

PACKAGE DIMENSIONS

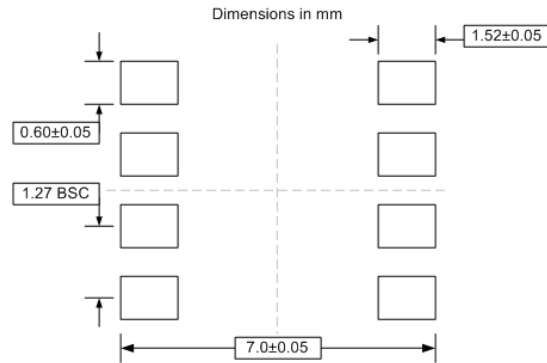


DIM	mm	
	MIN	MAX
A	3.81	3.99
B	4.80	4.98
C	1.27 BSC	
D	0.10	0.25
E	1.37	1.68
F	0.36	0.48
G	0.25	
H	0.19	0.25
I	0.41	0.86

SOIC8 (D)



PCB LAND PATTERN/FOOTPRINT



PART ORDERING INFORMATION

Part Number	Package	Marking
CTS100LVEL11NG	MLP8	L1G / YWW
CTS100LVEL11DG	SOIC8	CTS100G / LVEL11 / YYWW
CTS100LVEL11TG	MSOP8	HL11G / YYWW