PCM6020-Q1 Automotive, 2-Channel, 768-kHz, Audio ADC With Integrated Microphone Bias and Input Fault Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C ≤ T_A ≤ +125°C
- ADC performance:
  - Line differential input dynamic range: 110 dB
  - Microphone differential input dynamic range: 110 dB
  - THD+N: –94 dB
  - Channel summing mode supports high SNR
- ADC input voltage:
  - Differential, 10-V_{RMS} full-scale inputs
  - Single-ended, 5-V_{RMS} full-scale inputs
- ADC sample rate (f_S) = 8 kHz to 768 kHz
- Programmable channel settings:
  - Channel gain: 0 dB to 42 dB, 1-dB steps
  - Digital volume control: –100 dB to 27 dB
  - Gain calibration with 0.1-dB resolution
  - Phase calibration with 163-ns resolution
- Programmable microphone bias (5 V to 9 V):
  - With integrated efficient boost converter
- Programmable microphone input fault diagnostics:
  - Open inputs or shorted inputs
  - Short to ground, MICBIAS, or VBAT
  - Microphone bias over current protection
- Low-latency signal processing filter selection
- Programmable HPF and biquad digital filters
- I^2C or SPI controls
- Audio serial data interface:
  - Format: TDM, I^2S, or left-justified (LJ)
  - Word length: 16 bits, 20 bits, 24 bits, or 32 bits
  - Master or slave interface
- Single-supply, 3.3-V operation
- I/O supply operation: 3.3 V or 1.8 V
- Power consumption:
  - < 21.5 mW/channel at 48-kHz

2 Applications

- Emergency call (eCall)
- Telematics control unit
- Automotive head units
- Automotive external amplifiers

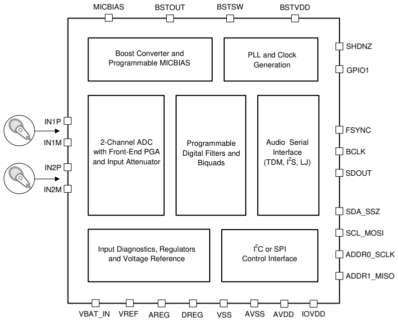
3 Description

The PCM6020-Q1 is a 2-channel high-performance, audio analog-to-digital converter (ADC) that supports analog input signals up to 10 V_{RMS}. The PCM6020-Q1 supports line and microphone inputs, and allows for both single-ended and differential input configurations. This device offers an integrated high-voltage, programmable microphone bias, and input diagnostic circuitry that allows direct connection to microphone-based automotive systems with full fault diagnostic capability for direct-coupled inputs. The PCM6020-Q1 integrates an efficient boost converter to generate a high voltage microphone bias using an external, low-voltage, 3.3-V supply, which is a readily available supply in the system to generate the high-voltage, programmable microphone bias. The PCM6020-Q1 integrates the programable channel gain, digital volume control, a low-jitter phase-locked loop (PLL), a programmable high-pass filter (HPF), biquad filters, low-latency filter modes, and allows for sample rates up to 768 kHz. The PCM6020-Q1 supports time-division multiplexing (TDM), I^2S, or left-justified (LJ) audio formats, and can be controlled with either the I^2C or SPI interface. These integrated high-performance features, along with a single, 3.3-V supply operation, make the PCM6020-Q1 device along with PCM6xx0-Q1 device family an excellent choice for scalable, space-constrained automotive systems. The PCM6020-Q1 is part of a larger PCM6xx0-Q1 device family, available for download at ti.com.

Device Information [1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM6020-Q1	WQFN (32)	5.00 mm x 5.00 mm with 0.5-mm pitch

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Application Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

5 Device Comparison Table

FEATURE	PCM6020-Q1	PCM6240-Q1	PCM6260-Q1	PCM6480-Q1	PCM6340-Q1	PCM6360-Q1
Control interface	I^{2}C or SPI					
Digital audio serial interface	TDM or I^{2}S or left-justified (LJ)					
Audio analog channel	2	4	6	4	4	6
Audio PDM input channel	0	0	0	4	0	0
General-purpose input or output pins	5	5	1	5 (multiplexed with PDM interface)	5	1
Microphone bias voltage	Programmable 5 V to 9 V in steps of 0.5 V					
Microphone bias LDO supply	Generated using integrated efficient boost converter with external low-voltage BSTVDD = 3.3-V supply				Powered directly using external high-voltage HVDD (as high as 12 V) supply	
Input fault diagnostics	Comprehensive input fault diagnostics for DC-coupled microphone inputs with programmable thresholds					
Package	WQFN (RTV), 32-pin, 5.00 mm x 5.00 mm (0.5-mm pitch)					
Compatibility	Package, and control registers compatible; replacements of each other. See the *Scalable Automotive Audio Solutions Using the PCM6xx0-Q1 Family of Products* application report for further details.					

6 Pin Configuration and Functions

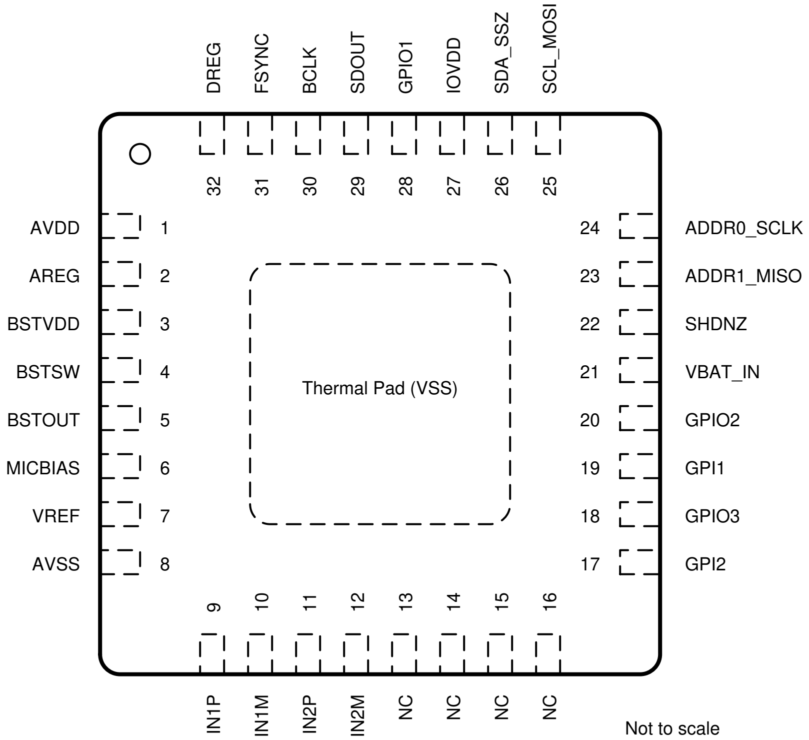


Figure 6-1. RTV Package, 32-Pin WQFN With Exposed Thermal Pad, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	Analog supply	Analog power (3.3 V, nominal)
2	AREG	Analog supply	Analog regulator output voltage for analog supply (1.8 V, nominal)
3	BSTVDD	Analog supply	Boost converter supply voltage
4	BSTSW	Analog supply	Boost converter switch input
5	BSTOUT	Analog supply	Boost converter output voltage
6	MICBIAS	Analog	MICBIAS output (programmable output up to 9 V)

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	VREF	Analog	Analog reference voltage filter output
8	AVSS	Analog supply	Analog ground; short directly to the board ground plane
9	IN1P	Analog input	Analog input 1P pin
10	IN1M	Analog input	Analog input 1M pin
11	IN2P	Analog input	Analog input 2P pin
12	IN2M	Analog input	Analog input 2M pin
13	NC	—	Not used; pin must be grounded
14	NC	—	Not used; pin must be grounded
15	NC	—	Not used; pin must be grounded
16	NC	—	Not used; pin must be grounded
17	GPI2	Digital input	General-purpose digital input-2 (multipurpose functions such as daisy-chain input, PLL input clock source, and so on)
18	GPIO3	Digital I/O	General-purpose digital input/output-4 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so on)
19	GPI1	Digital input	General-purpose digital input-1 (multipurpose functions such as daisy-chain input, PLL input clock source, and so on)
20	GPIO2	Digital I/O	General-purpose digital input/output-2 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so on)
21	VBAT_IN	Analog	Analog VBAT input monitoring pin (used for input diagnostics)
22	SHDNZ	Digital input	Device hardware shutdown and reset (active low)
23	ADDR1_MISO	Digital I/O	For I^2C operation: I^2C slave address A1 pin. For SPI operation: SPI slave output pin.
24	ADDR0_SCLK	Digital input	For I^2C operation: I^2C slave address A0 pin. For SPI operation: SPI serial bit clock.
25	SCL_MOSI	Digital input	For I^2C operation: clock pin for I^2C control bus. For SPI operation: SPI slave input pin.
26	SDA_SSZ	Digital I/O	For I^2C operation: data pin for I^2C control bus. For SPI operation: SPI slave select pin.
27	IOVDD	Digital supply	Digital I/O power supply (1.8 V or 3.3 V, nominal)
28	GPIO1	Digital I/O	General-purpose digital input/output-1 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so on)
29	SDOUT	Digital output	Audio serial data interface bus output
30	BCLK	Digital I/O	Audio serial data interface bus bit clock
31	FSYNC	Digital I/O	Audio serial data interface bus frame synchronization signal
32	DREG	Digital supply	Digital regulator output voltage for digital core supply (1.5 V, nominal)
Thermal Pad	Thermal Pad (VSS)	Ground supply	Thermal pad shorted to the internal device ground. Short the thermal pad directly to the board ground plane.

7 Specifications

7.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	BSTVDD to VSS (thermal pad)	–0.3	3.9	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Battery voltage	VBAT_IN to AVSS	–0.3	18	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	18	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner package pins	±750	
			All other non-corner package pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD(1)	Analog supply voltage to AVSS	3.0	3.3	3.6	V
BSTVDD	Boost converter supply voltage to VSS (thermal pad)	3.0	3.3	3.6	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
INPUTS					
VBAT_IN	VBAT_IN input pin voltage to AVSS	0	12.6	18	V
INxx	Analog input pins voltage to AVSS for line-in recording	0		14.2	V
	Analog input pins voltage to AVSS for microphone recording	0.1		MICBIAS – 0.1	V
	Analog input pins voltage to AVSS during short to VBAT_IN			VBAT_IN	V
	Digital input pins voltage to VSS (thermal pad)	0		IOVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

		MIN	NOM	MAX	UNIT
OTHERS					
	GPIOx or GPIx (used as MCLK input) clock frequency			36.864[2]	MHz
C_b	SCL and SDA bus capacitance for I^2C interface supports standard-mode and fast-mode			400	pF
	SCL and SDA bus capacitance for I^2C interface supports fast-mode plus			550	
C_L	Digital output load capacitance		20	50	pF
	Boost converter inductor for 6MHz clocking mode (recommended inductor CIGW201610GL2R2MLE)		2.2		µH

(1) AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

(2) MCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5 ns. For better audio noise performance, MCLK input must be used with low jitter.

7.4 Thermal Information

THERMAL METRIC[1]		PCM6020-Q1	UNIT
		RTV (WQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR LINE INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input, input fault diagnostic not supported		10		V_{RMS}
		DC-coupled input, DC common-mode voltage INxP = INxM = 7.1 V, input fault diagnostic not supported				
	Single-ended input full-scale AC signal voltage	AC-coupled input, input fault diagnostic not supported		5		V_{RMS}
		DC-coupled input, DC common-mode voltage INxP = INxM = 7.1 V, input fault diagnostic not supported				
SNR	Signal-to-noise ratio, A-weighted[1] [2]	IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain	105	110		dB
		IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		110		
		IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain		101		

7.5 Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DR	Dynamic range, A-weighted(2)	IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		110		dB
		IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		110		
		IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain		101		
THD+N	Total harmonic distortion(2)	IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–95	–78	dB
		IN1 differential DC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–95		
		IN1 differential DC-coupled input selected and –13-dB full-scale AC signal input, 12-dB channel gain		–91		
	Channel gain control range	Programmable 1-dB steps	0		42	dB
ADC PERFORMANCE FOR MICROPHONE INPUT RECORDING						
	Differential input full-scale AC signal voltage(3)	AC-coupled input, input fault diagnostic not supported. CHx_MIC_RANGE register bit is set to high.		10		V_{RMS}
		DC-coupled input, DC differential common-mode voltage INxP – INxM > 3.4 V, DC common-mode voltage INxP < (MICBIAS – 1.7 V) and DC common-mode voltage INxM > 1.7 V. CHx_MIC_RANGE register bit is set to high to support AC differential signal max swing > 2 Vrms(4).				
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		110		dB
		IN1 differential DC-coupled input selected and AC-signal shorted to ground, DC differential common-mode voltage IN1P – IN1M < 5.0 V, 0-dB channel gain	105	110		
DR	Dynamic range, A-weighted(2)	IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		110		dB
		IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, DC differential common-mode voltage IN1P – IN1M < 5.0 V, 0-dB channel gain		110		
THD+N	Total harmonic distortion(2)	IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–92		dB
		IN1 differential DC-coupled input selected and –15-dB full-scale AC signal input, 0-dB channel gain		–90	–78	
	Channel gain control range	Programmable 1-dB steps	0		42	dB
ADC OTHER PARAMETERS						
	Input impedance	Differential input, between INxP and INxM		50		kΩ
		Single-ended input, between INxP and INxM		25		
	Digital volume control range	Programmable 0.5-dB steps	–100		27	dB

7.5 Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Output data sample rate	Programmable	7.35		768	kHz
	Output data sample word length	Programmable	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		12		Hz
	Interchannel isolation	–1-dB full-scale AC signal line-in input to non measurement channel		–134		dB
	Interchannel gain mismatch	–6-dB full-scale AC signal line-in input, 0-dB channel gain		0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		92		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 0-dB channel gain, 1-V_{RMS} AC input, 1-kHz signal on both pins and measure level at output, CHx_CFG0 D3-2 register bits set to 2b'10 to configure device in high CMRR performance mode		70		dB
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS		6.8		μV_{RMS}
	MICBIAS voltage	Programmable 0.5-V steps	5		9	V
	MICBIAS current drive	MICBIAS voltage 9 V			80	mA
	MICBIAS load regulation	MICBIAS voltage 9 V, measured up to maximum load	0		1	%
	MICBIAS over current protection threshold	MICBIAS voltage 9 V	82			mA
INPUT DIAGNOSTICS						
	Fault monitoring repetition rate	Programmable, DC-coupled input	1	4	8	ms
	Fault response time	Fault monitoring repetition rate 4-ms, DC-coupled input		16		ms
	Threshold voltage for (INxx – AVSS) input shorted to ground	Programmable 60-mV steps, DC-coupled input	0		900	mV
	Threshold voltage for (INxP – INxM) input shorted together	Programmable 30-mV steps, DC-coupled input	0		450	mV
	Threshold voltage for (MICBIAS – INxx) input shorted to MICBIAS	Programmable 30-mV steps, DC-coupled input	0		450	mV
	Threshold voltage for (VBAT – INxx) input shorted to VBAT_IN	Programmable 30-mV steps, DC-coupled input	0		450	mV
DIGITAL I/O						
$V_{IL(SHDNZ)}$	Low-level digital input logic voltage threshold	SHDNZ pin	–0.3		0.25 × IOVDD	V
$V_{IH(SHDNZ)}$	High-level digital input logic voltage threshold	SHDNZ pin	0.75 × IOVDD		IOVDD + 0.3	V

7.5 Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except SDA and SCL, IOVDD 1.8-V operation	–0.3		0.35 × IOVDD	V
		All digital pins except SDA and SCL, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins except SDA and SCL, IOVDD 1.8-V operation	0.65 × IOVDD		IOVDD + 0.3	V
		All digital pins except SDA and SCL, IOVDD 3.3-V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins except SDA and SCL, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins except SDA and SCL, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins except SDA and SCL, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins except SDA and SCL, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold	SDA and SCL	–0.5		0.3 × IOVDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold	SDA and SCL	0.7 × IOVDD		IOVDD + 0.5	V
$V_{OL1(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –3 mA, IOVDD > 2 V			0.4	V
$V_{OL2(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –2 mA, IOVDD ≤ 2 V			0.2 x IOVDD	V
$I_{OL(I2C)}$	Low-level digital output current	SDA, $V_{OL(I2C)}$ = 0.4 V, standard-mode or fast-mode	3			mA
		SDA, $V_{OL(I2C)}$ = 0.4 V, fast-mode plus	20			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V	–5	0.1	5	µA
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in hardware shutdown mode	SHDNZ = 0, all device external clocks stopped		0.5		µA
I_{BSTVDD}				0.1		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All device external clocks stopped		4		µA
I_{BSTVDD}				0.1		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption when MICBIAS ON, MICBIAS voltage 9 V, 40 mA load, ADC off	f_S = 48 kHz, BCLK = 256 × f_S		2.1		mA
I_{BSTVDD}				162.5		
I_{IOVDD}				0.01		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 16-kHz	MICBIAS off, PLL on, BCLK = 512 × f_S		13.9		mA
I_{BSTVDD}				0		
I_{IOVDD}				0.1		

7.5 Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 48-kHz	MICBIAS off, PLL off, BCLK = 512 × f_S		13.7		mA
I_{BSTVDD}				0		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 48-kHz	MICBIAS off, PLL on, BCLK = 256 × f_S		15.1		mA
I_{BSTVDD}				0		
I_{IOVDD}				0.2		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

(3) Microphone inputs support a 2 V_{RMS} differential input full-scale AC signal voltage, if the CHx_MIC_RANGE register bit is set to low (default value). However, if the input DC common-mode differential voltage is higher than 4 V, then TI recommends setting the CHx_MIC_RANGE register bit high to avoid any saturation resulting from the high input DC common-mode differential voltage.

(4) If the CHx_MIC_RANGE register bit is set to high (default value is low) in DC-coupled input configuration mode, then the input differential DC common-mode along with input differential AC signal must be less than 10 V_{RMS} for differential input configuration mode. Similarly, for single-ended input configuration mode, the input DC common-mode voltage along with the input AC signal must be less than 5 V_{RMS} .

7.6 Timing Requirements: I^{2}C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 7-1 for timing diagram

		MIN	NOM	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HIGH}	High period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time	0		3.45	µs
$t_{SU;DAT}$	Data setup time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Setup time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST-MODE					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0		0.9	µs
$t_{SU;DAT}$	Data setup time	100			ns
t_r	SDA and SCL rise time	20		300	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		300	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HIGH}	High period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time	0			µs
$t_{SU;DAT}$	Data setup time	50			ns
t_r	SDA and SCL Rise Time			120	ns
t_f	SDA and SCL Fall Time	20 × (IOVDD / 5.5 V)		120	ns
$t_{SU;STO}$	Setup time for STOP condition	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

7.7 Switching Characteristics: I^2C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 7-1 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDA)}$	SCL to SDA delay	Standard-mode	200		1250	ns
		Fast-mode	200		850	ns
		Fast-mode plus			400	ns

7.8 Timing Requirements: SPI Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-2 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(SCLK)}$	SCLK period		40			ns
$t_{H(SCLK)}$	SCLK high pulse duration		18			ns
$t_{L(SCLK)}$	SCLK low pulse duration		18			ns
t_{LEAD}	Enable lead time		16			ns
t_{TRAIL}	Enable trail time		16			ns
t_{DSEQ}	Sequential transfer delay		20			ns
$t_{SU(MOSI)}$	MOSI data setup time		8			ns
$t_{HLD(MOSI)}$	MOSI data hold time		8			ns
$t_{r(SCLK)}$	SCLK rise time	10% - 90% rise time			6	ns
$t_{f(SCLK)}$	SCLK fall time	90% - 10% fall time			6	ns

7.9 Switching Characteristics: SPI Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-2 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{a(MISO)}$	MISO access time	IOVDD = 1.8 V			18	ns
		IOVDD = 3.3 V			14	
$t_{d(MISO)}$	SCLK to MISO delay	50% of SCLK to 50% of MISO, IOVDD = 1.8 V			19	ns
		50% of SCLK to 50% of MISO, IOVDD = 3.3 V			15	
$t_{dis(MISO)}$	MISO disable time	IOVDD = 1.8 V			18	ns
		IOVDD = 3.3 V			14	

7.10 Timing Requirements: TDM, I^{2}S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-3 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

7.11 Switching Characteristics: TDM, I^{2}S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-3 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V			14	
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V			14	
$f_{(BCLK)}$	BCLK output clock frequency; master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{L(BCLK)}$	BCLK low pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{d(FSYNC)}$	BCLK to FSYNC delay; master mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V			14	
$t_{r(BCLK)}$	BCLK rise time; master mode	10% - 90% rise time, IOVDD = 1.8 V			10	ns
		10% - 90% rise time, IOVDD = 3.3 V			10	
$t_{f(BCLK)}$	BCLK fall time; master mode	90% - 10% fall time, IOVDD = 1.8 V			8	ns
		90% - 10% fall time, IOVDD = 3.3 V			8	

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

7.12 Timing Diagrams

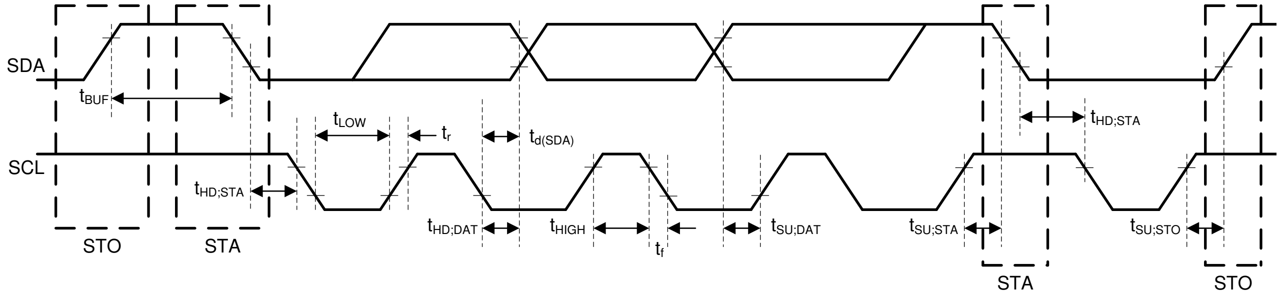


Figure 7-1. I²C Interface Timing Diagram

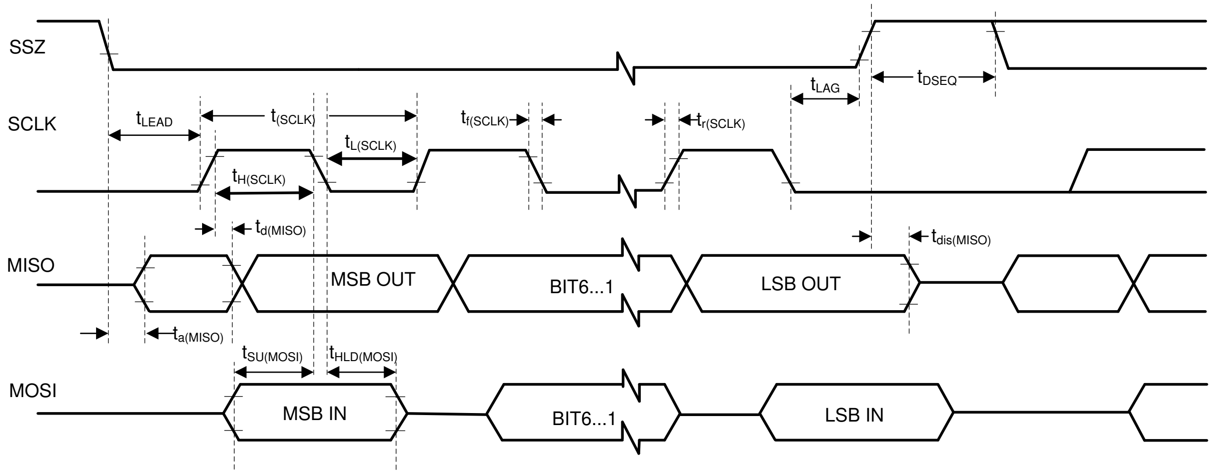


Figure 7-2. SPI Interface Timing Diagram

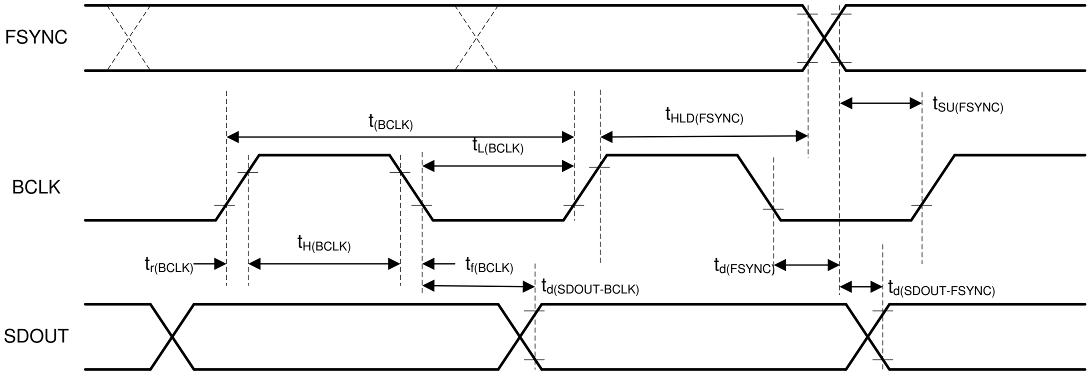
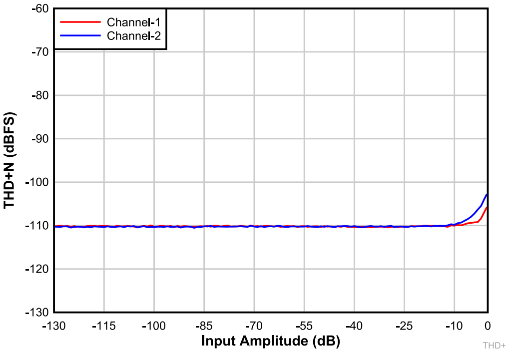


Figure 7-3. TDM, I²S, LJ Interface Timing Diagram

7.13 Typical Characteristics

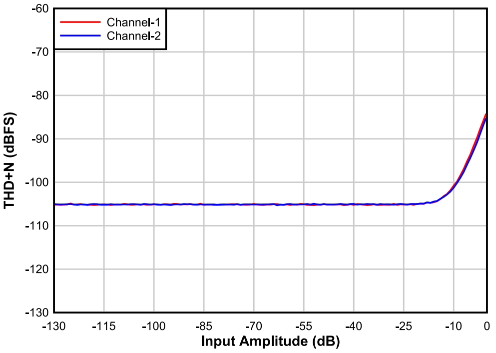
at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, channel gain = 0 dB, linear phase decimation filter, and MICBIAS programmed voltage = 8 V (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted)



Plot1_LINE_THDN_VS_AMPL.grf

AC-coupled differential line input

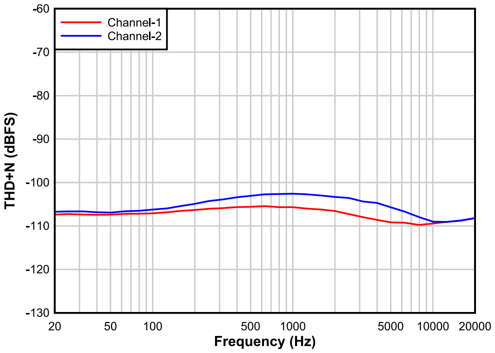
Figure 7-4. THD+N vs Input Amplitude



Plot2_LINE_SE_THDN_VS_AMPL.grf

AC-coupled single-ended line input

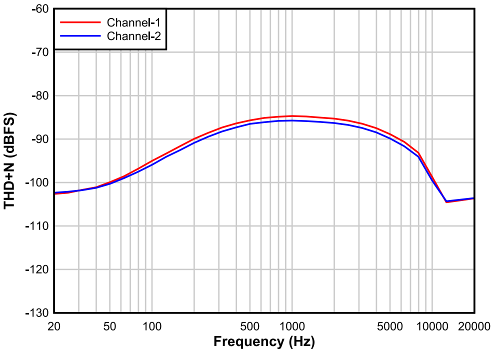
Figure 7-5. THD+N vs Input Amplitude



Plot3_LINE_THDN_VS_FREQ.grf

AC-coupled differential line input

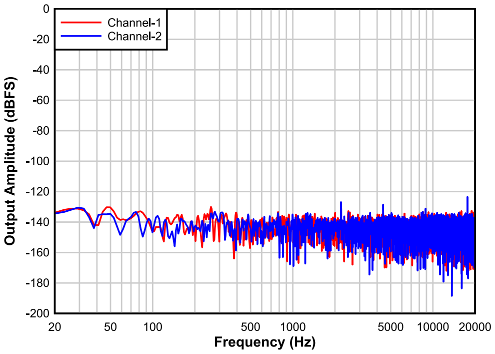
Figure 7-6. THD+N vs Input Frequency With a –1-dBr Input (non A-weighted)



Plot4_LINE_SE_THDN_VS_FREQ.grf

AC-coupled single-ended line input

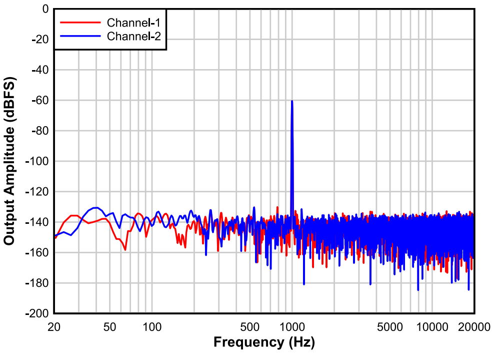
Figure 7-7. THD+N vs Input Frequency With a –1-dBr Input (non A-weighted)



Plot5_LINE_FFT_IDLE.grf

AC-coupled differential line input

Figure 7-8. FFT With Idle Input (non A-weighted)



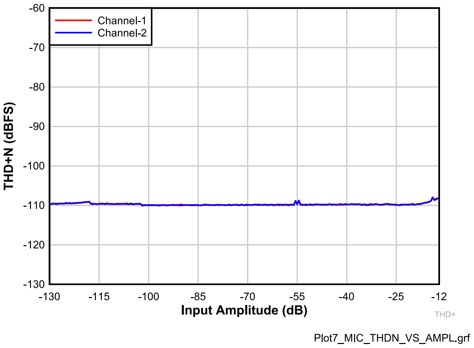
Plot6_LINE_FFT_m60dB.grf

AC-coupled differential line input

Figure 7-9. FFT With a –60-dBr Input (non A-weighted)

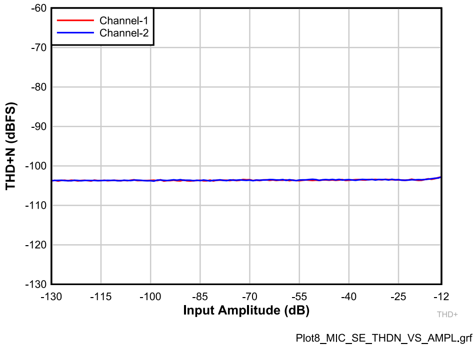
7.13 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, channel gain = 0 dB, linear phase decimation filter, and MICBIAS programmed voltage = 8 V (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted)



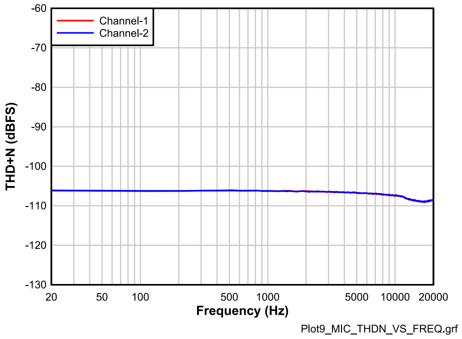
DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-10. THD+N vs Input Amplitude



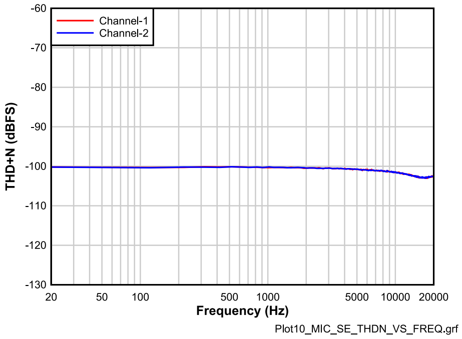
DC-coupled single-ended microphone input with DC common-mode 1NxP = 4 V and INxM = 0 V, high-swing mode enabled

Figure 7-11. THD+N vs Input Amplitude



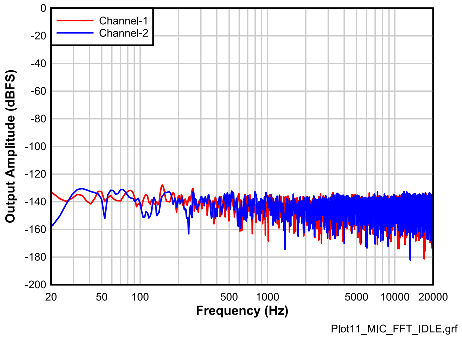
DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-12. THD+N vs Input Frequency With a –15-dBr Input (non A-weighted)



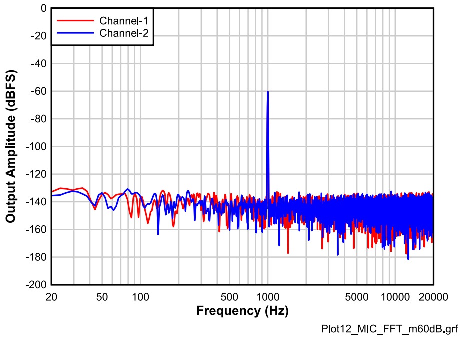
DC-coupled single-ended microphone input with DC common-mode 1NxP = 4 V and INxM = 0 V, high-swing mode enabled

Figure 7-13. THD+N vs Input Frequency With a –15-dBr Input (non A-weighted)



DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-14. FFT With Idle Input (non A-weighted)

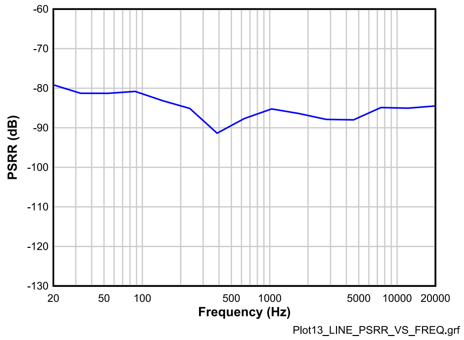


DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-15. FFT With a –60-dBr Input (non A-weighted)

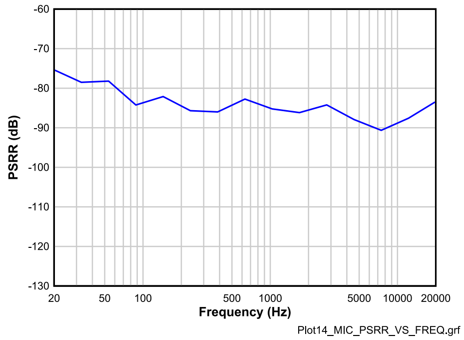
7.13 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, channel gain = 0 dB, linear phase decimation filter, and MICBIAS programmed voltage = 8 V (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted)



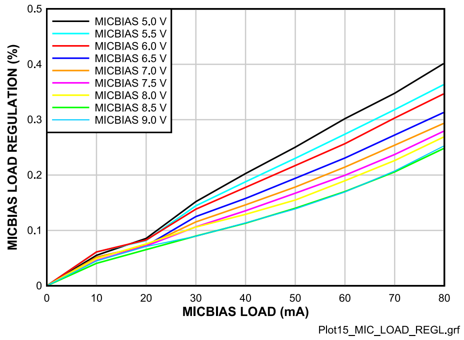
AC-coupled differential line input

Figure 7-16. Power-Supply Rejection Ratio vs Ripple Frequency With 1-V_{PP} Amplitude



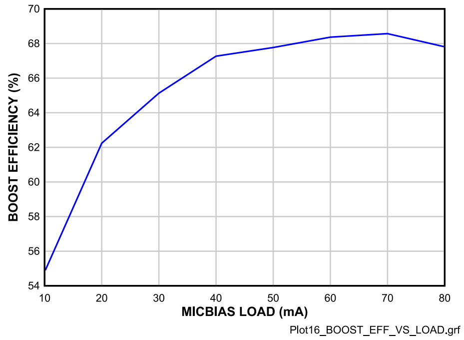
DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-17. Power-Supply Rejection Ratio vs Ripple Frequency With 1-V_{PP} Amplitude



DC-coupled differential microphone input

Figure 7-18. MICBIAS Load Regulation vs MICBIAS Load Current



DC-coupled differential microphone input with DC common-mode 1NxP = 6 V and INxM = 2 V, high-swing mode enabled

Figure 7-19. Boost Efficiency vs MICBIAS Load Current

8 Detailed Description

8.1 Overview

The PCM6020-Q1 is from a scalable PCM6xx0-Q1 family of devices. As with the extended family of devices, the PCM6020-Q1 consists of a high-performance, low-power, flexible, multichannel, audio analog-to-digital converter (ADC) with extensive feature integration. This device is intended for automotive applications such as vehicle cabin active noise cancellation, hands-free in-vehicle communication, emergency call, and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained automotive sub-system designs. Package, performance, and device-compatible configuration registers make this device well suited for scalable system designs.

The PCM6020-Q1 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADCs
- Configurable single-ended or differential audio inputs with high voltage signal swing
- High-voltage, low-noise programmable microphone bias output
- Highly flexible, comprehensive input fault diagnostic
- Automatic gain controller (AGC)
- Programmable decimation filters with linear-phase or low-latency filter
- Programmable channel gain, volume control, and biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF) and digital channel mixer
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the PCM6020-Q1 for configuring the control registers is supported using an I^2C or SPI interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I^2S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

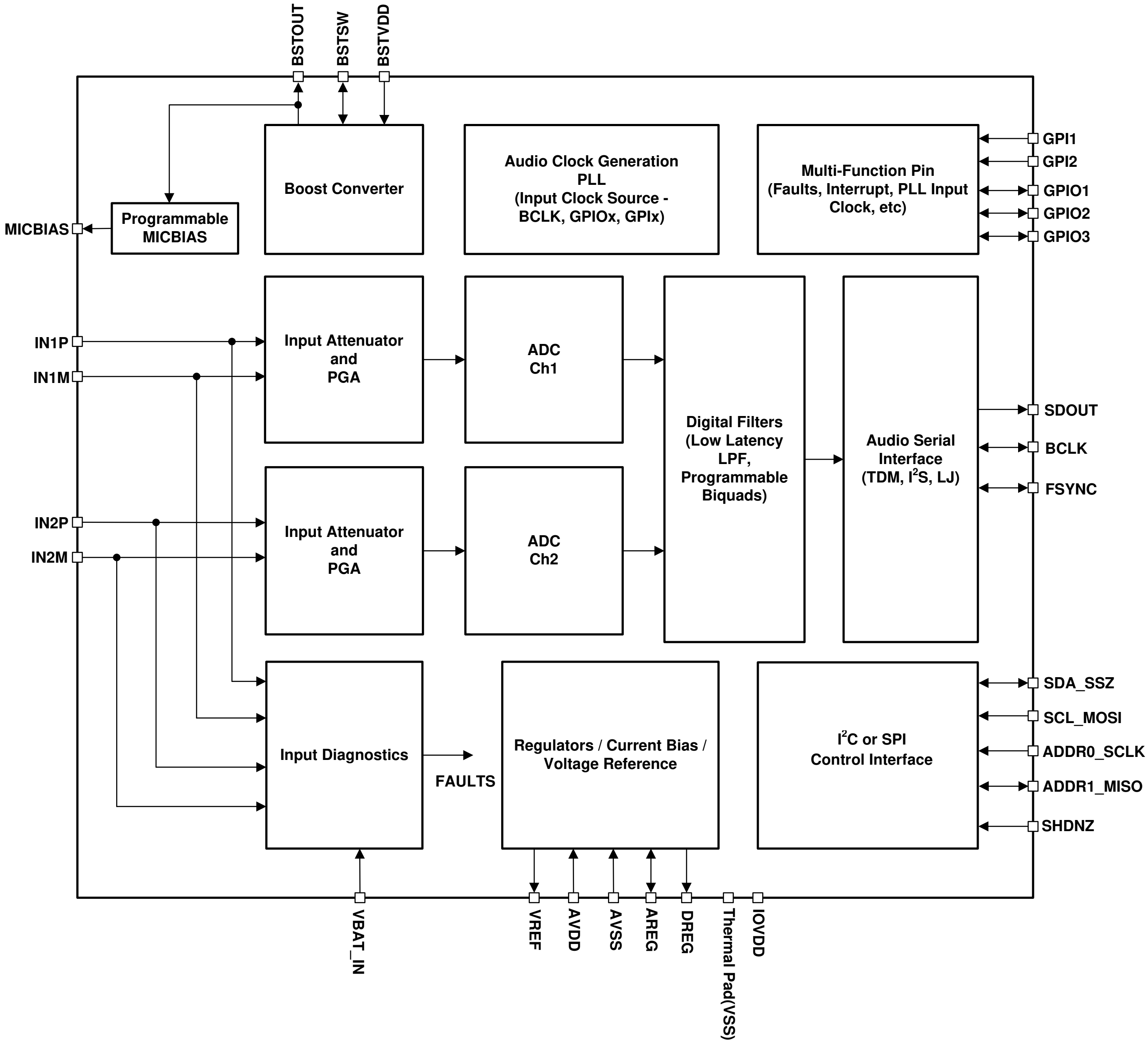
The device can support multiple devices by sharing the common I^2C and TDM buses across devices. Moreover, the device includes a daisy-chain feature and a secondary audio serial output data pin. These features relax the shared TDM bus timing requirements and board design complexities when operating multiple devices for applications requiring high audio data bandwidth.

lists the reference abbreviations used throughout this document to registers that control the device.

Table 8-1. Abbreviations for Register References

REFERENCE	ABBREVIATION	DESCRIPTION	EXAMPLE
Page y, register z, bit k	Py_Rz_Dk	Single data bit. The value of a single bit in a register.	Page 4, register 36, bit 0 = P4_R36_D0
Page y, register z, bits k-m	Py_Rz_D[k:m]	Range of data bits. A range of data bits (inclusive).	Page 4, register 36, bits 3, 2, 1, 0 = P4_R36_D[3:0]
Page y, register z	Py_Rz	One entire register. All eight bits in the register as a unit.	Page 4, register 36 = P4_R36
Page y, registers z-n	Py_Rz-Rn	Range of registers. A range of registers in the same page.	Page 4, registers 36, 37, 38 = P4_R36-R38

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

8.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All these registers can be accessed using either I^2C or SPI communication to the device. For more information, see the *Programming* section.

8.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCM6020-Q1 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^2S or left-justified protocols format, programmable data length options, very flexible master-slave configurability for bus clock lines, and the ability to communicate with multiple devices within a system directly.

The bus protocol TDM, I^2S, or left-justified (LJ) format can be selected by using the ASI_FORMAT[1:0], P0_R7_D[7:6] register bits. As shown in Table 8-2 and Table 8-3, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the ASI_WLEN[1:0], P0_R7_D[5:4] register bits.

Table 8-2. Audio Serial Interface Format

P0_R7_D[7:6] : ASI_FORMAT[1:0]	AUDIO SERIAL INTERFACE FORMAT
00 (default)	Time division multiplexing (TDM) mode
01	Inter IC sound (I^2S) mode
10	Left-justified (LJ) mode
11	Reserved (do not use this setting)

Table 8-3. Audio Output Channel Data Word-Length

P0_R7_D[5:4] : ASI_WLEN[1:0]	AUDIO OUTPUT CHANNEL DATA WORD-LENGTH
00	Output channel data word-length set to 16 bits
01	Output channel data word-length set to 20 bits
10	Output channel data word-length set to 24 bits
11 (default)	Output channel data word-length set to 32 bits

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 64) to allow all output channel audio data transmissions to complete on the audio bus by a device or multiple PCM6020-Q1 devices sharing the same audio bus. The device supports up to two output channels that can be configured to place their audio data on bus slot 0 to slot 63. Table 8-4 lists the output channel slot configuration settings. In I^{2}S and LJ mode, the slots are divided into two sets, left-channel slots and right-channel slots, as described in the *Inter IC Sound (I^{2}S) Interface* and *Left-Justified (LJ) Interface* sections.

Table 8-4. Output Channel Slot Assignment Settings

P0_R11_D[5:0] : CH1_SLOT[5:0]	OUTPUT CHANNEL 1 SLOT ASSIGNMENT
00 0000 = 0d (default)	Slot 0 for TDM or left slot 0 for I^{2}S, LJ.
00 0001 = 1d	Slot 1 for TDM or left slot 1 for I^{2}S, LJ.
…	…
01 1111 = 31d	Slot 31 for TDM or left slot 31 for I^{2}S, LJ.
10 0000 = 32d	Slot 32 for TDM or right slot 0 for I^{2}S, LJ.
…	…
11 1110 = 62d	Slot 62 for TDM or right slot 30 for I^{2}S, LJ.
11 1111 = 63d	Slot 63 for TDM or right slot 31 for I^{2}S, LJ.

Similarly, the slot assignment setting for output channel 2 can be done using the CH2_SLOT (P0_R12) register.

The slot word length is the same as the output channel data word length set for the device. The output channel data word length must be set to the same value for all PCM6020-Q1 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

The device also includes a feature that offsets the start of the slot data transfer with respect to the frame sync by up to 31 cycles of the bit clock. Table 8-5 lists the programmable offset configuration settings.

Table 8-5. Programmable Offset Settings for the ASI Slot Start

P0_R8_D[4:0] : TX_OFFSET[4:0]	PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START
0 0000 = 0d (default)	The device follows the standard protocol timing without any offset.
0 0001 = 1d	Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I^{2}S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing.
......	......
1 1110 = 30d	Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I^{2}S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.
1 1111 = 31d	Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I^{2}S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the FSYNC_POL, P0_R7_D3 register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the BCLK_POL, P0_R7_D2 register bit.

8.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 8-1 to Figure 8-4 illustrate the protocol timing for TDM operation with various configurations.

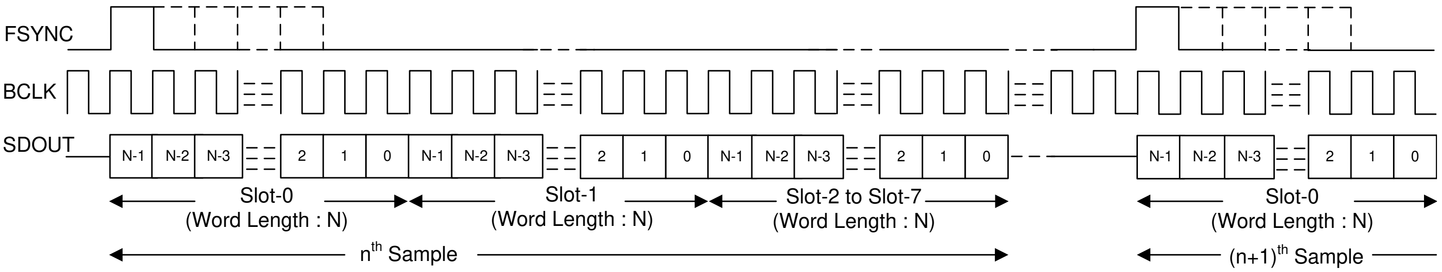


Figure 8-1. TDM Mode Standard Protocol Timing (TX_OFFSET = 0)

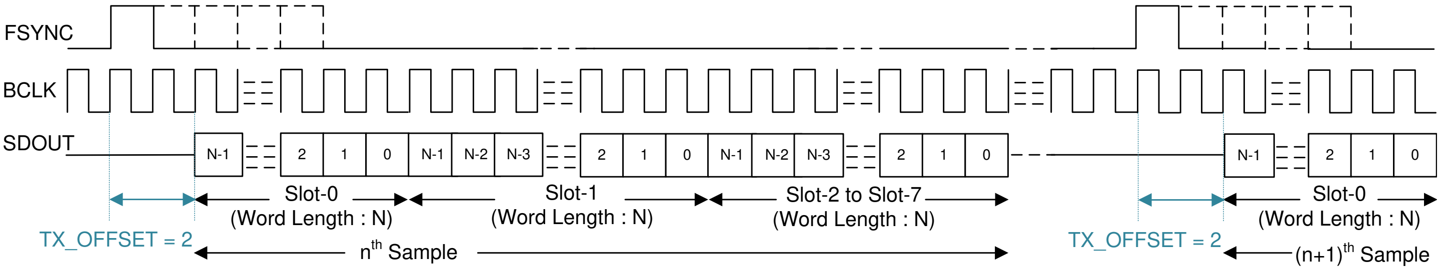


Figure 8-2. TDM Mode Protocol Timing (TX_OFFSET = 2)

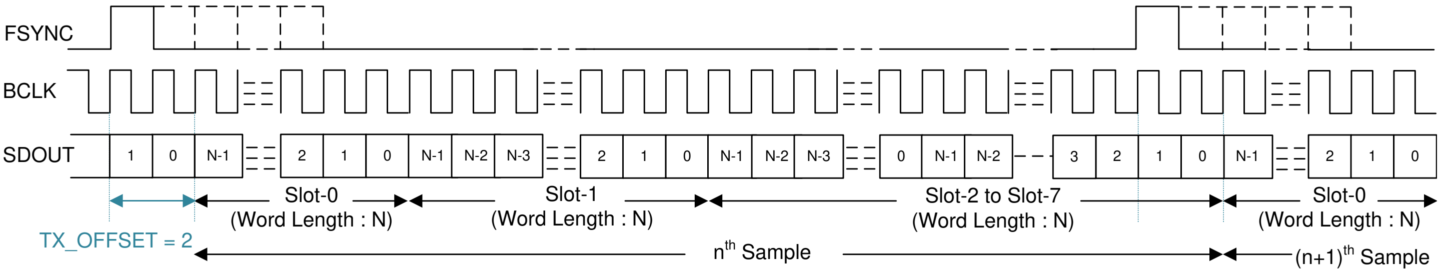


Figure 8-3. TDM Mode Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 2)

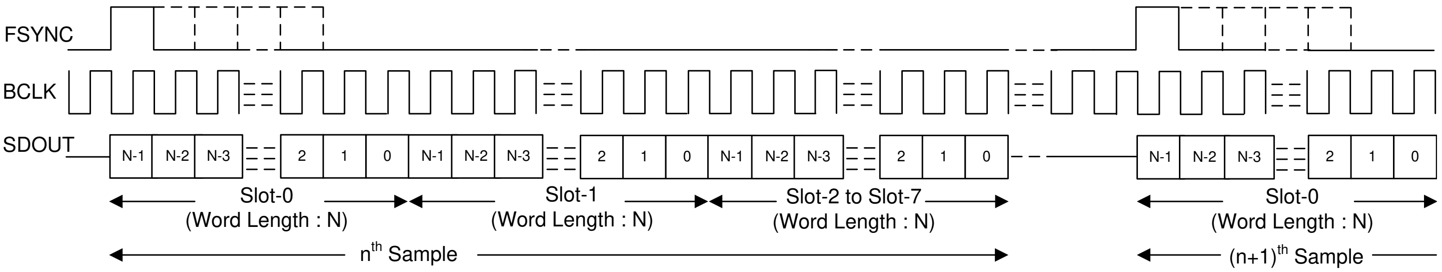


Figure 8-4. TDM Mode Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a TX_OFFSET value higher than 0 is recommended.

8.3.1.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. Figure 8-5 to Figure 8-8 show the protocol timing for I^{2}S operation with various configurations.

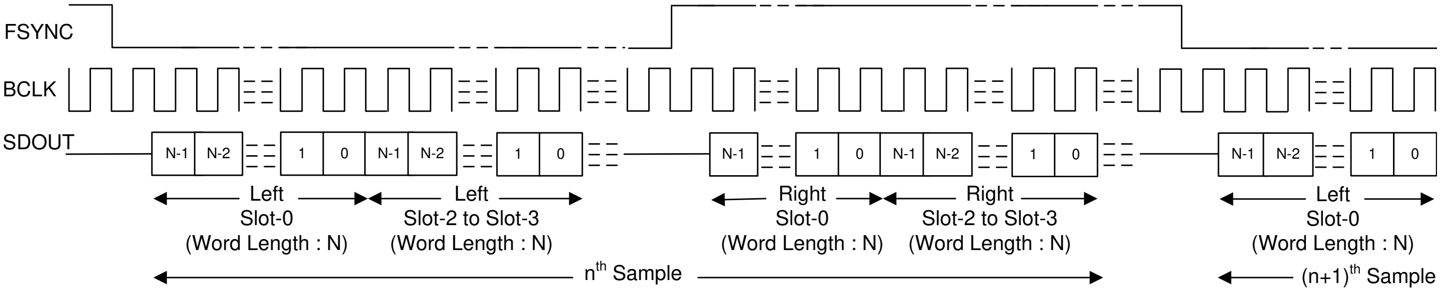


Figure 8-5. I^{2}S Mode Standard Protocol Timing (TX_OFFSET = 0)

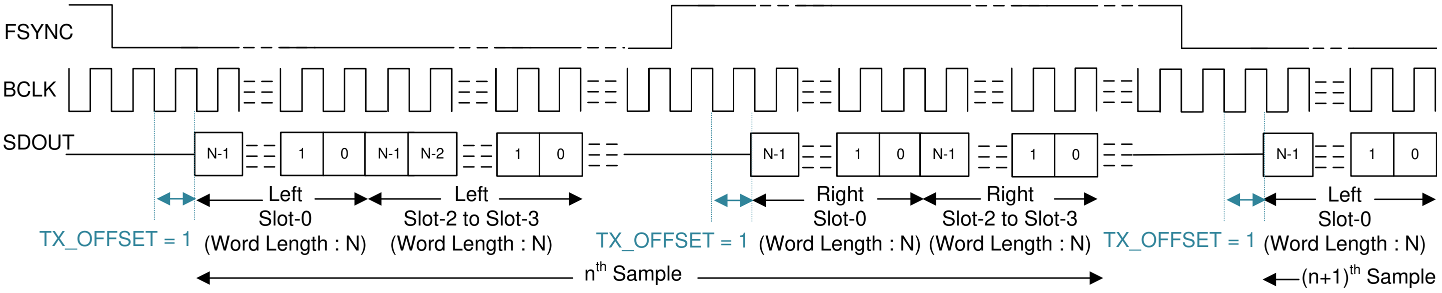


Figure 8-6. I^{2}S Protocol Timing (TX_OFFSET = 1)

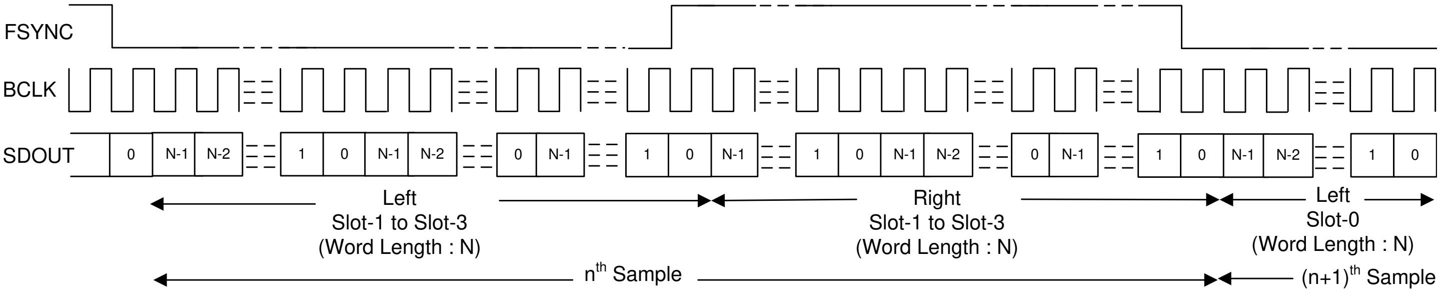


Figure 8-7. I^{2}S Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

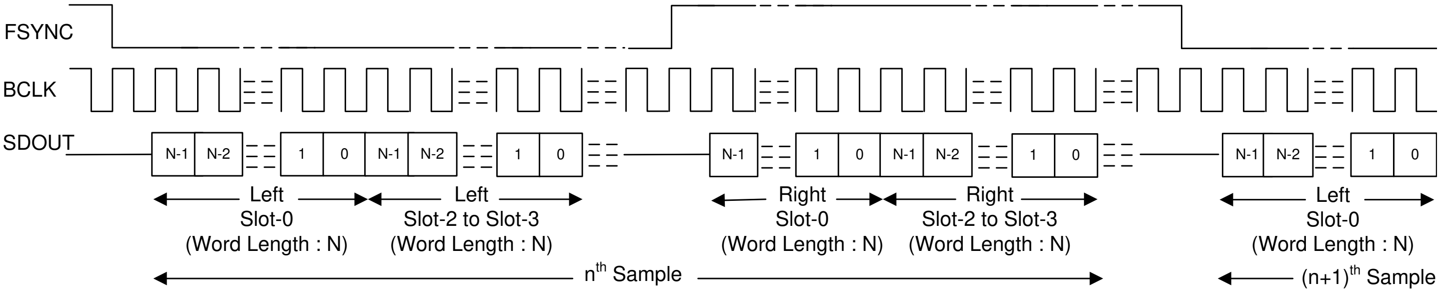


Figure 8-8. I^{2}S Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in I^{2}S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

8.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. Figure 8-9 to Figure 8-12 illustrate the protocol timing for LJ operation with various configurations.

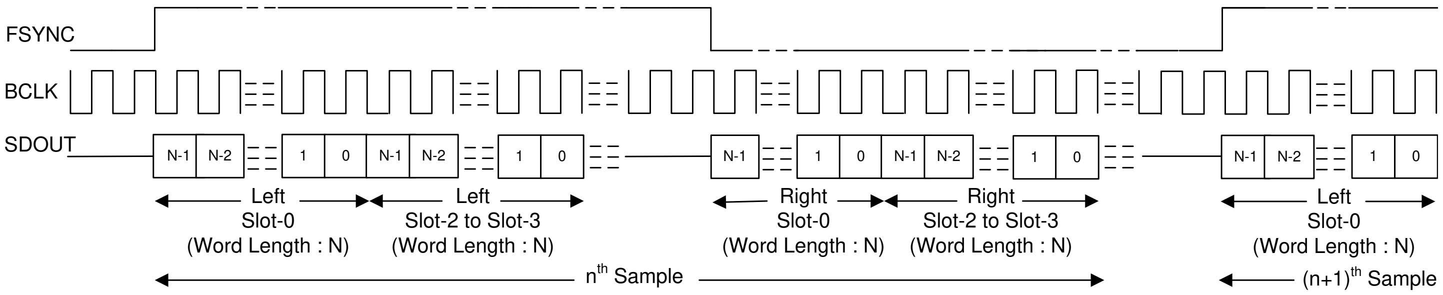


Figure 8-9. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)

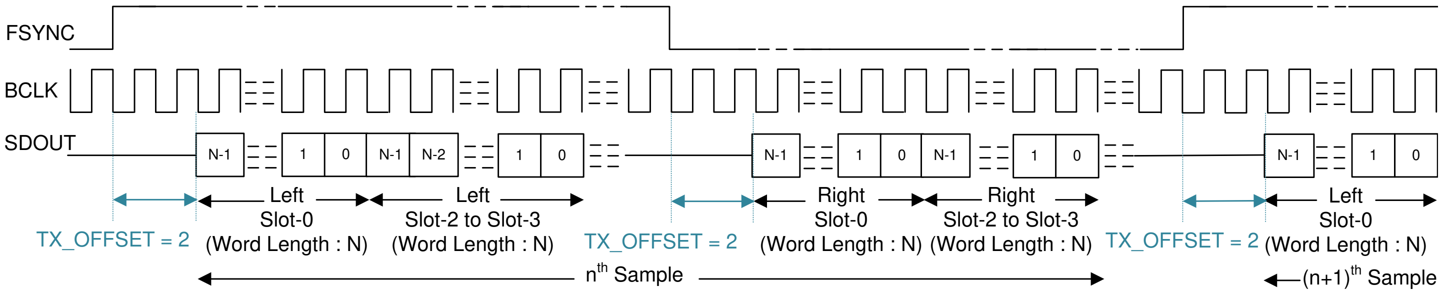


Figure 8-10. LJ Protocol Timing (TX_OFFSET = 2)

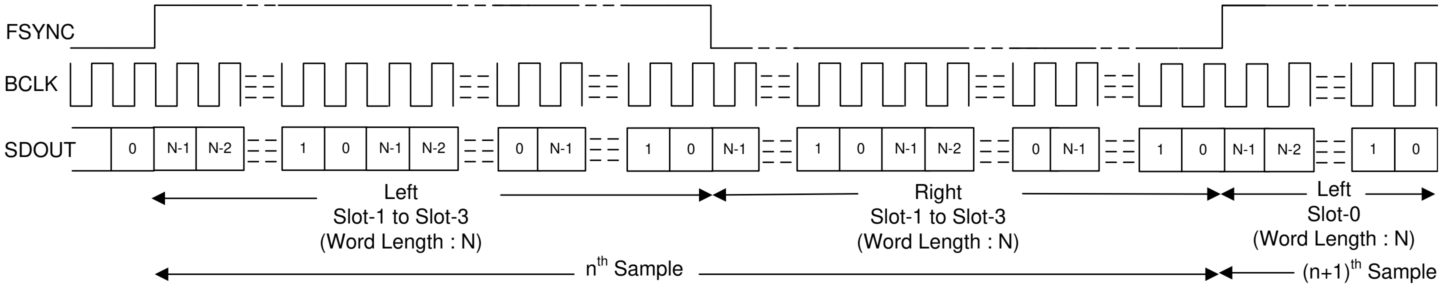


Figure 8-11. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

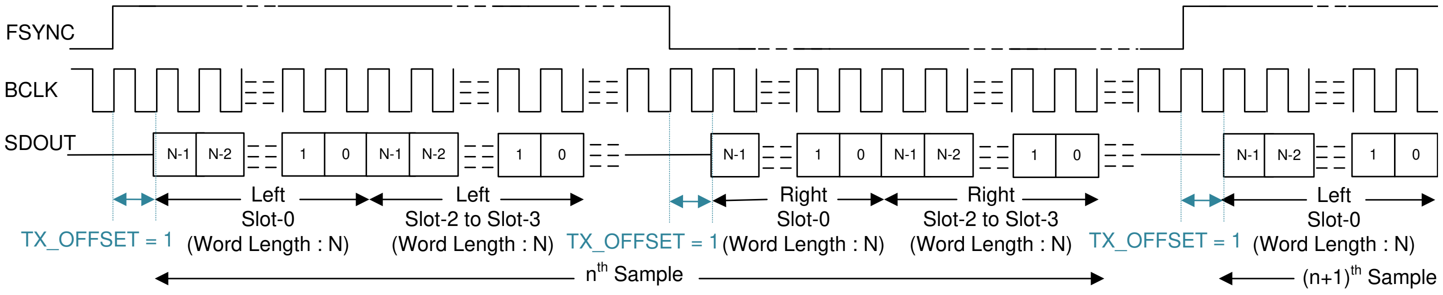


Figure 8-12. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

8.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect multiple PCM6xx0-Q1 devices by sharing a single common I^2C control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone array for beam-forming operation, hands-free in-vehicle communication, car cabin active noise cancellation, and so forth. Figure 8-13 shows a diagram of multiple PCM6020-Q1 devices in a configuration where the control and audio data buses are shared.

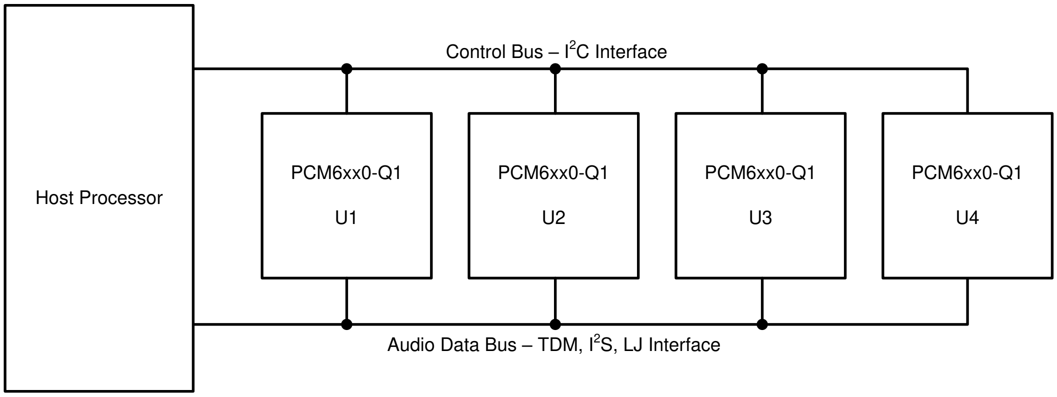


Figure 8-13. Multiple PCM6020-Q1 Devices With Shared Control and Audio Data Buses

The PCM6020-Q1 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- Supports up to four pin-programmable I^2C slave addresses
- I^2C broadcast simultaneously writes to (or triggers) all PCM6020-Q1 devices
- Supports up to 64 configuration output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIOx pin can be configured as a secondary output data lane for the audio serial interface
- The GPIOx or GPIx pin can be used in a daisy-chain configuration of multiple PCM6xx0-Q1 devices
- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable master and slave options for the audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices

See the *Multiple PCM6xx0-Q1 Devices With Shared TDM and I^2C Bus* application report for further details.

8.3.2 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the ADC modulator and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio bus.

The device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 8-6 and Table 8-7 list the supported FSYNC and BCLK frequencies.

Table 8-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)	FSYNC (384 kHz)	FSYNC (768 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072	6.144	12.288
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608	9.216	18.432
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144	12.288	24.576
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216	18.432	**Reserved**
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288	24.576	**Reserved**
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432	**Reserved**	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576	**Reserved**	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	8.192	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	16.384	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

Table 8-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224	5.6448	11.2896
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336	8.4672	16.9344
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448	11.2896	22.5792
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672	16.9344	**Reserved**
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896	22.5792	**Reserved**
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344	**Reserved**	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792	**Reserved**	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	7.5264	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	15.0528	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

The status register ASI_STS, P0_R21, captures the device auto detect result for the FSYNC frequency and the BCLK to FSYNC ratio. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes the record channels accordingly.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks. The device also supports an option to use the BCLK, GPIOx, or the GPIx pin (as MCLK) as the audio clock source without using the PLL to reduce power consumption. However, the ADC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications.

The device also supports an audio bus master mode operation using the GPIOx or GPIx pin (as MCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on master mode configuration and operation are discussed in the *Configuring and Operating TLV320ADCx140 as Audio Bus Master* application report.

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the ASI_ERR, P0_R9_D5 and AUTO_CLK_CFG, P0_R19_D6, register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the *PCM6xx0Q1EVM-PDK Evaluation Module* user's guide and the *PurePath™ Console Graphical Development Suite for Audio System Design and Development* development suite.

8.3.3 Input Channel Configuration

The PCM6020-Q1 consists of two pairs of analog input pins (INxP and INxM) that can be configured as either differential or single-ended inputs for the recording channel. The device supports simultaneous recording of up to two channels using the multichannel ADC. The input source for the analog pins can be either analog microphones or line, aux inputs from the system board. Table 8-8 describes how to set the input configuration for the record channel.

Table 8-8. Input Source Selection for the Record Channel

P0_R60_D[6:5] : CH1_INSRC[1:0]	INPUT CHANNEL 1 RECORD SOURCE SELECTION
00 (default)	Analog differential input for channel 1
01	Analog single-ended input for channel 1
10 or 11	Reserved (do not use this setting)

Similarly, the input source selection setting for input channel 2 can be configured using the CH2_INSRC[1:0] (P0_R65_D[6:5]) register bits.

The device supports the input DC fault diagnostic feature for microphone recording with the DC-coupled inputs configuration; however, the device also supports an option for AC-coupled inputs if the DC diagnostic is not required for the specific input pins. This configuration can be done independently for each channel by setting the CH1_DC (P0_R60_D4) and CH2_DC (P0_R65_D4) register bits.

For the DC-coupled line input configuration, the DC common-mode difference (INxP – INxM) for the analog input pins must be 0 V to support the 10-V_{RMS} full-scale differential input. For the DC-coupled microphone input configuration, the DC common-mode difference (INxP – INxM) for the analog input pins must be within 3.4 V to 5.0 V to support the 2-V_{RMS} full-scale differential input in the default mode of operation. Alternatively, the device has a mode to support more than a 2-V_{RMS} differential DC-coupled microphone signal by setting the CH1_MIC_IN_RANGE, P0_R60_D3, register bit for channel 1 and, similarly, the CH2_MIC_IN_RANGE, P0_R65_D3 register bit for channels 2. If the CH1_MIC_IN_RANGE bit is set high (the recommended setting to support a higher DC common-mode difference and a higher AC signal swing), then the device supports the maximum differential input voltage IN1P–IN1M as high as 8.4 V (for the MICBIAS 9-V setting), including the AC signal and DC differential common-mode voltage. The DC differential common-mode voltage is later filtered out by the digital high-pass filter and the digital output full-scale corresponds to the 10-V_{RMS} AC signal in this case.

Figure 8-14 and Figure 8-15 show how to connect a DC-coupled microphone for a differential and single-ended input, respectively. The value of the external bias resistor, R1, must be appropriately chosen based upon the microphone impedance. For a differential input, the value of the external bias resistor is recommended to be used for half of the microphone impedance, whereas for a single-ended input, the external bias resistor is recommended to be the same as the microphone impedance.

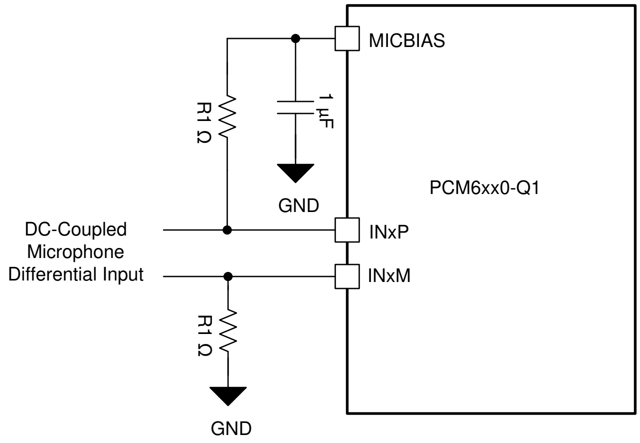


Figure 8-14. DC-Coupled Microphone Differential Input Connection

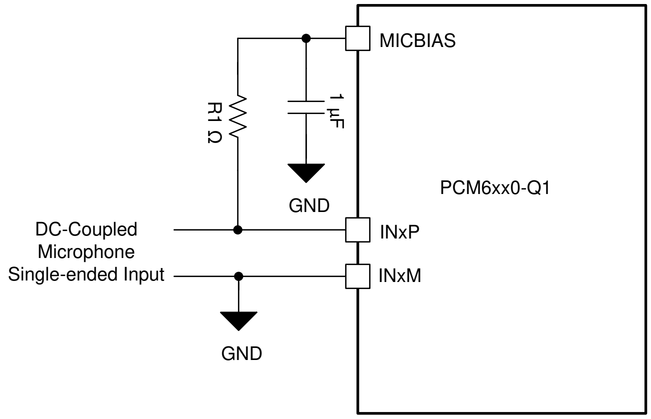


Figure 8-15. DC-Coupled Microphone Single-Ended Input Connection

In AC-coupled mode, the value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage. For single-ended input configuration, the INxM pin must be grounded after the AC coupling capacitor in AC-coupled mode.

Figure 8-16 and Figure 8-17 show how to connect an AC-coupled microphone or line source for a differential and single-ended input, respectively. In AC-coupled mode, the device input pins INxP and INxM, must be biased appropriately for the DC common-mode value either using the on-chip MICBIAS output voltage along with external bias resistor, R0, or using an external bias generator circuit. The maximum value for resistor R0 depends upon the signal swing and the MICBIAS value programmed. See the *PCM6xx0-Q1 AC Coupled External Resistor Calculator* to calculate the R0 value for the desired system configuration.

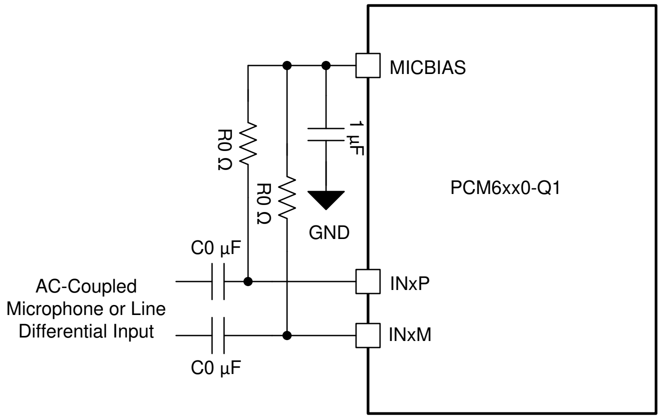


Figure 8-16. AC-Coupled Microphone or Line Differential Input Connection

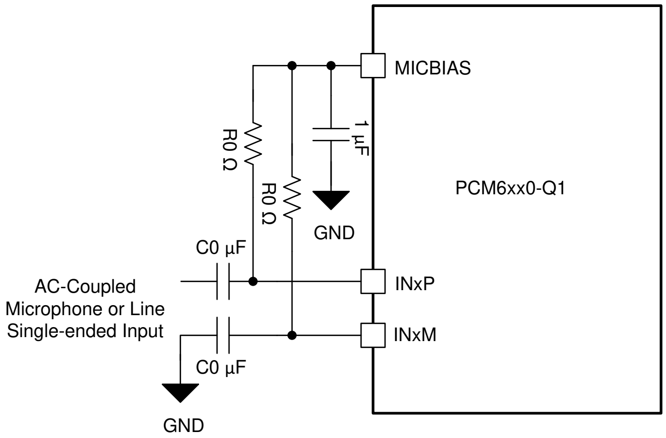


Figure 8-17. AC-Coupled Microphone or Line Single-Ended Input Connection

8.3.4 Reference Voltage

All audio data converters require a DC reference voltage. The PCM6020-Q1 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with good PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to the analog ground (AVSS).

To achieve low power consumption, this audio reference block is powered down in sleep mode or software shutdown; see the *Sleep Mode or Software Shutdown* section for more details. When exiting sleep mode, the audio reference block is powered up using internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1-µF decoupling capacitor. If a higher value of the decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG, P0_R2_D[4:3] register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

8.3.5 Microphone Bias

The device integrates a built-in, low-noise, programmable, high-voltage, microphone bias pin (MICBIAS) that can be used in the system for biasing the analog microphone. The integrated bias amplifier supports up to 80 mA of load current, which can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine tuned for specific microphone combinations. The PCM6020-Q1 has an integrated efficient boost converter to generate the high voltage supply for the programmable microphone bias using an external, low-voltage, 3.3-V BSTVDD supply.

When using the MICBIAS pin for biasing multiple microphones, TI recommends avoiding common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. Table 8-9 shows the available microphone bias programmable options.

Table 8-9. MICBIAS Programmable Settings

P0_R59_D[7:4] : MBIAS_VAL[3:0]	MICBIAS OUTPUT VOLTAGE
0000 to 0110	Reserved (do not use these settings)
0111	Set to 5.0 V
1000	Set to 5.5 V
1001	Set to 6.0 V
1010	Set to 6.5 V
1011	Set to 7.0 V
1100	Set to 7.5 V
1101	Set to 8.0 V
1110	Set to 8.5 V
1111	Set to 9.0 V

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ, P0_R117_D7 register bit. Additionally, the device provides an option to configure the GPIOx pins to directly control the microphone bias output power on or power off. This feature is useful in some systems to control the microphone directly without engaging the host for I^{2}C or SPI communication. The MICBIAS_PDZ, P0_R117_D7 register bit value is ignored if the GPIOx pins are configured to control the microphone bias power on or power off.

8.3.6 Input DC Fault Diagnostics

Each input of the PCM6020-Q1 features highly comprehensive DC fault diagnostics that can be configured to detect fault conditions in the DC-coupled input configuration and trigger an interrupt request to a host processor. Diagnostics are enabled for each channel by configuring DIAG_CFG0, P0_R100. For channels with diagnostics enabled, the input pins are scanned automatically by an integrated SAR ADC with a programmable repetition rate. The repetition rate can be configured using the REP_RATE, P0_R103_D7-6 register bits. For fastest fault response time and also to get better signal integrity and signal chain performance for the record channel, REP_RATE must be configured to 0 (non-default setting). The diagnostic processor averages eight consecutive samples per test to improve noise performance. The DC fault diagnostics is not supported in the AC-coupled input configuration.

The device features various programmable threshold registers, P0_R101 to P0_R102, which can by configured by the host processor to define the fault region for a different category of fault condition detection. Additionally, there is also a debounce feature, configured with FAULT_DBNCE_SEL, P0_R103_D3-2. This feature sets the number of consecutive scan counts where the fault condition occurs before the latched status register is tripped, thus reducing false triggers by transient events. The device also has a moving average feature, P0_R104, which continuously averages out the newly measured data with old measured data and thus reduces the false triggers by any short-duration transient events.

8.3.6.1 Fault Conditions

8.3.6.1.1 Input Pin Short to Ground

A short to ground fault occurs when the voltage of the input pin is measured below the threshold voltage with respect to ground (AVSS). The threshold can be set by configuring DIAG_SHT_GND, P0_R102_D7-4.

8.3.6.1.2 Input Pin Short to MICBIAS

A short to MICBIAS fault occurs when the difference between the voltage measured for the MICBIAS pin and the input pin (MICBIAS – INxx) is less than the threshold. The threshold can be set by configuring DIAG_SHT_MICBIAS, P0_R102_D3-0.

8.3.6.1.3 Open Inputs

In the event that a microphone becomes disconnected from the inputs, the microphone bias resistors pull INxP to MICBIAS and INxM to ground. The combination of INxP shorted to MICBIAS and INxM shorted to ground for the same channel in a diagnostic sweep results in an open input fault condition.

8.3.6.1.4 Short Between INxP and INxM

An input terminal shorted fault occurs when the difference between the voltage measured for the input pin INxP and the input pin INxM of the same channel is less than the threshold. The threshold can be set by configuring DIAG_SHT_TERM, P0_R101_D7-4.

8.3.6.1.5 Input Pin Overvoltage

An input terminal overvoltage fault occurs when the voltage measured for the input pin is above the voltage measured for the MICBIAS pin.

8.3.6.1.6 Input Pin Short to VBAT_IN

A short to VBAT_IN fault occurs when the difference between the voltage measured for the VBAT_IN pin and the input pin, ABS(VBAT_IN – INxx), is less than the threshold or both the VBAT_IN and INxx pin measured voltages are above 11.7 V. The threshold can be set by configuring DIAG_SHT_VBAT_IN, P0_R101_D3-0.

When VBAT_IN is less than MICBIAS, false fault detections can exist based on the signal level of the INxx pin. To minimize false detections there is also a separate debounce count for this condition set by configuring VSHORT_DBNCE, P0_R106_D1.

8.3.6.2 Fault Reporting

Faults are reported in live and latched status registers. The live registers, P1_R45 to P1_R55, are updated continuously with each new scan and report the most recent measurements reported by the diagnostics processor. The latched status of each diagnostic fault is reported by the channel in P0_R46 to P0_R55, and a latched summary by the channel is reported in CHx_LTCH, P0_R45. If the LTCH_CLR_ON_READ, P0_R40_D0, bit is set to '0', then the latched registers clear upon reading, and are latched if the associated bit in the live fault registers transitions from a ‘0’ to a ‘1’. A transition of any bit in the latched register from a ‘0’ to ‘1’ triggers an interrupt request.

For detecting a persistent fault, an additional mode is available for the latched registers. In this mode, the latched registers are only cleared upon reading if the status bit in the associated live status register is ‘0’ at the time of reading. This mode is enabled (default setting) by configuring LTCH_CLR_ON_READ, P0_R40_D0 to a ‘1’.

8.3.6.2.1 Overcurrent and Overtemperature Protection

The device has an overcurrent protection circuit that limits the current drawn out of the MICBIAS output to the maximum supported level when an external undesired short event occurs on the MICBIAS pin. The device sets the status flag, P0_R44_D4 bit, on an overcurrent detection. Additionally, the device has an overtemperature detection circuit that is enabled by default and sets the status flag, P0_R44_D5 bit, whenever the die junction temperature goes higher than the supported level.

Additionally, the P0_R58 and P0_R40_D4:3 register can be configured to shutdown MICBIAS along with the on-chip boost on an overtemperature detection. TI recommends configuring PD_ON_FLT_CFG, P0_R40_D4-3 to '10' so that on an overtemperature detection, the device powers-down MICBIAS, the on-chip boost, and all ADC channels.

More details and information on fault diagnostics are discussed in the *PCM6xx0-Q1 Fault Diagnostics, Interrupts, and Protection Features* application report.

8.3.7 Signal-Chain Processing

The PCM6020-Q1 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the PCM6020-Q1 optimized for a variety of end-equipment and applications that require multichannel audio capture. Figure 8-18 shows a conceptual block diagram that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.

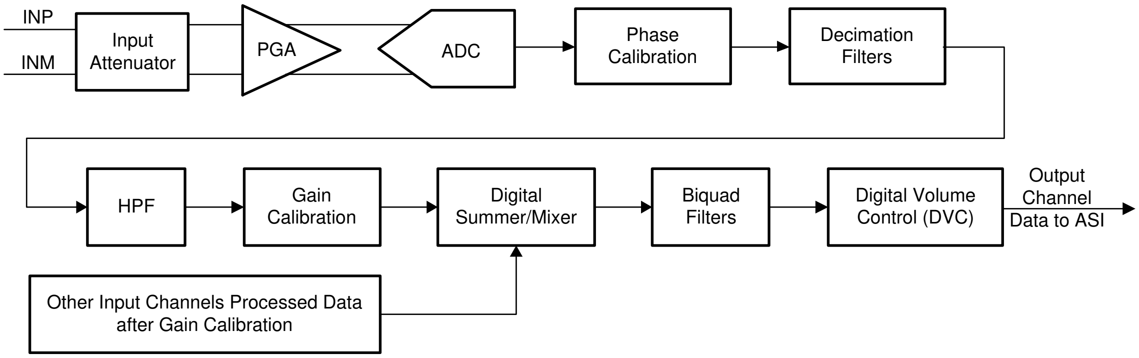


Figure 8-18. Signal-Chain Processing Flowchart

The front-end input attenuator allows the device to accept the high-voltage input signal that is attenuated by the input attenuator circuit before being routed to a low-noise programmable gain amplifier (PGA). Along with a low-noise and low-distortion, multibit, delta-sigma ADC, the front-end PGA enables the PCM6020-Q1 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device also has an integrated programmable biquad filter that allows for custom low-pass, high-pass, or any other desired frequency shaping. Thus, the overall signal chain architecture removes the requirement to add external components for antialiasing low-pass filtering, and thus saves drastically on the external system component cost and board space. See the *PCM6xx0-Q1 Integrated Analog Antialiasing Filter and Flexible Digital Filter* application report for further details.

The signal chain also consists of various highly programmable digital processing blocks, such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, and volume control. The details on these processing blocks are discussed further in this section.

The desired input channels for recording can be enabled or disabled by using the IN_CH_EN (P0_R115) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI_OUT_EN (P0_R116) register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel recording is on, then that use case is supported by setting the DYN_CH_PUPD_EN, P0_R117_D4 register bit to 1'b1 but do not power-down channel 1 in this mode of operation.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

For output sample rates of 192 kHz or lower, the device supports all features for 2-channel recording and various programmable processing blocks. However, for output sample rates higher than 192 kHz, there are limitations in the number of simultaneous channel recordings supported and the number of biquad filters and such. See the *PCM6xx0-Q1 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

8.3.7.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each input channel that can be set to the appropriate value based on the maximum input signal expected in the system and the ADC VREF setting used (see the *Reference Voltage* section), which determines the ADC full-scale signal level.

Configure the desired channel gain setting before powering up the ADC channel and do not change this setting while the ADC is powered on. The programmable range supported for each channel gain is from 0 dB to 42 dB in steps of 1 dB. To achieve low-noise performance, the device internal logic first maximizes the gain for the front-end low-noise analog PGA, and then applies any residual programmed channel gain in the digital processing block.

Table 8-10 shows the programmable options available for the channel gain.

Table 8-10. Channel Gain Programmable Settings

P0_R61_D[7:2] : CH1_GAIN[5:0]	CHANNEL GAIN SETTING FOR INPUT CHANNEL 1
00 0000 = 0d (default)	Input channel 1 gain is set to 0 dB
00 0001 = 1d	Input channel 1 gain is set to 1 dB
00 0010 = 2d	Input channel 1 gain is set to 2 dB
…	…
10 1001 = 41d	Input channel 1 gain is set to 41 dB
10 1010 = 42d	Input channel 1 gain is set to 42 dB
10 1011 to 11 1111 = 43d to 63d	Reserved (do not use these settings)

Similarly, the channel gain setting for input channel 2 can be configured using the CH2_GAIN (P0_R66) register bits.

The device also has a programmable digital volume control with a range from –100 dB to 27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the ADC channel is powered-up and recording. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang-up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the DVOL_GANG (P0_R108_D7) register bit.

Table 8-11 shows the programmable options available for the digital volume control.

Table 8-11. Digital Volume Control (DVC) Programmable Settings

P0_R62_D[7:0] : CH1_DVOL[7:0]	DVC SETTING FOR OUTPUT CHANNEL 1
0000 0000 = 0d	Output channel 1 DVC is set to mute
0000 0001 = 1d	Output channel 1 DVC is set to –100 dB
0000 0010 = 2d	Output channel 1 DVC is set to –99.5 dB
0000 0011 = 3d	Output channel 1 DVC is set to –99 dB
…	…
1100 1000 = 200d	Output channel 1 DVC is set to –0.5 dB
1100 1001 = 201d (default)	Output channel 1 DVC is set to 0 dB
1100 1010 = 202d	Output channel 1 DVC is set to 0.5 dB
…	…
1111 1101 = 253d	Output channel 1 DVC is set to 26 dB
1111 1110 = 254d	Output channel 1 DVC is set to 26.5 dB
1111 1111 = 255d	Output channel 1 DVC is set to 27 dB

Similarly, the digital volume control setting for output channel 2 can be configured using the CH2_DVOL (P0_R67) register bits.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

8.3.7.2 Programmable Channel Gain Calibration

Along with the programmable channel gain and digital volume, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. Table 8-12 shows the programmable options available for the channel gain calibration.

Table 8-12. Channel Gain Calibration Programmable Settings

P0_R63_D[7:4] : CH1_GCAL[3:0]	CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 = 0d	Input channel 1 gain calibration is set to –0.8 dB
0001 = 1d	Input channel 1 gain calibration is set to –0.7 dB
…	…
1000 = 8d (default)	Input channel 1 gain calibration is set to 0 dB
…	…
1110 = 14d	Input channel 1 gain calibration is set to 0.6 dB
1111 = 15d	Input channel 1 gain calibration is set to 0.7 dB

Similarly, the channel gain calibration setting for input channel 2 can be configured using the CH2_GCAL (P0_R68) register bits.

8.3.7.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error. The modulator clock, the same clock used for ADC_MOD_CLK, is 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz). This feature is very useful for many applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. Table 8-13 shows the available programmable options for channel phase calibration.

Table 8-13. Channel Phase Calibration Programmable Settings

P0_R64_D[7:0] : CH1_PCAL[7:0]	CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 0000 = 0d (default)	Input channel 1 phase calibration with no delay
0000 0001 = 1d	Input channel 1 phase calibration delay is set to one cycle of the modulator clock
0000 0010 = 2d	Input channel 1 phase calibration delay is set to two cycles of the modulator clock
…	…
1111 1110 = 254d	Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock
1111 1111 = 255d	Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock

Similarly, the channel phase calibration setting for input channel 2 can be configured using the CH2_PCAL (P0_R69) register bits.

8.3.7.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. Table 8-14 shows the predefined –3-dB cutoff frequencies available that can be set by using the HPF_SEL[1:0] register bits of P0_R107. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF_SEL[1:0] register bits are set to 2'b00. Figure 8-19 shows a frequency response plot for the HPF filter.

Table 8-14. HPF Programmable Settings

P0_R107_D[1:0] : HPF_SEL[1:0]	–3-dB CUTOFF FREQUENCY SETTING	–3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	–3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
00	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter
01 (default)	0.00025 × f_S	4 Hz	12 Hz
10	0.002 × f_S	32 Hz	96 Hz
11	0.008 × f_S	128 Hz	384 Hz

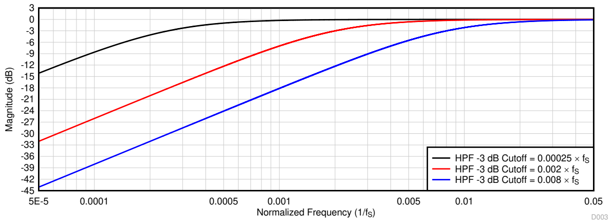


Figure 8-19. HPF Filter Frequency Response Plot

Equation 1 gives the transfer function for the first-order programable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (1)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in Table 8-15 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any ADC channel for recording. These programmable coefficients are 32-bit, two's complement numbers. Table 8-15 shows the filter coefficients for the first-order IIR filter.

Table 8-15. 1st-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	DEFAULT COEFFICIENT VALUE	COEFFICIENT REGISTER MAPPING
Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter)	N_0	0x7FFFFFFF	P4_R72-R75
	N_1	0x00000000	P4_R76-R79
	D_1	0x00000000	P4_R80-R83

8.3.7.5 Programmable Digital Biquad Filters

The PCM6xx0-Q1 supports up to 12 programmable digital biquad filters, out of that only up to six biquad filters are used for the PCM6020-Q1. These highly efficient filters achieve the desired frequence response. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. Equation 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (2)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in the *Programmable Coefficient Registers: Page 2* and *Programmable Coefficient Registers: Page 3* sections. If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. These programmable coefficients are 32-bit, two's complement numbers. As described in Table 8-16, these biquad filters can be allocated for each output channel based on the BIQUAD_CFG[1:0] register setting of P0_R108. By setting BIQUAD_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional filtering is required for the system application. See the *PCM6xx0-Q1 Programmable Biquad Filter Configuration and Applications* application report for further details.

Table 8-16. Biquad Filter Allocation to the Record Output Channel

PROGRAMMABLE BIQUAD FILTER	RECORD OUTPUT CHANNEL ALLOCATION USING P0_R108_D[6:5] REGISTER SETTING		
	BIQUAD_CFG[1:0] = 2'b01 (1 Biquad per Channel)	BIQUAD_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	BIQUAD_CFG[1:0] = 2'b11 (3 Biquads per Channel)
	SUPPORTS ALL 8 CHANNELS	SUPPORTS UP TO 6 CHANNELS	SUPPORTS UP TO 4 CHANNELS
Biquad filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 5	Not used	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 6	Not used	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 9	Not used	Not used	Allocated to output channel 1
Biquad filter 10	Not used	Not used	Allocated to output channel 2

Table 8-17 shows the biquad filter coefficients mapping to the register space.

Table 8-17. Biquad Filter Coefficients Register Mapping

PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING	PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING
Biquad filter 1	P2_R8-R27	Biquad filter 6	P2_R108-R127
Biquad filter 2	P2_R28-R47	Biquad filter 9	P3_R48-R67
Biquad filter 5	P2_R88-R107	Biquad filter 10	P3_R68-R87

8.3.7.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise. Table 8-18 lists the configuration settings available for channel summing mode.

Table 8-18. Channel Summing Mode Programmable Settings

P0_R107_D[3:2] : CH_SUM[2:0]	CHANNEL SUMMING MODE FOR INPUT CHANNELS	SNR AND DYNAMIC RANGE BOOST
00 (default)	Channel summing mode is disabled	Not applicable
01	Output channel 1 = (input channel 1 + input channel 2) / 2	3-dB boost in SNR and dynamic range
	Output channel 2 = (input channel 1 + input channel 2) / 2	
10 and 11	Reserved (do not use this setting)	Not applicable

The device additionally supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. The programmable mixer feature is available only if CH_SUM[2:0] is set to 2'b00. Figure 8-20 shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the *Programmable Coefficient Registers: Page 4* section. All mixer coefficients are 32-bit, two's complement numbers using a 1.31 number format. The value of 0x7FFFFFFF is equivalent to +1 (0-dB gain), the value 0x00000000 is equivalent to mute (zero data), and any values in between set the mixer attenuation computed using Equation 3. If the MSB is set to '1' then the attenuation remains the same but the signal phase is inverted. All IIR filter programmable coefficients are 32-bit, two's complement numbers.

$$\text{hex2dec (value)} / 2^{31} \tag{3}$$

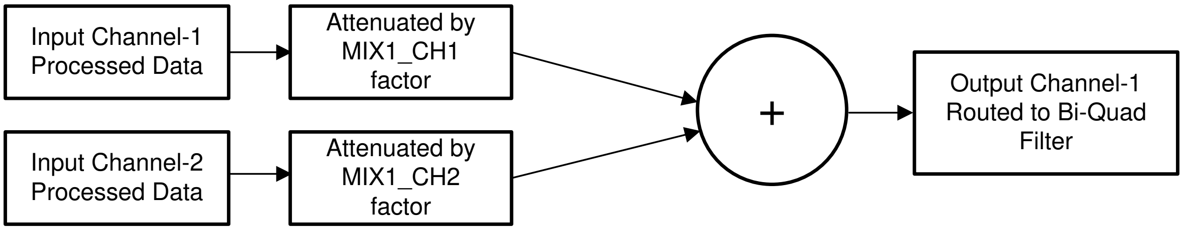


Figure 8-20. Programmable Digital Mixer Block Diagram

A similar mixer operation is performed by mixer 2 to generate output channel 2.

8.3.7.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. As illustrated in Figure 8-18, this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the DECI_FILT, P0_R107_D[5:4] register bits. Table 8-19 shows the configuration register setting for the decimation filter mode selection for the record channel.

Table 8-19. Decimation Filter Mode Selection for the Record Channel

P0_R107_D[5:4] : DECI_FILT[1:0]	DECIMATION FILTER MODE SELECTION
00 (default)	Linear phase filters are used for the decimation
01	Low-latency filters are used for the decimation
10	Ultra-low latency filters are used for the decimation
11	Reserved (do not use this setting)

8.3.7.7.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

8.3.7.7.1.1 Sampling Rate: 8 kHz or 7.35 kHz

Figure 8-21 and Figure 8-22 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 8 kHz or 7.35 kHz. Table 8-20 lists the specifications for a decimation filter with an
8-kHz or 7.35-kHz sampling rate.

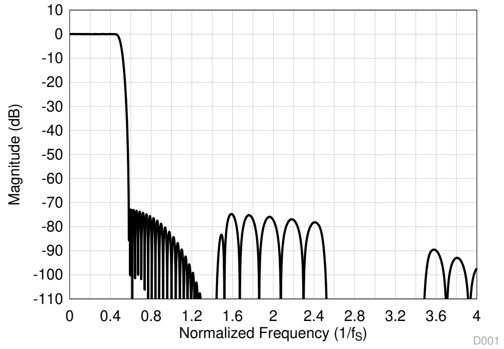


Figure 8-21. Linear Phase Decimation Filter Magnitude Response

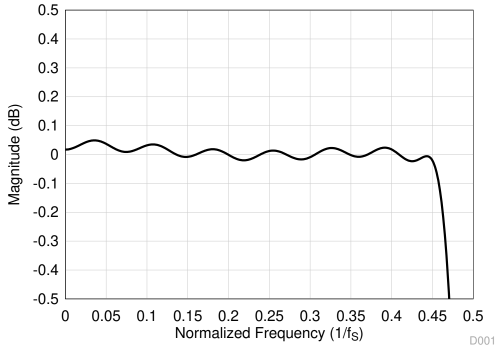


Figure 8-22. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-20. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

8.3.7.7.1.2 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-23 and Figure 8-24 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-21 lists the specifications for a decimation filter with an 16-kHz or 14.7-kHz sampling rate.

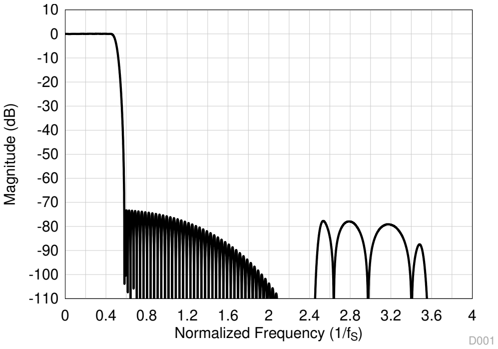


Figure 8-23. Linear Phase Decimation Filter Magnitude Response

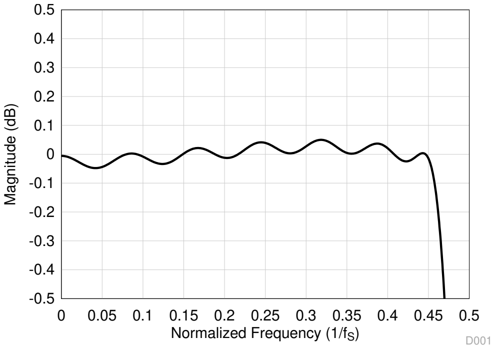


Figure 8-24. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-21. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		1/f_S

8.3.7.7.1.3 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-25 and Figure 8-26 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-22 lists the specifications for a decimation filter with an 24-kHz or 22.05-kHz sampling rate.

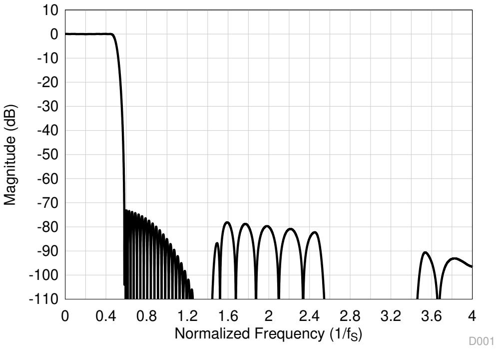


Figure 8-25. Linear Phase Decimation Filter Magnitude Response

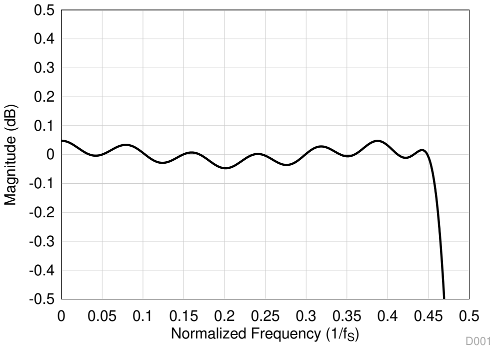


Figure 8-26. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-22. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		1/f_S

8.3.7.7.1.4 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-27 and Figure 8-28 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-23 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

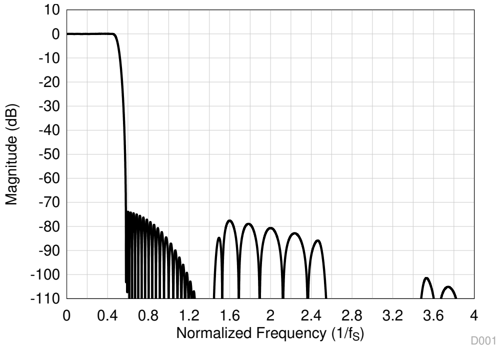


Figure 8-27. Linear Phase Decimation Filter Magnitude Response

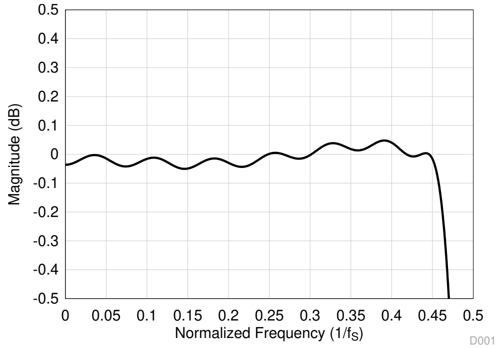


Figure 8-28. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-23. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		1/f_S

8.3.7.7.1.5 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-29 and Figure 8-30 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-24 lists the specifications for a decimation filter with an 48-kHz or 44.1-kHz sampling rate.

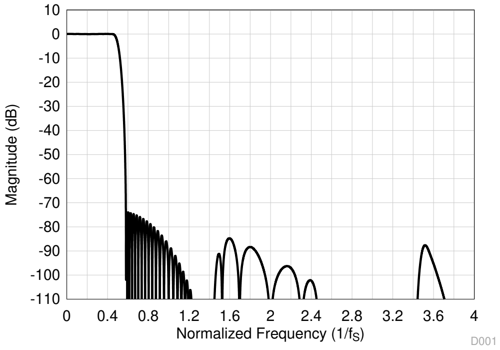


Figure 8-29. Linear Phase Decimation Filter Magnitude Response

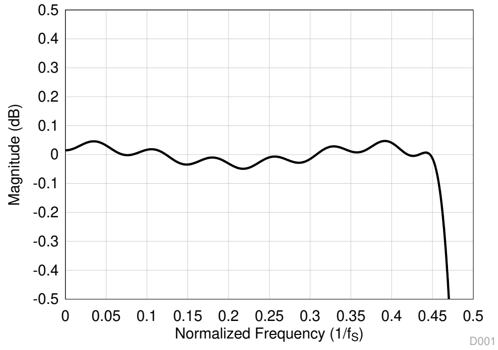


Figure 8-30. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-24. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.7.7.1.6 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-31 and Figure 8-32 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-25 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.

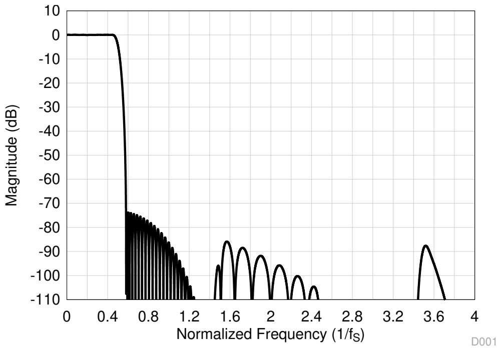


Figure 8-31. Linear Phase Decimation Filter Magnitude Response

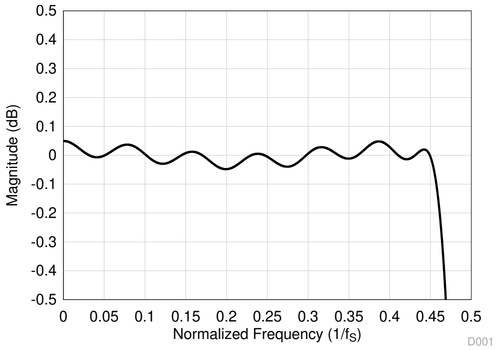


Figure 8-32. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-25. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.7.7.1.7 Sampling Rate: 192 kHz or 176.4 kHz

Figure 8-33 and Figure 8-34 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 192 kHz or 176.4 kHz. Table 8-26 lists the specifications for a decimation filter with an 192-kHz or 176.4-kHz sampling rate.

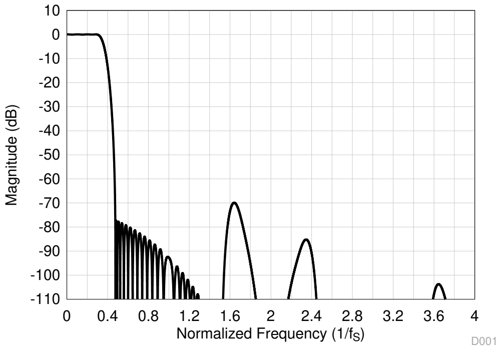


Figure 8-33. Linear Phase Decimation Filter Magnitude Response

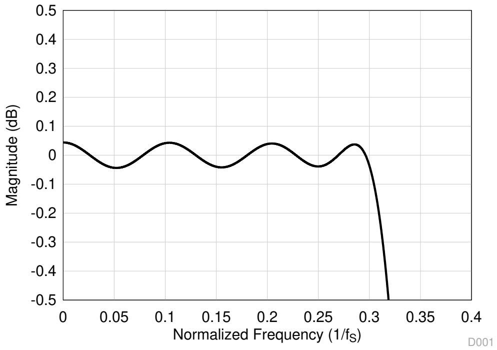


Figure 8-34. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-26. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		1/f_S

8.3.7.7.1.8 Sampling Rate: 384 kHz or 352.8 kHz

Figure 8-35 and Figure 8-36 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 384 kHz or 352.8 kHz. Table 8-27 lists the specifications for a decimation filter with an 384-kHz or 352.8-kHz sampling rate.

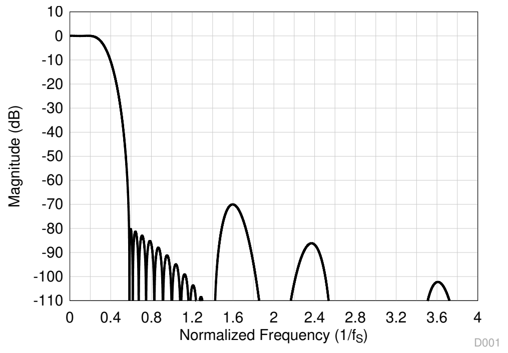


Figure 8-35. Linear Phase Decimation Filter Magnitude Response

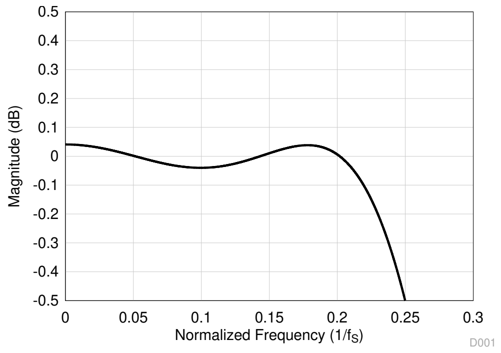


Figure 8-36. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-27. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.212 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	108.8			
Group delay or latency	Frequency range is 0 to 0.212 × f_S		7.2		1/f_S

8.3.7.7.1.9 Sampling Rate: 768 kHz or 705.6 kHz

Figure 8-37 and Figure 8-38 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 768 kHz or 705.6 kHz. Table 8-28 lists the specifications for a decimation filter with an 768-kHz or 705.6-kHz sampling rate.

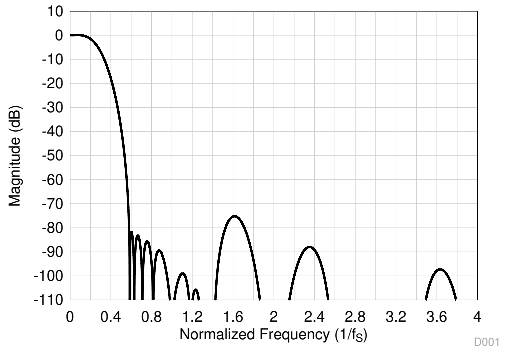


Figure 8-37. Linear Phase Decimation Filter Magnitude Response

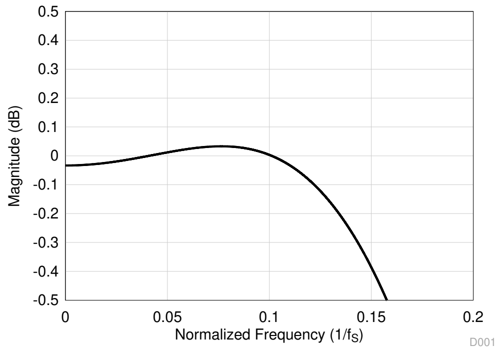


Figure 8-38. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-28. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.113 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 2 × f_S	75.0			dB
	Frequency range is 2 × f_S onwards	88.0			
Group delay or latency	Frequency range is 0 to 0.113 × f_S		5.9		1/f_S

8.3.7.7.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCM6020-Q1 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

8.3.7.7.2.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-39 shows the magnitude response and Figure 8-40 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-29 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

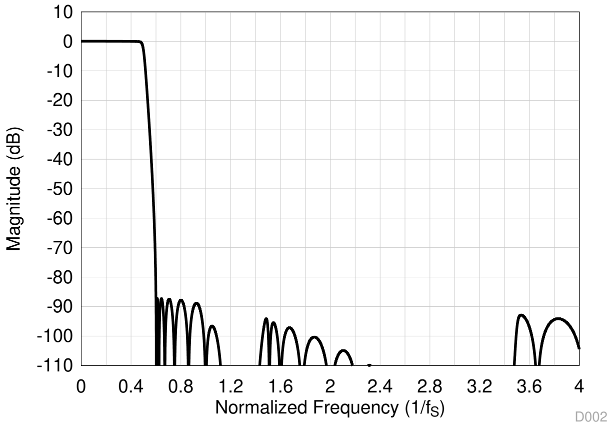


Figure 8-39. Low-Latency Decimation Filter Magnitude Response

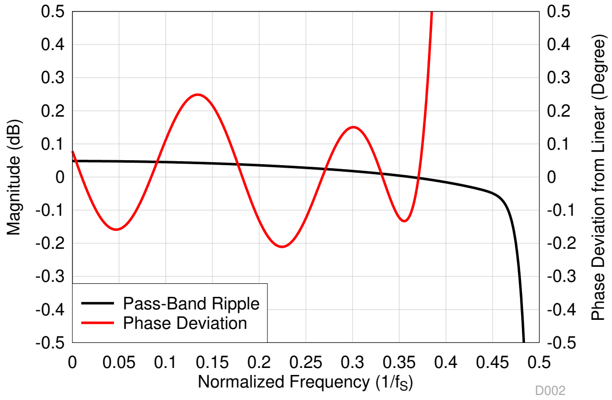


Figure 8-40. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-29. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	$1/f_S$
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

8.3.7.7.2.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-41 shows the magnitude response and Figure 8-42 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-30 lists the specifications for a decimation filter with a 24-kHz or 22.05-kHz sampling rate.

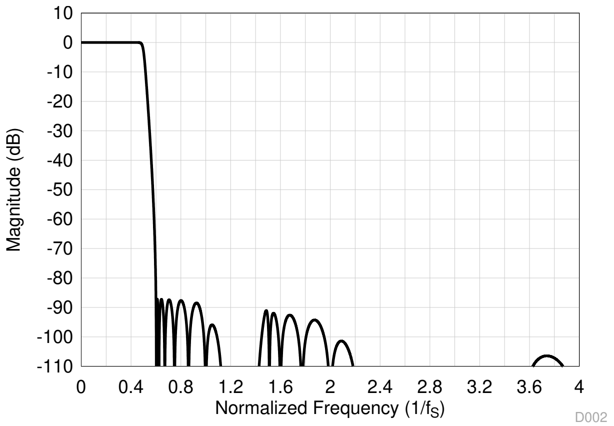


Figure 8-41. Low-Latency Decimation Filter Magnitude Response

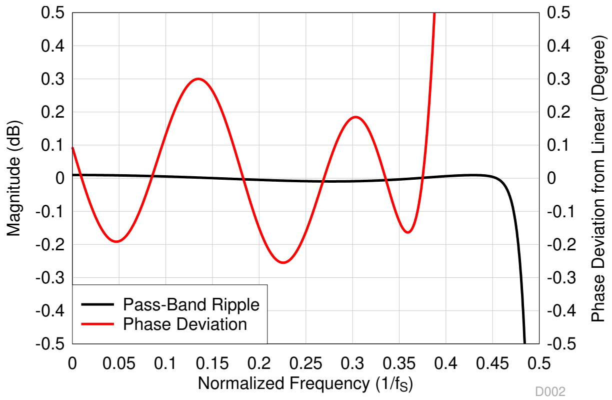


Figure 8-42. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-30. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.7.7.2.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-43 shows the magnitude response and Figure 8-44 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-31 lists the specifications for a decimation filter with a 32-kHz or 29.4-kHz sampling rate.

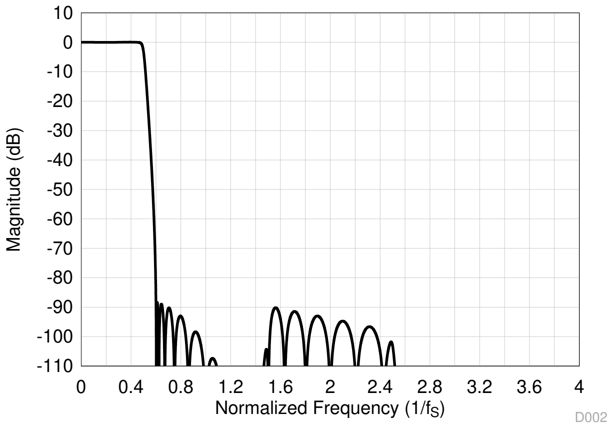


Figure 8-43. Low-Latency Decimation Filter Magnitude Response

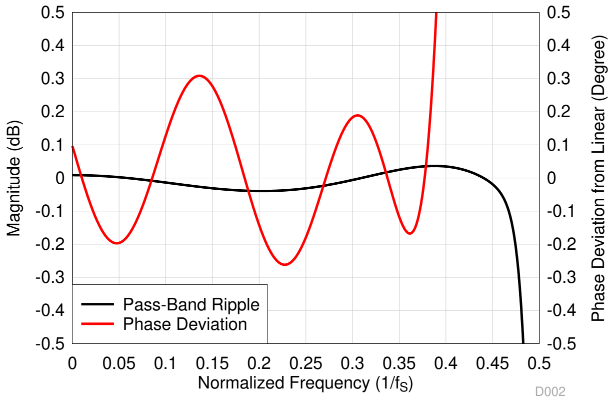


Figure 8-44. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-31. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

8.3.7.7.2.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-45 shows the magnitude response and Figure 8-46 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-32 lists the specifications for a decimation filter with a 48-kHz or 44.1-kHz sampling rate.

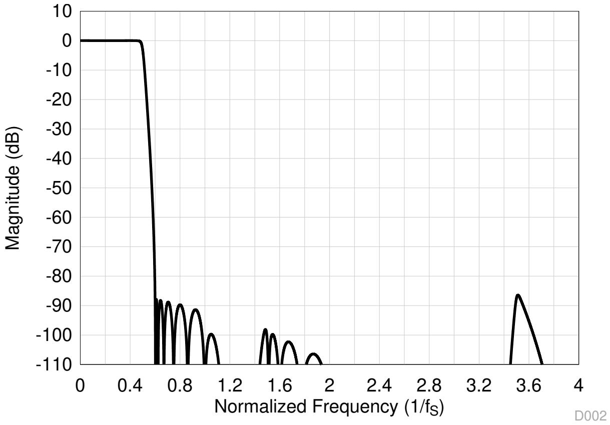


Figure 8-45. Low-Latency Decimation Filter Magnitude Response

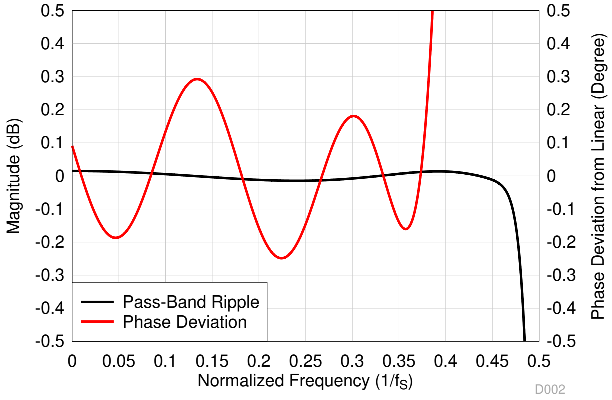


Figure 8-46. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-32. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

8.3.7.7.2.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-47 shows the magnitude response and Figure 8-48 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-33 lists the specifications for a decimation filter with a 96-kHz or 88.2-kHz sampling rate.

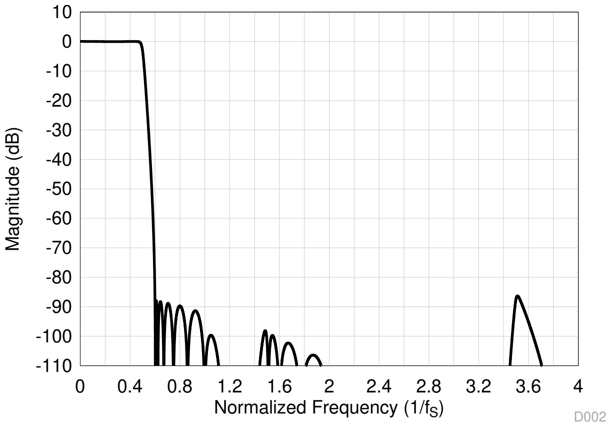


Figure 8-47. Low-Latency Decimation Filter Magnitude Response

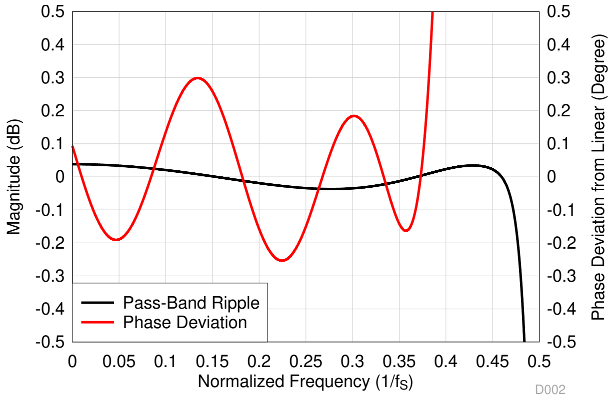


Figure 8-48. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-33. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.7.7.2.6 Sampling Rate: 192 kHz or 176.4 kHz

Figure 8-49 shows the magnitude response and Figure 8-50 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 192 kHz or 176.4 kHz. Table 8-34 lists the specifications for a decimation filter with a 192-kHz or 176.4-kHz sampling rate.

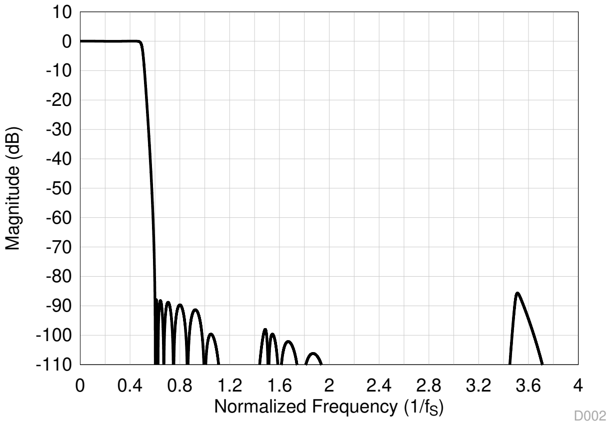


Figure 8-49. Low-Latency Decimation Filter Magnitude Response

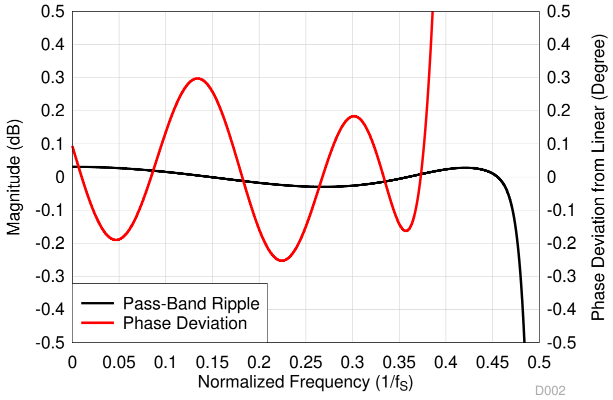


Figure 8-50. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-34. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	1/f_S
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.7.7.3 Ultra-Low-Latency Filters

For applications where ultra-low latency (within the audio band) is critical, the ultra-low-latency decimation filters on the PCM6020-Q1 can be used. The device supports these filters with a group delay of approximately four samples with an almost linear phase response within the 0.325 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the ultra-low-latency filters.

8.3.7.7.3.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-51 shows the magnitude response and Figure 8-52 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-35 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

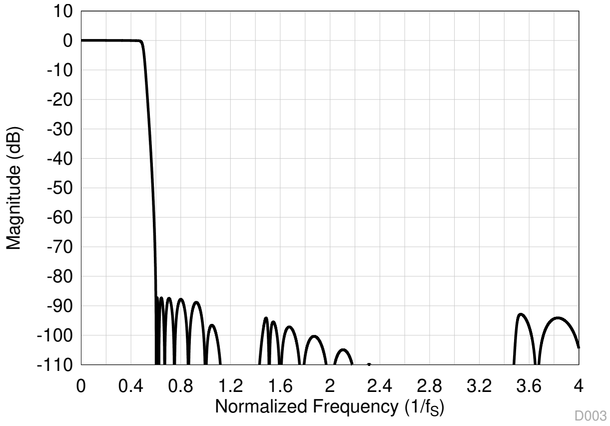


Figure 8-51. Ultra-Low-Latency Decimation Filter Magnitude Response

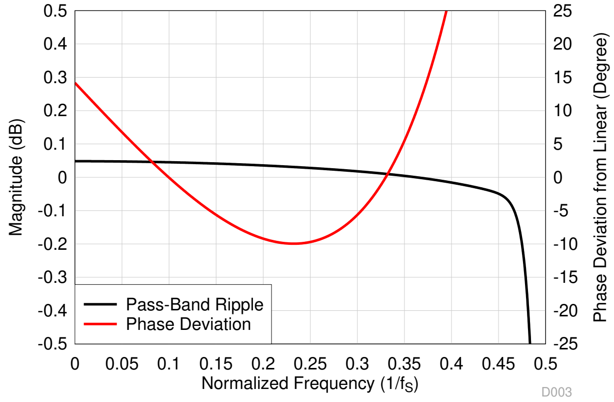


Figure 8-52. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-35. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.45 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.3		1/f_S
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.512		0.512	1/f_S
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.2	Degrees

8.3.7.7.3.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-53 shows the magnitude response and Figure 8-54 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-36 lists the specifications for a decimation filter with a 24-kHz or 22.05-kHz sampling rate.

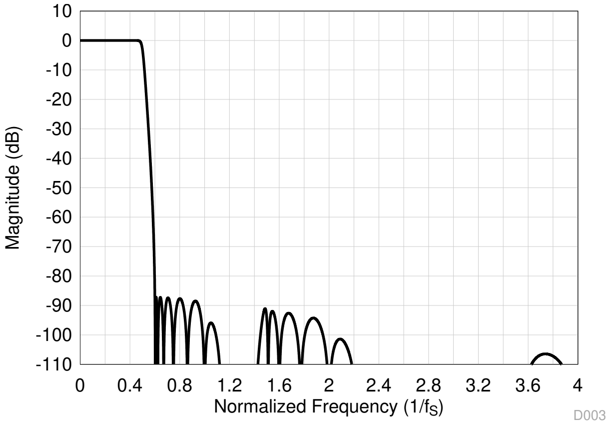


Figure 8-53. Ultra-Low-Latency Decimation Filter Magnitude Response

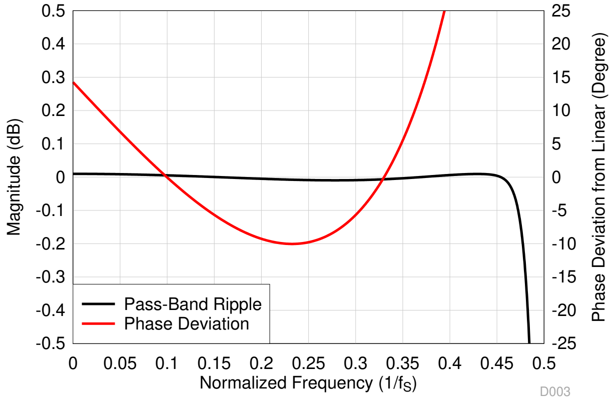


Figure 8-54. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-36. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.46 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.1			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		1/f_S
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.514		0.514	1/f_S
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.3	Degrees

8.3.7.7.3.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-55 shows the magnitude response and Figure 8-56 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-37 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

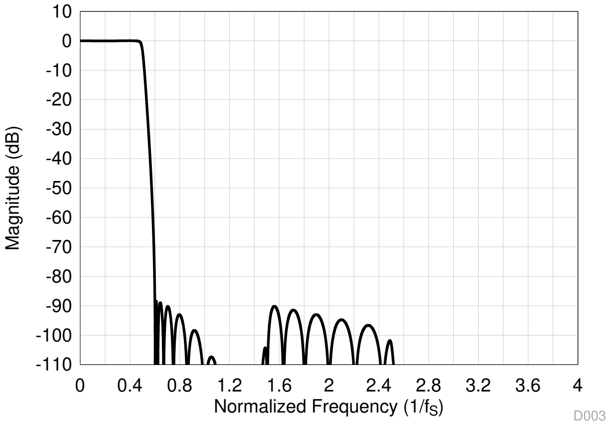


Figure 8-55. Ultra-Low-Latency Decimation Filter Magnitude Response

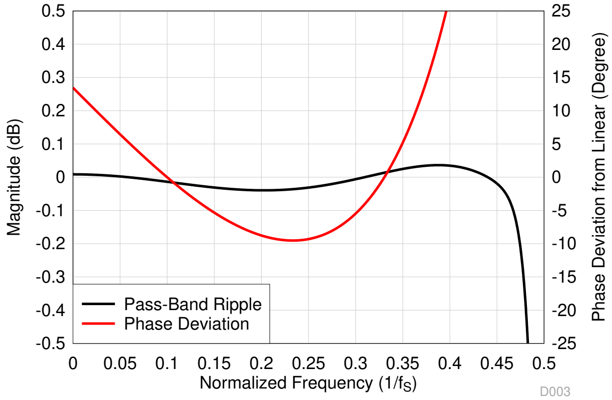


Figure 8-56. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-37. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		5.2		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.492		0.492	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–9.5		13.5	Degrees

8.3.7.7.3.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-57 shows the magnitude response and Figure 8-58 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-38 lists the specifications for a decimation filter with a 48-kHz or 44.1-kHz sampling rate.

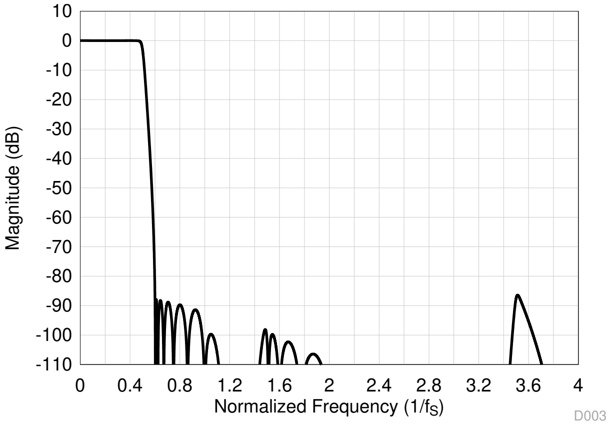


Figure 8-57. Ultra-Low-Latency Decimation Filter Magnitude Response

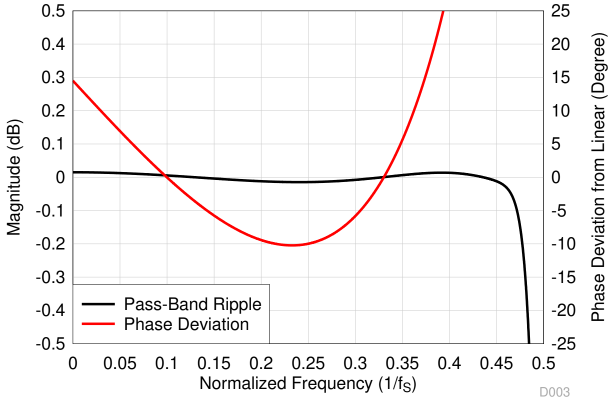


Figure 8-58. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-38. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.525		0.525	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.3		14.5	Degrees

8.3.7.7.3.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-59 shows the magnitude response and Figure 8-60 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-39 lists the specifications for a decimation filter with a 96-kHz or 88.2-kHz sampling rate.

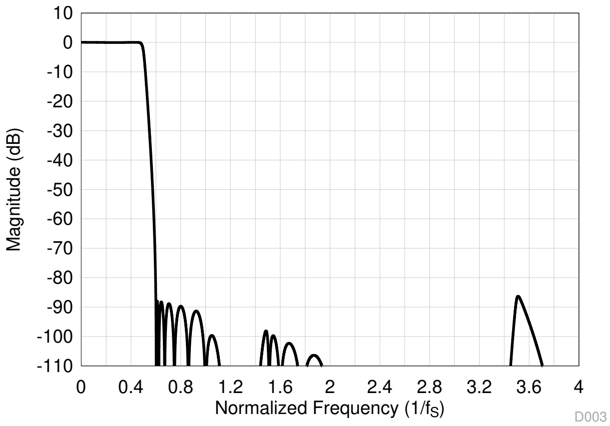


Figure 8-59. Ultra-Low-Latency Decimation Filter Magnitude Response

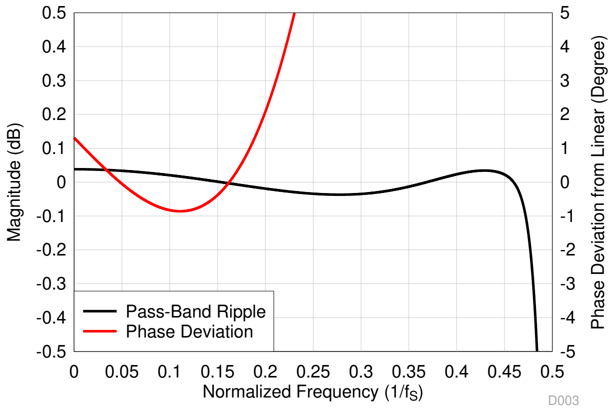


Figure 8-60. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-39. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.1625 × f_S		3.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.1625 × f_S	–0.091		0.091	1/f_S
Phase deviation	Frequency range is 0 to 0.1625 × f_S	–0.86		1.30	Degrees

8.3.7.7.3.6 Sampling Rate: 192 kHz or 176.4 kHz

Figure 8-61 shows the magnitude response and Figure 8-62 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 192 kHz or 176.4 kHz. Table 8-40 lists the specifications for a decimation filter with a 192-kHz or 176.4-kHz sampling rate.

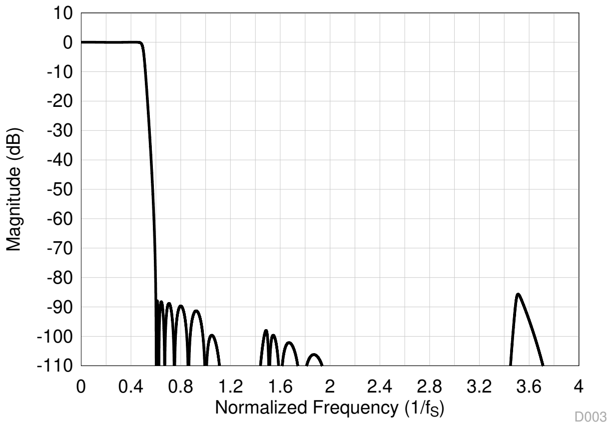


Figure 8-61. Ultra-Low-Latency Decimation Filter Magnitude Response

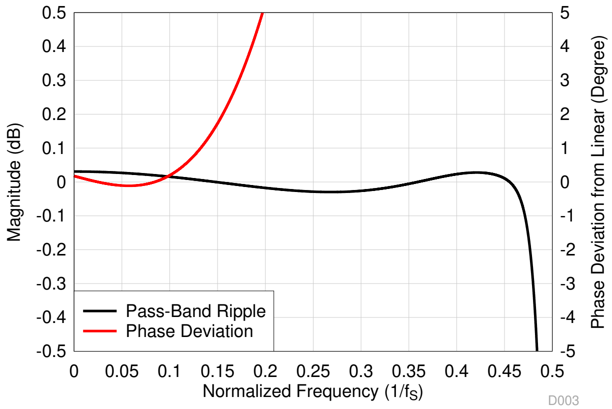


Figure 8-62. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-40. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.085 × f_S		3.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.085 × f_S	–0.024		0.024	$1/f_S$
Phase deviation	Frequency range is 0 to 0.085 × f_S	–0.12		0.18	Degrees

8.3.7.7.3.7 Sampling Rate: 384 kHz or 352.8 kHz

Figure 8-63 shows the magnitude response and Figure 8-64 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 384 kHz or 352.8 kHz. Table 8-41 lists the specifications for a decimation filter with a 384-kHz or 352.8-kHz sampling rate.

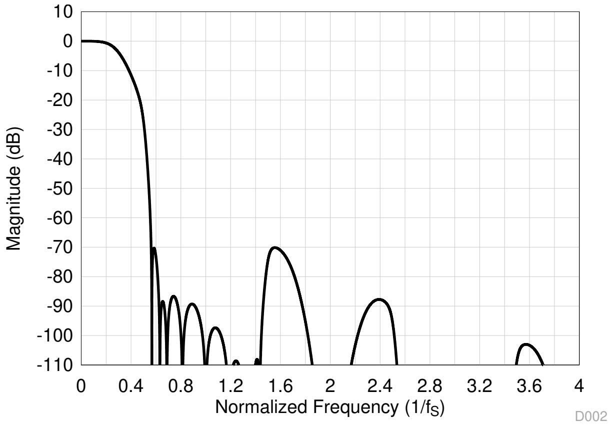


Figure 8-63. Ultra-Low-Latency Decimation Filter Magnitude Response

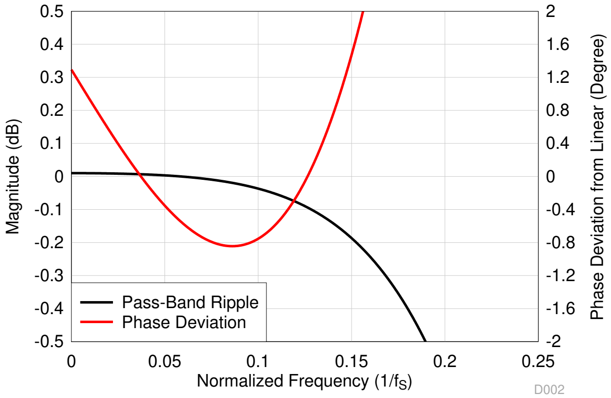


Figure 8-64. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-41. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.1 × f_S	–0.04		0.01	dB
Stop-band attenuation	Frequency range is 0.56 × f_S onwards	70.1			dB
Group delay or latency	Frequency range is 0 to 0.157 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.157 × f_S	–0.18		0.18	$1/f_S$
Phase deviation	Frequency range is 0 to 0.157 × f_S	–0.85		2.07	Degrees

8.3.8 Automatic Gain Controller (AGC)

The device includes an automatic gain controller (AGC) for ADC recording that must be used only for the AC-coupled input configuration. As shown in Figure 8-65, the AGC can be used to maintain a nominally constant output level when recording speech. Instead of manually setting the channel gain in AGC mode, the circuitry automatically adjusts the channel gain when the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters, including target level, maximum gain allowed, attack and release (or decay) time constants, and noise thresholds that allow the algorithm to be fine-tuned for any particular application.

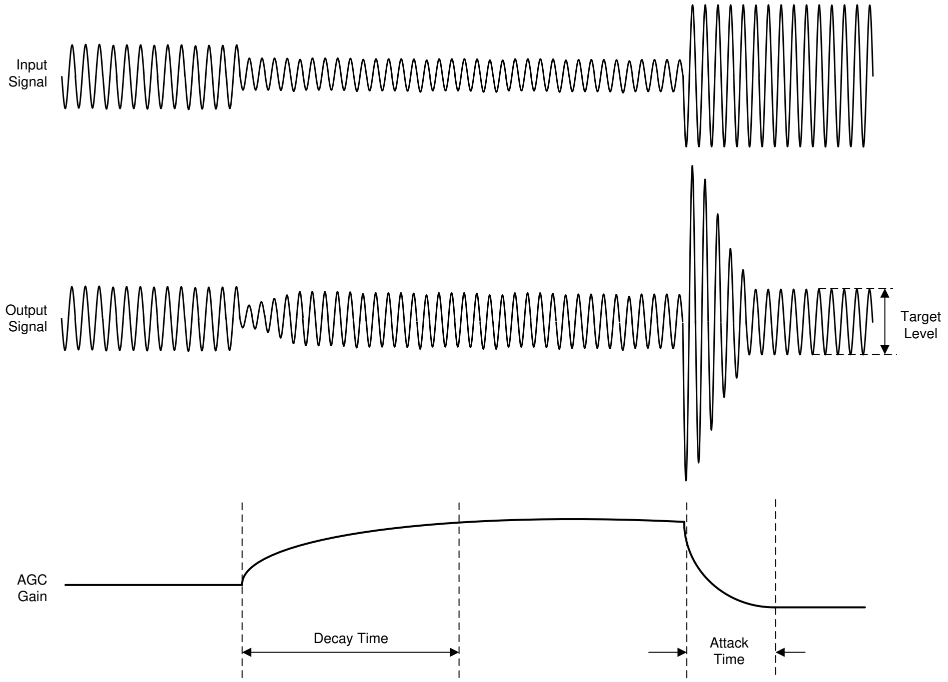


Figure 8-65. AGC Characteristics

The target level (AGC_LVL) represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The PCM6020-Q1 allows programming of different target levels, which can be programmed from –6 dB to –36 dB relative to a full-scale signal, and the AGC_LVL default value is set to –34 dB. The target level is recommended to be set with enough margin to prevent clipping when loud sounds occur. Table 8-42 lists the AGC target level configuration settings.

Table 8-42. AGC Target Level Programmable Settings

P0_R112_D[7:4] : AGC_LVL[3:0]	AGC TARGET LEVEL FOR OUTPUT
0000	The AGC target level is the –6-dB output signal level
0001	The AGC target level is the –8-dB output signal level
0010	The AGC target level is the –10-dB output signal level
…	…
1110 (default)	The AGC target level is the –34-dB output signal level
1111	The AGC target level is the –36-dB output signal level

The maximum gain allowed (AGC_MAXGAIN) gives flexibility to the designer to restrict the maximum gain applied by the AGC. This feature limits the channel gain in situations where environmental noise is greater than the programmed noise threshold. The AGC_MAXGAIN can be programmed from 3 dB to 42 dB with steps of 3 dB and the default value is set to 24 dB. Table 8-43 lists the AGC_MAXGAIN configuration settings.

Table 8-43. AGC Maximum Gain Programmable Settings

P0_R112_D[3:0] : AGC_MAXGAIN[3:0]	AGC MAXIMUM GAIN ALLOWED
0000	The AGC maximum gain allowed is 3 dB
0001	The AGC maximum gain allowed is 6 dB
0010	The AGC maximum gain allowed is 9 dB
…	…
0111 (default)	The AGC maximum gain allowed is 24 dB
…	…
1110	The AGC maximum gain allowed is 39 dB
1111	The AGC maximum gain allowed is 42 dB

For further details on the AGC various configurable parameter and application use, see the *Using the Automatic Gain Controller in PCM6xx0-Q1* application report.

8.3.9 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. Such event are an audio serial interface (ASI) bus error and input DC fault diagnostic faults. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down the record channel as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the record channel. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7], P0_R51_D7 is set low. The clock fault is also available for readback in the live fault status register bit INT_LIVE0, P1_R44 as well as latched to the fault status register bit INT_LTCH0, P0_R44, which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault statuses. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIOx pins and also can be configured as an open-drain output so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

When an input DC fault event is detected, the internal IRQ signal is asserted if the interrupt mask registers INT_MASK1, P0_R42 and INT_MASK2, P0_R43 are configured appropriately to unmask all the desired fault diagnostics interrupts. Each input channel can be independently set for an interrupt mask. Table 8-44 and Table 8-45 list the mask settings available for the input DC diagnostics fault interrupts.

Table 8-44. Interrupt Mask Register-1 for DC Faults Diagnostic

P0_R42 : INT_MASK1	INTERRUPT MASK REGISTER 1 FOR DC FAULTS DIAGNOSTIC INTERRUPTS
INT_MASK1[7]	Channel 1 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[6]	Channel 2 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[5]	Channel 3 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[4]	Channel 4 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[3]	Channel 5 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[2]	Channel 6 input DC faults diagnostic interrupt mask and unmask register bit
INT_MASK1[1]	Short to the VBAT_IN (when VBAT_IN is lower than MICBIAS) fault interrupt mask and unmask register bit
INT_MASK1[0]	Reserved

Table 8-45. Interrupt Mask Register-2 for DC Faults Diagnostic

P0_R43 : INT_MASK2	INTERRUPT MASK REGISTER 2 FOR DC FAULTS DIAGNOSTIC INTERRUPTS
INT_MASK2[7]	Open the input fault interrupt mask and unmask register bit for all channels
INT_MASK2[6]	Inputs shorted each other fault interrupt mask and unmask register bit for all channels
INT_MASK2[5]	IN1P input shorted to ground fault interrupt mask and unmask register bit for all channels
INT_MASK2[4]	IN1M input shorted to ground fault interrupt mask and unmask register bit for all channels
INT_MASK2[3]	IN1P input shorted to MICBIAS fault interrupt mask and unmask register bit for all channels
INT_MASK2[2]	IN1M input shorted to MICBIAS fault interrupt mask and unmask register bit for all channels
INT_MASK2[1]	IN1P input shorted to VBAT_IN fault interrupt mask and unmask register bit for all channels
INT_MASK2[0]	IN1M input shorted to VBAT_IN fault interrupt mask and unmask register bit for all channels

The device supports the channel-specific input DC fault latched status registers for all channels from CH1_LTCH, P0_R46 to CH2_LTCH, P0_R47, which are read-only registers. The device also has a consolidated summary status register across channels for the input DC latched fault status register, CHx_LTCH, P0_R45 that the host can read to quickly know which channel fault has occurred. Reading the latched fault status registers, CH1_LTCH to CH2_LTCH, clears all the latched fault status including the summary status register, CHx_LTCH. Table 8-46 shows various input DC fault diagnostics status bits that are supported by the device.

Table 8-46. Input DC Faults Diagnostic Latched Status

P0_R46 : CH1_LTCH	CHANNEL 1 INPUT FAULTS DIAGNOSTIC LATCHED STATUS
CH1_LTCH[7]	Channel 1 open input fault detection status bit (self-clearing bit)
CH1_LTCH[6]	Channel 1 inputs shorted together fault detection status bit (self-clearing bit)
CH1_LTCH[5]	Channel 1 IN1P input shorted to ground fault detection status bit (self-clearing bit)
CH1_LTCH[4]	Channel 1 IN1M input shorted to ground fault detection status bit (self-clearing bit)
CH1_LTCH[3]	Channel 1 IN1P input shorted to MICBIAS fault detection status bit (self-clearing bit)
CH1_LTCH[2]	Channel 1 IN1M input shorted to MICBIAS fault detection status bit (self-clearing bit)
CH1_LTCH[1]	Channel 1 IN1P input shorted to VBAT_IN fault detection status bit (self-clearing bit)
CH1_LTCH[0]	Channel 1 IN1M input shorted to VBAT_IN fault detection status bit (self-clearing bit)

Similarly, the DC faults diagnostic latched status for input channel 2 can be monitored using the CH2_LTCH (P0_R47) register.

The device GPIOx pins can be additionally configured to route the internal IRQ interrupt signal on the GPIOx pins and also can be configured as an open-drain output so that this pin can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as an active low or active high polarity by setting the INT_POL, P0_R40_D7 register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0], P0_R40_D[6:5] register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live status registers that determine if all the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in P0_R118, DEV_STS0 and P0_R119, DEV_STS1.

The device has a GPIO1 multifunction pin that can be configured for a desired specific function. Additionally the device has two more GPIO pins and two GPI pins supported that can be used in the system for various other features. Table 8-47 shows all possible allocation of these multifunction pins for all the various features.

Table 8-47. Multifunction Pin Assignments

ROW	PIN FUNCTION	GPIO1	GPIO2	GPIO3	GPI1	GPI2
—	—	GPIO1_CFG [4:0]	GPIO2_CFG [4:0]	GPIO3_CFG [4:0]	GPI1_CFG[4:0]	GPI2_CFG[4:0]
—	—	P0_R33[7:4]	P0_R34[7:4]	P0_R35[7:4]	P0_R36[7:4]	P0_R37[7:4]
A	Pin disabled	S(1)	S (default)	S (default)	S (default)	S (default)
B	General-purpose output (GPO)	S	S	S	NS(2)	NS
C	Interrupt output (IRQ)	S (default)	S	S	NS	NS
D	Secondary ASI output (SDOUT2)	S	S	S	NS	NS
F	MiCBIAS on/off input (BIASEN)	S	S	S	S	S
G	General-purpose input (GPI)	S	S	S	S	S
H	Master clock input (MCLK)	S	S	S	S	S
I	ASI daisy-chain input (SDIN)	S	S	S	S	S

(1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.
(2) NS means the feature mentioned in this row is *not supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.

Each GPIOx pin can be independently set for the desired drive configurations setting using the GPIOx_DRV[3:0] register bits. Table 8-48 lists the drive configuration settings.

Table 8-48. GPIOx Pins Drive Configuration Settings

P0_R33_D[3:0] : GPIO1_DRV[3:0]	GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1
000	The GPIO1 pin is set to high impedance (floated)
001	The GPIO1 pin is set to be driven active low or active high
010 (default)	The GPIO1 pin is set to be driven active low or weak high (on-chip pullup)
011	The GPIO1 pin is set to be driven active low or Hi-Z (floated)
100	The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high
101	The GPIO1 pin is set to be driven Hi-Z (floated) or active high
110 and 111	Reserved (do not use these settings)

Similarly, the GPIO2 and GPIO3 pins can be configured using the GPIO2_DRV(P0_R34) and GPIO3_DRV(P0_R35) register bits, respectively.

When configured as a general-purpose output (GPO), the GPIOx pin values can be driven by writing the GPIO_VAL P0_R38 registers. The GPIO_MON, P0_R39 register can be used to readback the status of the GPIOx and GPIx pins when configured as a general-purpose input (GPI).

8.4 Device Functional Modes

8.4.1 Hardware Shutdown

The device enters hardware shutdown mode when the SHDNZ pin is asserted low or the AVDD supply voltage is not applied to the device. In hardware shutdown mode, the device consumes the minimum quiescent current from the AVDD supply. All configuration registers and programmable coefficients lose their value in this mode, and I^2C or SPI communication to the device is not supported.

If the SHDNZ pin is asserted low when the device is in active mode, the device ramps down volume on the record data, powers down the analog and digital blocks, and puts the device into hardware shutdown mode in 25 ms (typical). The device can also be immediately put into hardware shutdown mode from active mode if the SHDNZ_CFG[1:0], P0_R5_D[3:2], register bits are set to 2'b00. After the SHDNZ pin is asserted low, and after the device enters hardware shutdown mode, keep the SHDNZ pin low for at least 1 ms before releasing SHDNZ for further device operation.

Assert the SHDNZ pin high only when the IOVDD supply settles to a steady voltage level. When the SHDNZ pin goes high, the device sets all configuration registers and programmable coefficients to their default values, and then enters sleep mode.

8.4.2 Sleep Mode or Software Shutdown

In sleep mode or software shutdown mode, the device consumes very low quiescent current from the AVDD supply and, at the same time, allows the I^2C or SPI communication to wake the device for active operation.

The device can also enter sleep mode when the host device sets the SLEEP_ENZ, P0_R2_D0 bit to 1'b0. If the SLEEP_ENZ bit is asserted low when the device is in active mode, the device ramps down the volume on the record data, powers down the analog and digital blocks, and enters sleep mode. However, the device still continues to retain the last programmed value of the device configuration registers and programmable coefficients.

In sleep mode, do not perform any I^2C or SPI transactions, except for exiting sleep mode in order to enter active mode. After entering sleep mode, wait at least 10 ms before starting I^2C or SPI transactions to exit sleep mode.

8.4.3 Active Mode

If the host device exits sleep mode by setting the SLEEP_ENZ bit to 1'b1, the device enters active mode. In active mode, I^2C or SPI transactions can be done to configure and power-up the device for active operation. After entering active mode, wait at least 1 ms before starting any I^2C or SPI transactions in order to allow the device to complete the internal wake-up sequence.

After configuring all other registers for the target application and system settings, configure the input and output channel enable registers, P0_R115 (IN_CH_EN) and P0_R116 (ASI_OUT_CH_EN), respectively. Lastly, configure the device power-up register, P0_R117 (PWR_CFG). All programmable coefficient values must be written before powering up the respective channel.

In active mode, the power-up and power-down status of various blocks is monitored by reading the read-only device status bits located in the P0_R117 (DEV_STS0) and P0_R118 (DEV_STS1) registers.

8.4.4 Software Reset

A software reset can be done any time by asserting the SW_RESET bit, P0_R1_D0, which is a self-clearing bit. This software reset immediately shuts down the device, and restores all device configuration registers and programmable coefficients to their default values.

8.5 Programming

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. These registers are called *device control registers* and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). Page 1 consists of the live status registers and input diagnostic successive-approximation register (SAR) data for advanced diagnostic purposes. All programmable coefficient registers are located in page 2, page 3, and page 4. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

8.5.1 Control Serial Interfaces

The device control registers can be accessed using either I^{2}C or SPI communication to the device.

By monitoring the SDA_SSZ, SCL_MOSI, ADDR0_SCLK, and ADDR1_MISO device pins, which are the multiplexed pins for the I^{2}C or SPI Interface, the device automatically detects whether the host device is using I^{2}C or SPI communication to configure the device. For a given end application, the host device must always use either the I^{2}C or SPI interface, but not both, to configure the device.

8.5.1.1 I^{2}C Control Interface

The device supports the I^{2}C control protocol as a slave device, and is capable of operating in standard mode, fast mode, and fast mode plus. The I^{2}C control protocol requires a 7-bit slave address. The five most significant bits (MSBs) of the slave address are fixed at 10010 and cannot be changed. The two least significant bits (LSBs) are programmable and are controlled by the ADDR0_SCLK and ADDR1_MISO pins. These two pins must always be either pulled to VSS or IOVDD. If the I2C_BRDCAST_EN (P0_R2_D2) bit is set to 1'b1, then the I^{2}C slave address is fixed to 1001000 in order to allow simultaneous I^{2}C broadcast communication to all PCM6020-Q1 devices in the system. Table 8-49 lists the four possible device addresses resulting from this configuration.

Table 8-49. I^{2}C Slave Address Settings

ADDR1_MISO	ADDR0_SCLK	I2C_BRDCAST_EN (P0_R2_D2)	I^{2}C SLAVE ADDRESS
0	0	0 (default)	1001 000
0	1	0 (default)	1001 001
1	0	0 (default)	1001 010
1	1	0 (default)	1001 011
X	X	1	1001 000

8.5.1.1.1 General I^{2}C Operation

The I^{2}C bus employs two signals, SDA (data) and SCL (clock), to communicate between the integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a START condition on the bus and ends with the master device driving a STOP condition on the bus. The bus uses transitions on the data pin (SDA) when the clock is at logic high to indicate START and STOP conditions. A high-to-low transition on SDA indicates a START, and a low-to-high transition indicates a STOP condition. Normal data-bit transitions must occur within the low time of the clock period.

The master device drives a START condition followed by the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The slave device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this step occurs, the master device transmits the next byte of the sequence. Each slave device is addressed by a unique 7-bit slave address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between START and STOP conditions. When the last word transfers, the master device generates a STOP condition to release the bus. Figure 8-66 shows a generic data transfer sequence.

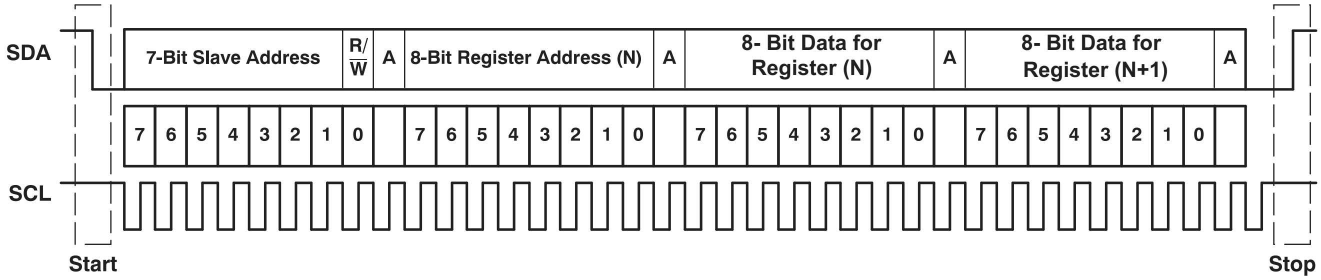


Figure 8-66. Typical I^{2}C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

8.5.1.1.2 I^{2}C Single-Byte and Multiple-Byte Transfers

The device I^{2}C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The device supports sequential I^{2}C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I^{2}C write transaction takes place. For I^{2}C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a STOP or START condition is transmitted, determines how many registers are written.

8.5.1.1.2.1 I^{2}C Single-Byte Write

As shown in Figure 8-67, a single-byte data write transfer begins with the master device transmitting a START condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I^{2}C slave address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the master device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the master transmits the byte of data to be written to the specified register. When finished, the slave device responds with an acknowledge bit (ACK). Finally, the master device transmits a STOP condition to complete the single-byte data write transfer.

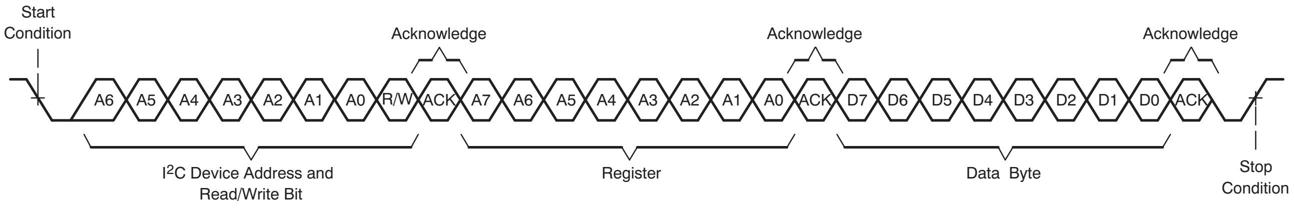


Figure 8-67. I^{2}C Single-Byte Write Transfer

8.5.1.1.2.2 I²C Multiple-Byte Write

As shown in Figure 8-68, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the slave device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the master device transmits a STOP condition after the last data-byte write transfer.

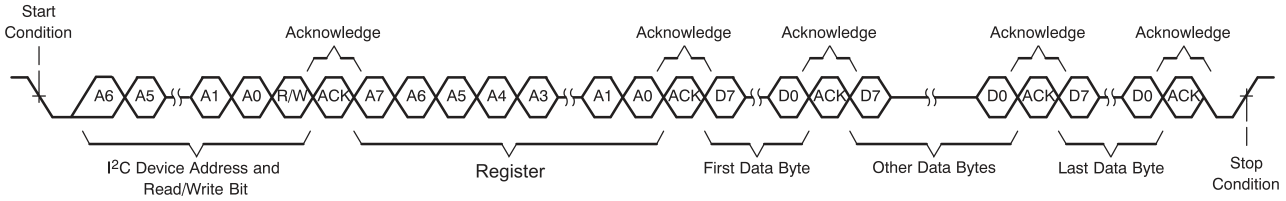


Figure 8-68. I²C Multiple-Byte Write Transfer

8.5.1.1.2.3 I²C Single-Byte Read

As shown in Figure 8-69, a single-byte data read transfer begins with the master device transmitting a START condition followed by the I²C slave address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the slave address and the read/write bit, the device responds with an acknowledge bit (ACK). The master device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The master device transmits another START condition followed by the slave address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the master device transmits a not-acknowledge (NACK) followed by a STOP condition to complete the single-byte data read transfer.

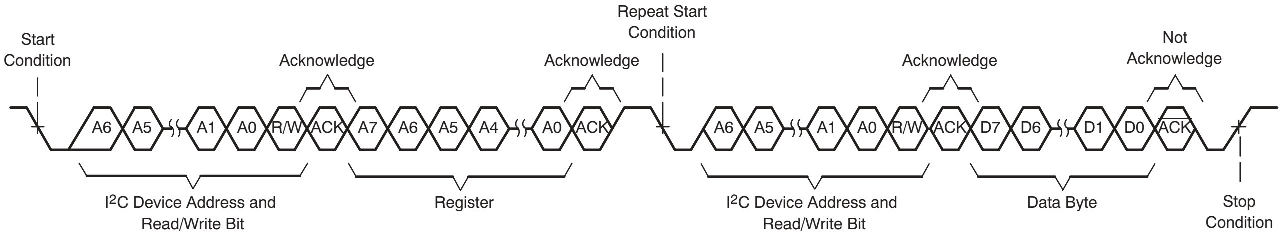


Figure 8-69. I²C Single-Byte Read Transfer

8.5.1.1.2.4 I²C Multiple-Byte Read

As shown in Figure 8-70, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the master device. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the master device transmits a not-acknowledge (NACK) followed by a STOP condition to complete the data read transfer.

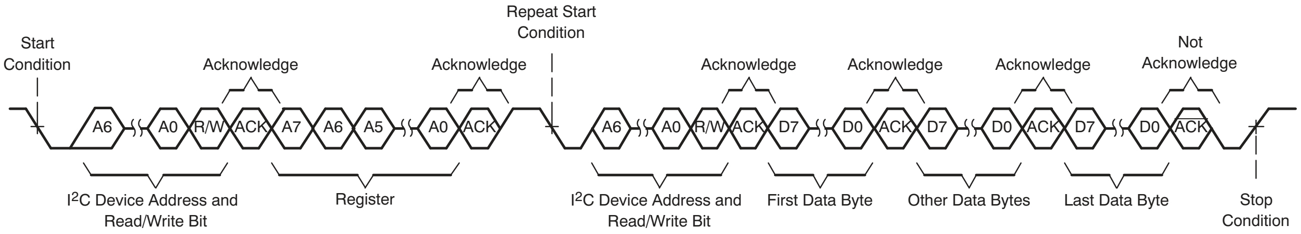


Figure 8-70. I²C Multiple-Byte Read Transfer

8.5.1.2 SPI Control Interface

The general SPI protocol allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions by taking the slave-select pin SSZ from high to low. The SPI slave devices (such as the PCM6020-Q1) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). When the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The PCM6020-Q1 supports a standard SPI control protocol with a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0) and a clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). The SSZ pin can remain low between transmissions; however, the device only interprets the first eight bits transmitted after the falling edge of SSZ as a command byte, and the next eight bits as a data byte only if writing to a register. The device is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI pin prior to the data for that register. Table 8-50 shows the command structure. The first seven bits specify the address of the register that is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus.

In the case of a register write, set the R/W bit to 0. A second byte of data is sent to the MOSI pin and contains the data to be written to the register. A register read is accomplished in a similar fashion. The 8-bit command word sends the 7-bit register address, followed by the R/W bit equal to 1 to signify a register read. The 8-bit register data is then clocked out of the device on the MISO pin during the second eight SCLK clocks in the frame. The device supports sequential SPI addressing for a multiple-byte data write/read transfer until the SSZ pin is pulled high. A multiple-byte data write or read transfer is identical to a single-byte data write or read transfer, respectively, until all data byte transfers complete. The host device must keep the SSZ pin low during all data byte transfers. Figure 8-71 shows the single-byte write transfer and Figure 8-72 illustrates the single-byte read transfer.

Table 8-50. SPI Command Word

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

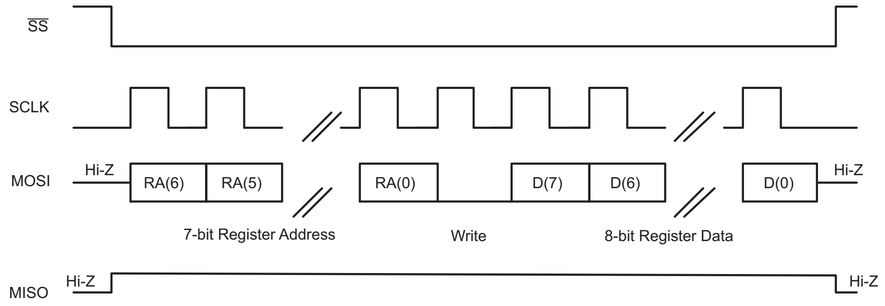


Figure 8-71. SPI Single-Byte Write Transfer

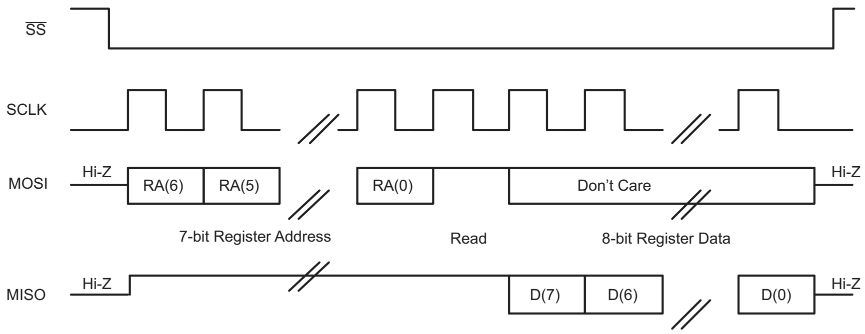


Figure 8-72. SPI Single-Byte Read Transfer

8.6 Register Maps

This section describes the control registers for the device in detail. All registers are eight bits in width and are allocated to the device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using either I^2C or SPI communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). Page 1 consists of the live status registers and input diagnostic SAR data for advanced diagnostic purposes. All programmable coefficient registers are located in page 2, page 3, and page 4. The device current page can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

8.6.1 Device Configuration Registers

This section describes the device configuration registers for page 0 and page 1.

8.6.1.1 Registers Access Type

Table 8-51 lists the access codes used for the PCM6xx0-Q1 registers.

Table 8-51. PCM6xx0-Q1 Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.2 Page 0 Registers

Table 8-52 lists the memory-mapped registers for the Page 0 registers. All register offset addresses not listed in Table 8-52 should be considered as reserved locations and the register contents should not be modified.

Table 8-52. PAGE 0 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 8.6.1.2.1
0x1	SW_RESET	Software reset register	0x00	Section 8.6.1.2.2
0x2	SLEEP_CFG	Sleep mode register	0x00	Section 8.6.1.2.3
0x5	SHDN_CFG	Shutdown configuration register	0x05	Section 8.6.1.2.4
0x7	ASI_CFG0	ASI configuration register 0	0x30	Section 8.6.1.2.5
0x8	ASI_CFG1	ASI configuration register 1	0x00	Section 8.6.1.2.6
0x9	ASI_CFG2	ASI configuration register 2	0x00	Section 8.6.1.2.7
0xB	ASI_CH1	Channel 1 ASI slot configuration register	0x00	Section 8.6.1.2.8
0xC	ASI_CH2	Channel 2 ASI slot configuration register	0x01	Section 8.6.1.2.9
0x13	MST_CFG0	ASI master mode configuration register 0	0x02	Section 8.6.1.2.10
0x14	MST_CFG1	ASI master mode configuration register 1	0x48	Section 8.6.1.2.11
0x15	ASI_STS	ASI bus clock monitor status register	0xFF	Section 8.6.1.2.12
0x16	CLK_SRC	Clock source configuration register	0x10	Section 8.6.1.2.13
0x21	GPIO_CFG0	GPIO configuration register 0	0x22	Section 8.6.1.2.14
0x22	GPIO_CFG1	GPIO configuration register 1	0x00	Section 8.6.1.2.15
0x23	GPIO_CFG2	GPIO configuration register 2	0x00	Section 8.6.1.2.16
0x24	GPI_CFG0	GPI configuration register 0	0x00	Section 8.6.1.2.17
0x25	GPI_CFG1	GPI configuration register 1	0x00	Section 8.6.1.2.18
0x26	GPIO_VAL	GPIO output value register	0x00	Section 8.6.1.2.19
0x27	GPIO_MON	GPIO monitor value register	0x00	Section 8.6.1.2.20
0x28	INT_CFG	Interrupt configuration register	0x00	Section 8.6.1.2.21
0x29	INT_MASK0	Interrupt mask register 0	0xFF	Section 8.6.1.2.22
0x2A	INT_MASK1	Interrupt mask register 1	0x03	Section 8.6.1.2.23
0x2B	INT_MASK2	Interrupt mask register 2	0x00	Section 8.6.1.2.24
0x2C	INT_LTCH0	Latched interrupt readback register 0	0x00	Section 8.6.1.2.25
0x2D	CHx_LTCH	Channel diagnostic summary latched status register	0x00	Section 8.6.1.2.26
0x2E	CH1_LTCH	Channel 1 diagnostic latched status register	0x00	Section 8.6.1.2.27
0x2F	CH2_LTCH	Channel 2 diagnostic latched status register	0x00	Section 8.6.1.2.28
0x34	INT_MASK3	Interrupt mask register 3	0x00	Section 8.6.1.2.29
0x35	INT_LTCH1	Latched interrupt readback register 1	0x00	Section 8.6.1.2.30
0x36	INT_LTCH2	Latched interrupt readback register 2	0x00	Section 8.6.1.2.31
0x37	INT_LTCH3	Latched interrupt readback register 3	0x00	Section 8.6.1.2.32
0x38	MBDIAG_CFG0	MICBIAS diagnostic register 0	0xBA	Section 8.6.1.2.33
0x39	MBDIAG_CFG1	MICBIAS diagnostic register 1	0x4B	Section 8.6.1.2.34
0x3A	MBDIAG_CFG2	MICBIAS diagnostic register 2	0x10	Section 8.6.1.2.35
0x3B	BIAS_CFG	Bias configuration register	0xD0	Section 8.6.1.2.36
0x3C	CH1_CFG0	Channel 1 configuration register 0	0x10	Section 8.6.1.2.37
0x3D	CH1_CFG1	Channel 1 configuration register 1	0x00	Section 8.6.1.2.38
0x3E	CH1_CFG2	Channel 1 configuration register 2	0xC9	Section 8.6.1.2.39
0x3F	CH1_CFG3	Channel 1 configuration register 3	0x80	Section 8.6.1.2.40
0x40	CH1_CFG4	Channel 1 configuration register 4	0x00	Section 8.6.1.2.41
0x41	CH2_CFG0	Channel 2 configuration register 0	0x10	Section 8.6.1.2.42

Table 8-52. PAGE 0 Registers (continued)

Address	Acronym	Register Name	Reset Value	Section
0x42	CH2_CFG1	Channel 2 configuration register 1	0x00	Section 8.6.1.2.43
0x43	CH2_CFG2	Channel 2 configuration register 2	0xC9	Section 8.6.1.2.44
0x44	CH2_CFG3	Channel 2 configuration register 3	0x80	Section 8.6.1.2.45
0x45	CH2_CFG4	Channel 2 configuration register 4	0x00	Section 8.6.1.2.46
0x64	DIAG_CFG0	Input diagnostic configuration register 0	0x00	Section 8.6.1.2.47
0x65	DIAG_CFG1	Input diagnostic configuration register 1	0x37	Section 8.6.1.2.48
0x66	DIAG_CFG2	Input diagnostic configuration register 2	0x87	Section 8.6.1.2.49
0x67	DIAG_CFG3	Input diagnostic configuration register 3	0xB8	Section 8.6.1.2.50
0x68	DIAG_CFG4	Input diagnostic configuration register 4	0x00	Section 8.6.1.2.51
0x6A	BOOST_CFG	Boost configuration register	0x00	Section 8.6.1.2.52
0x6B	DSP_CFG0	DSP configuration register 0	0x01	Section 8.6.1.2.53
0x6C	DSP_CFG1	DSP configuration register 1	0x48	Section 8.6.1.2.54
0x70	AGC_CFG0	AGC configuration register 0	0xE7	Section 8.6.1.2.55
0x73	IN_CH_EN	Input channel enable configuration register	0xFC	Section 8.6.1.2.56
0x74	ASI_OUT_CH_EN	ASI output channel enable configuration register	0x00	Section 8.6.1.2.57
0x75	PWR_CFG	Power up configuration register	0x00	Section 8.6.1.2.58
0x76	DEV_STS0	Device status value register 0	0x00	Section 8.6.1.2.59
0x77	DEV_STS1	Device status value register 1	0x80	Section 8.6.1.2.60
0x7E	I2C_CKSUM	I^{2}C Checksum	0x00	Section 8.6.1.2.61

8.6.1.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x0]

PAGE_CFG is shown in Figure 8-73 and described in Table 8-53.

Return to the Table 8-52.

The device memory map is divided into pages. This register sets the page.

Figure 8-73. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

Table 8-53. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 … 255d = Page 255

8.6.1.2.2 SW_RESET Register (Address = 0x1) [Reset = 0x0]

SW_RESET is shown in Figure 8-74 and described in Table 8-54.

Return to the Table 8-52.

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

Figure 8-74. SW_RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R-0000000b							R/W-0b

Table 8-54. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits; Write only reset value
0	SW_RESET	R/W	0b	Software reset. This bit is self-clearing. 0d = Do not reset 1d = Reset

8.6.1.2.3 SLEEP_CFG Register (Address = 0x2) [Reset = 0x0]

SLEEP_CFG is shown in Figure 8-75 and described in Table 8-55.

Return to the Table 8-52.

This register configures the regulator, VREF quick charge, I^{2}C broadcast and sleep mode.

Figure 8-75. SLEEP_CFG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		VREF_QCHG[1:0]		I2C_BRDCAST_EN	RESERVED	SLEEP_ENZ
R/W-0b	R/W-00b		R/W-00b		R/W-0b	R-0b	R/W-0b

Table 8-55. SLEEP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6-5	RESERVED	R/W	00b	Reserved bits; Write only reset values
4-3	VREF_QCHG[1:0]	R/W	00b	The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)
2	I2C_BRDCAST_EN	R/W	0b	I^{2}C broadcast addressing setting. 0d = I^{2}C broadcast mode disabled; the I^{2}C slave address is determined based on the ADDR pins 1d = I^{2}C broadcast mode enabled; the I^{2}C slave address is fixed at 1001 100
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	SLEEP_ENZ	R/W	0b	Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode

8.6.1.2.4 SHDN_CFG Register (Address = 0x5) [Reset = 0x5]

SHDN_CFG is shown in Figure 8-76 and described in Table 8-56.

Return to the Table 8-52.

This register configures the device shutdown

Figure 8-76. SHDN_CFG Register

7	6	5	4	3	2	1	0
RESERVED				SHDNZ_CFG[1:0]		DREG_KA_TIME[1:0]	

Figure 8-76. SHDN_CFG Register (continued)

R-0000b	R/W-01b	R/W-01b

Table 8-56. SHDN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved bits; Write only reset value
3-2	SHDNZ_CFG[1:0]	R/W	01b	Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved
1-0	DREG_KA_TIME[1:0]	R/W	01b	These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical)

8.6.1.2.5 ASI_CFG0 Register (Address = 0x7) [Reset = 0x30]

ASI_CFG0 is shown in Figure 8-77 and described in Table 8-57.

Return to the Table 8-52.

This register is the ASI configuration register 0.

Figure 8-77. ASI_CFG0 Register

7	6	5	4	3	2	1	0
ASI_FORMAT[1:0]		ASI_WLEN[1:0]		FSYNC_POL	BCLK_POL	TX_EDGE	TX_FILL
R/W-00b		R/W-11b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-57. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_FORMAT[1:0]	R/W	00b	ASI protocol format. 0d = TDM mode 1d = I^{2}S mode 2d = LJ (left-justified) mode 3d = Reserved
5-4	ASI_WLEN[1:0]	R/W	11b	ASI word or slot length. 0d = 16 bits 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	FSYNC_POL	R/W	0b	ASI FSYNC polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	BCLK_POL	R/W	0b	ASI BCLK polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	TX_EDGE	R/W	0b	ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting

Table 8-57. ASI_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_FILL	R/W	0b	ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles

8.6.1.2.6 ASI_CFG1 Register (Address = 0x8) [Reset = 0x0]

ASI_CFG1 is shown in Figure 8-78 and described in Table 8-58.

Return to the Table 8-52.

This register is the ASI configuration register 1.

Figure 8-78. ASI_CFG1 Register

7	6	5	4	3	2	1	0
TX_LSB	TX_KEEPER[1:0]		TX_OFFSET[4:0]				
R/W-0b	R/W-00b		R/W-00000b				

Table 8-58. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_LSB	R/W	0b	ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
6-5	TX_KEEPER[1:0]	R/W	00b	ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles
4-0	TX_OFFSET[4:0]	R/W	00000b	ASI data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

8.6.1.2.7 ASI_CFG2 Register (Address = 0x9) [Reset = 0x0]

ASI_CFG2 is shown in Figure 8-79 and described in Table 8-59.

Return to the Table 8-52.

This register is the ASI configuration register 2.

Figure 8-79. ASI_CFG2 Register

7	6	5	4	3	2	1	0

Figure 8-79. ASI_CFG2 Register (continued)

ASI_DAISY	RESERVED	ASI_ERR	ASI_ERR_RCOV	RESERVED
R/W-0b	R-0b	R/W-0b	R/W-0b	R-0000b

Table 8-59. ASI_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_DAISY	R/W	0b	ASI daisy chain connection. 0d = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus
6	RESERVED	R	0b	Reserved bit; Write only reset value
5	ASI_ERR	R/W	0b	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
4	ASI_ERR_RCOV	R/W	0b	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.1.2.8 ASI_CH1 Register (Address = 0xB) [Reset = 0x0]

ASI_CH1 is shown in Figure 8-80 and described in Table 8-60.

Return to the Table 8-52.

This register is the ASI slot configuration register for channel 1.

Figure 8-80. ASI_CH1 Register

7	6	5	4	3	2	1	0
RESERVED	CH1_OUTPUT	CH1_SLOT[5:0]					
R-0b	R/W-0b	R/W-000000b					

Table 8-60. ASI_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6	CH1_OUTPUT	R/W	0b	Channel 1 output line. 0d = Channel 1 output is on the ASI primary output pin (SDOUT) 1d = Channel 1 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH1_SLOT[5:0]	R/W	000000b	Channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.1.2.9 ASI_CH2 Register (Address = 0xC) [Reset = 0x1]

ASI_CH2 is shown in Figure 8-81 and described in Table 8-61.

Return to the Table 8-52.

This register is the ASI slot configuration register for channel 2.

Figure 8-81. ASI_CH2 Register

7	6	5	4	3	2	1	0
RESERVED	CH2_OUTPUT	CH2_SLOT[5:0]					
R-0b	R/W-0b	R/W-000001b					

Table 8-61. ASI_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6	CH2_OUTPUT	R/W	0b	Channel 2 output line. 0d = Channel 2 output is on the ASI primary output pin (SDOUT) 1d = Channel 2 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH2_SLOT[5:0]	R/W	000001b	Channel 2 slot assignment. 0d = TDM is slot 0 or I^{2}S, LJ is left slot 0 1d = TDM is slot 1 or I^{2}S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^{2}S, LJ is left slot 31 32d = TDM is slot 32 or I^{2}S, LJ is right slot 0 33d = TDM is slot 33 or I^{2}S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^{2}S, LJ is right slot 31

8.6.1.2.10 MST_CFG0 Register (Address = 0x13) [Reset = 0x2]

MST_CFG0 is shown in Figure 8-82 and described in Table 8-62.

Return to the Table 8-52.

This register is the ASI master mode configuration register 0.

Figure 8-82. MST_CFG0 Register

7	6	5	4	3	2	1	0
MST_SLV_CFG	AUTO_CLK_CFG	AUTO_MODE_PLL_DIS	BCLK_FSYNC_GATE	FS_MODE	MCLK_FREQ_SEL[2:0]		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-010b		

Table 8-62. MST_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MST_SLV_CFG	R/W	0b	ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device) 1d = Device is in master mode (both BCLK and FSYNC are generated from the device)
6	AUTO_CLK_CFG	R/W	0b	Automatic clock configuration setting. 0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived) 1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings)
5	AUTO_MODE_PLL_DIS	R/W	0b	Automatic mode PLL setting. 0d = PLL is enabled in auto clock configuration 1d = PLL is disabled in auto clock configuration
4	BCLK_FSYNC_GATE	R/W	0b	BCLK and FSYNC clock gate (valid when the device is in master mode). 0d = Do not gate BCLK and FSYNC 1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode
3	FS_MODE	R/W	0b	Sample rate setting (valid when the device is in master mode). 0d = f_S is a multiple (or submultiple) of 48 kHz 1d = f_S is a multiple (or submultiple) of 44.1 kHz

Table 8-62. MST_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MCLK_FREQ_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz

8.6.1.2.11 MST_CFG1 Register (Address = 0x14) [Reset = 0x48]

MST_CFG1 is shown in Figure 8-83 and described in Table 8-63.

Return to the Table 8-52.

This register is the ASI master mode configuration register 1.

Figure 8-83. MST_CFG1 Register

7	6	5	4	3	2	1	0
FS_RATE[3:0]				FS_BCLK_RATIO[3:0]			
R/W-0100b				R/W-1000b			

Table 8-63. MST_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE[3:0]	R/W	0100b	Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 15d = Reserved
3-0	FS_BCLK_RATIO[3:0]	R/W	1000b	Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d = Reserved 14d = Reserved 15d = Reserved

8.6.1.2.12 ASI_STS Register (Address = 0x15) [Reset = 0xFF]

ASI_STS is shown in Figure 8-84 and described in Table 8-64.

Return to the Table 8-52.

This register s the ASI bus clock monitor status register

Figure 8-84. ASI_STS Register

7	6	5	4	3	2	1	0
FS_RATE_STS[3:0]				FS_RATIO_STS[3:0]			
R-1111b				R-1111b			

Table 8-64. ASI_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE_STS[3:0]	R	1111b	Detected sample rate of the ASI bus. 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 14d = Reserved 15d = Invalid sample rate
3-0	FS_RATIO_STS[3:0]	R	1111b	Detected BCLK to FSYNC frequency ratio of the ASI bus. 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d = Reserved 14d = Reserved 15d = Invalid ratio

8.6.1.2.13 CLK_SRC Register (Address = 0x16) [Reset = 0x10]

CLK_SRC is shown in Figure 8-85 and described in Table 8-65.

Return to the Table 8-52.

This register is the clock source configuration register.

Figure 8-85. CLK_SRC Register

7	6	5	4	3	2	1	0
DIS_PLL_SLV_CLK_SRC	MCLK_FREQ_SEL_MODE	MCLK_RATIO_SEL[2:0]			RESERVED		
R/W-0b	R/W-0b	R/W-010b			R-000b		

Table 8-65. CLK_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_PLL_SLV_CLK_SRC	R/W	0b	Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1). 0d = BCLK is used as the audio root clock source 1d = MCLK (GPIOx or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting)
6	MCLK_FREQ_SEL_MODE	R/W	0b	Master mode MCLK (GPIOx or GPIx) frequency selection mode (valid when the device is in auto clock configuration). 0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R19) configuration 1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R22) configuration
5-3	MCLK_RATIO_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIOx or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode. 0d = Ratio of 64 1d = Ratio of 256 2d = Ratio of 384 3d = Ratio of 512 4d = Ratio of 768 5d = Ratio of 1024 6d = Ratio of 1536 7d = Ratio of 2304
2-0	RESERVED	R	000b	Reserved bits; Write only reset values

8.6.1.2.14 GPIO_CFG0 Register (Address = 0x21) [Reset = 0x22]

GPIO_CFG0 is shown in Figure 8-86 and described in Table 8-66.

Return to the Table 8-52.

This register is the GPIO configuration register 0.

Figure 8-86. GPIO_CFG0 Register

7	6	5	4	3	2	1	0
GPIO1_CFG[3:0]				RESERVED	GPIO1_DRV[2:0]		
R/W-0010b				R-0b	R/W-010b		

Table 8-66. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	R/W	0010b	GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = GPIO1 is configured as a secondary ASI output (SDOUT2) Dont use 5d = Reserved 6d = Reserved 7d = GPIO1 is configured as an input to power down all ADC channels 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Dont use Dont use
3	RESERVED	R	0b	Reserved bit; Write only reset value

Table 8-66. GPIO_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	GPIO1_DRV[2:0]	R/W	010b	GPIO1 output drive configuration (not used when GPIO1 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.2.15 GPIO_CFG1 Register (Address = 0x22) [Reset = 0x0]

GPIO_CFG1 is shown in Figure 8-87 and described in Table 8-67.

Return to the Table 8-52.

This register is the GPIO configuration register 1.

Figure 8-87. GPIO_CFG1 Register

7	6	5	4	3	2	1	0
GPIO2_CFG[3:0]				RESERVED	GPIO2_DRV[2:0]		
R/W-0000b				R-0b	R/W-000b		

Table 8-67. GPIO_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO2_CFG[3:0]	R/W	0000b	GPIO2 configuration. 0d = GPIO2 is disabled 1d = GPIO2 is configured as a general-purpose output (GPO) 2d = GPIO2 is configured as a device interrupt output (IRQ) 3d = GPIO2 is configured as a secondary ASI output (SDOUT2) Dont use 5d = Reserved 6d = Reserved 7d = GPIO2 is configured as an input to power down all ADC channels 8d = GPIO2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO2 is configured as a general-purpose input (GPI) 10d = GPIO2 is configured as a master clock input (MCLK) 11d = GPIO2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Dont use Dont use
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPIO2_DRV[2:0]	R/W	000b	GPIO2 output drive configuration (not used when GPIO2 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.2.16 GPIO_CFG2 Register (Address = 0x23) [Reset = 0x0]

GPIO_CFG2 is shown in Figure 8-88 and described in Table 8-68.

Return to the Table 8-52.

This register is the GPIO configuration register 2.

Figure 8-88. GPIO_CFG2 Register

7	6	5	4	3	2	1	0
GPIO3_CFG[3:0]				RESERVED	GPIO3_DRV[2:0]		
R/W-0000b				R-0b	R/W-000b		

Table 8-68. GPIO_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO3_CFG[3:0]	R/W	0000b	GPIO3 configuration. 0d = GPIO3 is disabled 1d = GPIO3 is configured as a general-purpose output (GPO) 2d = GPIO3 is configured as a device interrupt output (IRQ) 3d = GPIO3 is configured as a secondary ASI output (SDOUT2) Dont use 5d = Reserved 6d = Reserved 7d = GPIO3 is configured as an input to power down all ADC channels 8d = GPIO3 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO3 is configured as a general-purpose input (GPI) 10d = GPIO3 is configured as a master clock input (MCLK) 11d = GPIO3 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Dont use Dont use
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPIO3_DRV[2:0]	R/W	000b	GPIO3 output drive configuration (not used when GPIO3 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

8.6.1.2.17 GPI_CFG0 Register (Address = 0x24) [Reset = 0x0]

GPI_CFG0 is shown in Figure 8-89 and described in Table 8-69.

Return to the Table 8-52.

This register is the GPI configuration register 0.

Figure 8-89. GPI_CFG0 Register

7	6	5	4	3	2	1	0
GPI1_CFG[3:0]				RESERVED			
R/W-0000b				R-0000b			

Table 8-69. GPI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPI1_CFG[3:0]	R/W	0000b	GPI1 configuration. 0d = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Dont use Dont use
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.1.2.18 GPI_CFG1 Register (Address = 0x25) [Reset = 0x0]

GPI_CFG1 is shown in Figure 8-90 and described in Table 8-70.

Return to the Table 8-52.

This register is the GPI configuration register 1.

Figure 8-90. GPI_CFG1 Register

7	6	5	4	3	2	1	0
GPI2_CFG[3:0]				RESERVED			
R/W-0000b				R-0000b			

Table 8-70. GPI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPI2_CFG[3:0]	R/W	0000b	GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Dont use Dont use
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.1.2.19 GPIO_VAL Register (Address = 0x26) [Reset = 0x0]

GPIO_VAL is shown in Figure 8-91 and described in Table 8-71.

Return to the Table 8-52.

This register is the GPIO output value register.

Figure 8-91. GPIO_VAL Register

7	6	5	4	3	2	1	0
GPIO1_VAL	GPIO2_VAL	GPIO3_VAL	RESERVED				
R/W-0b	R/W-0b	R/W-0b	R-00000b				

Table 8-71. GPIO_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_VAL	R/W	0b	GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
6	GPIO2_VAL	R/W	0b	GPIO2 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
5	GPIO3_VAL	R/W	0b	GPIO3 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.1.2.20 GPIO_MON Register (Address = 0x27) [Reset = 0x0]

GPIO_MON is shown in Figure 8-92 and described in Table 8-72.

Return to the Table 8-52.

This register is the GPIO monitor value register.

Figure 8-92. GPIO_MON Register

7	6	5	4	3	2	1	0
GPIO1_MON	GPIO2_MON	GPIO3_MON	GPI1_MON	GPI2_MON	RESERVED		
R-0b	R-0b	R-0b	R-0b	R-0b	R-000b		

Table 8-72. GPIO_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_MON	R	0b	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6	GPIO2_MON	R	0b	GPIO2 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
5	GPIO3_MON	R	0b	GPIO3 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
4	GPI1_MON	R	0b	GPI1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
3	GPI2_MON	R	0b	GPI2 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
2-0	RESERVED	R	000b	Reserved bits; Write only reset value

8.6.1.2.21 INT_CFG Register (Address = 0x28) [Reset = 0x0]

INT_CFG is shown in Figure 8-93 and described in Table 8-73.

Return to the Table 8-52.

This regiser is the interrupt configuration register.

Figure 8-93. INT_CFG Register

7	6	5	4	3	2	1	0
INT_POL	INT_EVENT[1:0]		PD_ON_FLT_CFG[1:0]		LTCH_READ_CFG	PD_ON_FLT_RCV_CFG	LTCH_CLR_ON_READ

Figure 8-93. INT_CFG Register (continued)

R/W-0b	R/W-00b	R/W-00b	R/W-0b	R/W-0b	R/W-0b

Table 8-73. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	R/W	0b	Interrupt polarity. 0d = Active low (IRQZ) 1d = Active high (IRQ)
6-5	INT_EVENT[1:0]	R/W	00b	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event Dont use 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	PD_ON_FLT_CFG[1:0]	R/W	00b	Powerdown configuration when fault detected for any channel or MICBIAS fault detected. 0d = Faults event are not used for ADC and MICBIAS power down. It is recommend to set these bits as 2d to shutdown the blocks for which fault occurred. 1d = Only unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings 2d = Both masked or unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings. 3d = Reserved
2	LTCH_READ_CFG	R/W	0b	Interrupt latch registers readback configuration. 0d = All interrupts can be read through the LTCH registers 1d = Only unmasked interrupts can be read through the LTCH registers
1	PD_ON_FLT_RCV_CFG	R/W	0b	Recovery configuration for ADC channels when fault goes away. 0d = Auto recovery, ADC channels are re-powered up when fault goes away 1d = Manual recovery, ADC channels are required to power-up manually using P0_R119 when fault goes away
0	LTCH_CLR_ON_READ	R/W	0b	Configuration for clearing LTCH register bits. 0d = LTCH register bits are cleared on register read only if live status is zero 1d = LTCH register bits are cleared on register read irrespective of live status and set only if live status goes again low to high

8.6.1.2.22 INT_MASK0 Register (Address = 0x29) [Reset = 0xFF]

INT_MASK0 is shown in Figure 8-94 and described in Table 8-74.

Return to the Table 8-52.

This register is the interrupt masks register 0.

Figure 8-94. INT_MASK0 Register

7	6	5	4	3	2	1	0
INT_MASK0	INT_MASK0	INT_MASK0	INT_MASK0	RESERVED	RESERVED	RESERVED	RESERVED
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-74. INT_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0	R/W	1b	ASI clock error mask. 0d = Unmask 1d = Mask
6	INT_MASK0	R/W	1b	PLL lock interrupt mask. 0d = Unmask 1d = Mask
5	INT_MASK0	R/W	1b	Boost or MICBIAS over temperature interrupt mask. 0d = Unmask 1d = Mask
4	INT_MASK0	R/W	1b	Boost or MICBIAS over current interrupt mask. 0d = Unmask 1d = Mask
3	RESERVED	R/W	1b	Reserved bit; Write only reset value
2	RESERVED	R/W	1b	Reserved bit; Write only reset value
1	RESERVED	R/W	1b	Reserved bit; Write only reset value
0	RESERVED	R/W	1b	Reserved bit; Write only reset value

8.6.1.2.23 INT_MASK1 Register (Address = 0x2A) [Reset = 0x3]

INT_MASK1 is shown in Figure 8-95 and described in Table 8-75.

Return to the Table 8-52.

This register is the interrupt masks register 1.

Figure 8-95. INT_MASK1 Register

7	6	5	4	3	2	1	0
INT_MASK1	INT_MASK1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b

Table 8-75. INT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK1	R/W	0b	Channel 1 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
6	INT_MASK1	R/W	0b	Channel 2 input DC faults diagnostic interrupt mask. 0d = Unmask 1d = Mask
5	RESERVED	R/W	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	RESERVED	R/W	1b	Reserved bit; Write only reset value
0	RESERVED	R/W	1b	Reserved bit; Write only reset value

8.6.1.2.24 INT_MASK2 Register (Address = 0x2B) [Reset = 0x0]

INT_MASK2 is shown in Figure 8-96 and described in Table 8-76.

Return to the Table 8-52.

This register is the interrupt masks register 2.

Figure 8-96. INT_MASK2 Register

7	6	5	4	3	2	1	0
INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-76. INT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2	R/W	0b	Input diagnostics; Open inputs fault interrupt mask. 0d = Unmask 1d = Mask
6	INT_MASK2	R/W	0b	Input diagnostics; Inputs shorted fault interrupt mask. 0d = Unmask 1d = Mask
5	INT_MASK2	R/W	0b	Input diagnostics; INxP shorted to ground fault interrupt mask. 0d = Unmask 1d = Mask
4	INT_MASK2	R/W	0b	Input diagnostics; INxM shorted to ground fault interrupt mask. 0d = Unmask 1d = Mask
3	INT_MASK2	R/W	0b	Input diagnostics; INxP shorted to MICBIAS fault interrupt mask. 0d = Unmask 1d = Mask
2	INT_MASK2	R/W	0b	Input diagnostics; INxM shorted to MICBIAS fault interrupt mask. 0d = Unmask 1d = Mask
1	INT_MASK2	R/W	0b	Input diagnostics; INxP shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask
0	INT_MASK2	R/W	0b	Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask

8.6.1.2.25 INT_LTCH0 Register (Address = 0x2C) [Reset = 0x0]

INT_LTCH0 is shown in Figure 8-97 and described in Table 8-77.

Return to the Table 8-52.

This register is the latched Interrupt readback register 0.

Figure 8-97. INT_LTCH0 Register

7	6	5	4	3	2	1	0
INT_LTCH0	INT_LTCH0	INT_LTCH0	INT_LTCH0	RESERVED	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-77. INT_LTCH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0	R	0b	Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected
6	INT_LTCH0	R	0b	Status of PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected
5	INT_LTCH0	R	0b	Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected

Table 8-77. INT_LTCH0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_LTCH0	R	0b	Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected 1d = Fault detected
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.26 CHx_LTCH Register (Address = 0x2D) [Reset = 0x0]

CHx_LTCH is shown in Figure 8-98 and described in Table 8-78.

Return to the Table 8-52.

This register is the latched Interrupt status register for channel level diagnostic summary.

Figure 8-98. CHx_LTCH Register

7	6	5	4	3	2	1	0
STS_CHx_LTCH	STS_CHx_LTCH	RESERVED	RESERVED	RESERVED	RESERVED	STS_CHx_LTCH	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-78. CHx_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LTCH	R	0b	Status of CH1_LTCH (self-clearing bit). 0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1
6	STS_CHx_LTCH	R	0b	Status of CH2_LTCH (self-clearing bit). 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	STS_CHx_LTCH	R	0b	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS (self-clearing bit). 0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.27 CH1_LTCH Register (Address = 0x2E) [Reset = 0x0]

CH1_LTCH is shown in Figure 8-99 and described in Table 8-79.

Return to the Table 8-52.

This register is the latched Interrupt status register for channel 1 fault diagnostic

Figure 8-99. CH1_LTCH Register

7	6	5	4	3	2	1	0
CH1_LTCH	CH1_LTCH	CH1_LTCH	CH1_LTCH	CH1_LTCH	CH1_LTCH	CH1_LTCH	CH1_LTCH
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 8-99. CH1_LTCH Register (continued)

Table 8-79. CH1_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_LTCH	R	0b	Channel 1 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH1_LTCH	R	0b	Channel 1 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH1_LTCH	R	0b	Channel 1 IN1P short to ground fault status (self-clearing bit). 0d = IN1P no short to ground detected 1d = IN1P short to ground detected
4	CH1_LTCH	R	0b	Channel 1 IN1M short to ground fault status (self-clearing bit). 0d = IN1M no short to ground detected 1d = IN1M short to ground detected
3	CH1_LTCH	R	0b	Channel 1 IN1P short to MICBIAS fault status (self-clearing bit). 0d = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected
2	CH1_LTCH	R	0b	Channel 1 IN1M short to MICBIAS fault status (self-clearing bit). 0d = IN1M no short to MICBIAS detected 1d = IN1M short to MICBIAS detected
1	CH1_LTCH	R	0b	Channel 1 IN1P short to VBAT_IN fault status (self-clearing bit). 0d = IN1P no short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected
0	CH1_LTCH	R	0b	Channel 1 IN1M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected

8.6.1.2.28 CH2_LTCH Register (Address = 0x2F) [Reset = 0x0]

CH2_LTCH is shown in Figure 8-100 and described in Table 8-80.

Return to the Table 8-52.

This register is the latched Interrupt status register for channel 2 fault diagnostic.

Figure 8-100. CH2_LTCH Register

7	6	5	4	3	2	1	0
CH2_LTCH	CH2_LTCH	CH2_LTCH	CH2_LTCH	CH2_LTCH	CH2_LTCH	CH2_LTCH	CH2_LTCH
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-80. CH2_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_LTCH	R	0b	Channel 2 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected
6	CH2_LTCH	R	0b	Channel 2 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected
5	CH2_LTCH	R	0b	Channel 2 IN2P short to ground fault status (self-clearing bit). 0d = IN2P no short to ground detected 1d = IN2P short to ground detected
4	CH2_LTCH	R	0b	Channel 2 IN2M short to ground fault status (self-clearing bit). 0d = IN2M no short to ground detected 1d = IN2M short to ground detected

Table 8-80. CH2_LTCH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH2_LTCH	R	0b	Channel 2 IN2P short to MICBIAS fault status (self-clearing bit). 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected
2	CH2_LTCH	R	0b	Channel 2 IN2M short to MICBIAS fault status (self-clearing bit). 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected
1	CH2_LTCH	R	0b	Channel 2 IN2P short to VBAT_IN fault status (self-clearing bit). 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected
0	CH2_LTCH	R	0b	Channel 2 IN2M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected

8.6.1.2.29 INT_MASK3 Register (Address = 0x34) [Reset = 0x0]

INT_MASK3 is shown in Figure 8-101 and described in Table 8-81.

Return to the Table 8-52.

This register is the interrupt masks register 3.

Figure 8-101. INT_MASK3 Register

7	6	5	4	3	2	1	0
INT_MASK3	INT_MASK3	INT_MASK3	INT_MASK3	INT_MASK3	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-000b		

Table 8-81. INT_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK3	R/W	0b	INxP over voltage fault mask. 0d = Unmask 1d = Mask
6	INT_MASK3	R/W	0b	INxM over voltage fault mask. 0d = Unmask 1d = Mask
5	INT_MASK3	R/W	0b	MICBIAS high current fault mask. 0d = Unmask 1d = Mask
4	INT_MASK3	R/W	0b	MICBIAS low current fault mask. 0d = Unmask 1d = Mask
3	INT_MASK3	R/W	0b	MICBIAS over voltage fault mask. 0d = Unmask 1d = Mask
2-0	RESERVED	R	000b	Reserved bits; Write only reset value

8.6.1.2.30 INT_LTCH1 Register (Address = 0x35) [Reset = 0x0]

INT_LTCH1 is shown in Figure 8-102 and described in Table 8-82.

Return to the Table 8-52.

This register is the latched Interrupt readback register 1.

Figure 8-102. INT_LTCH1 Register

7	6	5	4	3	2	1	0

Figure 8-102. INT_LTCH1 Register (continued)

INT_LTCH1	INT_LTCH1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b

Table 8-82. INT_LTCH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH1	R	0b	Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected
6	INT_LTCH1	R	0b	Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault has detected
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

8.6.1.2.31 INT_LTCH2 Register (Address = 0x36) [Reset = 0x0]

INT_LTCH2 is shown in Figure 8-103 and described in Table 8-83.

Return to the Table 8-52.

This register is the latched Interrupt readback register 2.

Figure 8-103. INT_LTCH2 Register

7	6	5	4	3	2	1	0
INT_LTCH2	INT_LTCH2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

Table 8-83. INT_LTCH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2	R	0b	Channel 1 IN1M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1M over voltage fault detected 1d = IN1M over voltage fault has detected
6	INT_LTCH2	R	0b	Channel 2 IN2M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2M over voltage fault detected 1d = IN2M over voltage fault has detected
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

8.6.1.2.32 INT_LTCH3 Register (Address = 0x37) [Reset = 0x0]

INT_LTCH3 is shown in Figure 8-104 and described in Table 8-84.

Return to the Table 8-52.

This register is the latched Interrupt readback register 3.

Figure 8-104. INT_LTCH3 Register

7	6	5	4	3	2	1	0
INT_LTCH3	INT_LTCH3	INT_LTCH3	RESERVED				
R-0b	R-0b	R-0b	R-00000b				

Table 8-84. INT_LTCH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH3	R	0b	Fault status for MICBIAS high current (self-clearing bit). 0d = No fault detected 1d = Fault detected
6	INT_LTCH3	R	0b	Fault status for MICBIAS low current (self-clearing bit) 0d = No fault detected 1d = Fault detected
5	INT_LTCH3	R	0b	Fault status for MICBIAS over voltage (self-clearing bit). 0d = No fault detected 1d = Fault detected
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.1.2.33 MBDIAG_CFG0 Register (Address = 0x38) [Reset = 0xBA]

MBDIAG_CFG0 is shown in Figure 8-105 and described in Table 8-85.

Return to the Table 8-52.

This register is the MICBIAS diagnostic configuration register 0.

Figure 8-105. MBDIAG_CFG0 Register

7	6	5	4	3	2	1	0
MBIAS_HIGH_CURR_THRS[7:0]							
R/W-10111010b							

Table 8-85. MBDIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_HIGH_CURR_THRS[7:0]	R/W	10111010b	Threshold for MICBIAS high load current fault diagnostic. 0d to 56d = Reserved 57d = High load current threshold is set as 0 mA (typ) 58d = High load current threshold is set as 0.54 mA (typ) 59d = High load current threshold is set as 1.08 mA (typ) 60d to 185d = High load current threshold is set as per configuration 186d = High load current threshold is set as 69.66 mA (typ) 187d to 241d = High load current threshold is set as per configuration 242d = High load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

8.6.1.2.34 MBDIAG_CFG1 Register (Address = 0x39) [Reset = 0x4B]

MBDIAG_CFG1 is shown in Figure 8-106 and described in Table 8-86.

Return to the Table 8-52.

This register is the MICBIAS diagnostic configuration register 1.

Figure 8-106. MBDIAG_CFG1 Register

7	6	5	4	3	2	1	0
MBIAS_LOW_CURR_THRS[7:0]							

Figure 8-106. MBDIAG_CFG1 Register (continued)

R/W-01001011b

Table 8-86. MBDIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_LOW_CURR_THRS[7:0]	R/W	01001011b	Threshold for MICBIAS low load current fault diagnostic. 0d to 56d = Reserved 57d = Low load current threshold is set as 0 mA (typ) 58d = Low load current threshold is set as 0.54 mA (typ) 59d = Low load current threshold is set as 1.08 mA (typ) 60d to 74d = Low load current threshold is set as per configuration 75d = Low load current threshold is set as 9.72 mA (typ) 76d to 241d = Low load current threshold is set as per configuration 242d = Low load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

8.6.1.2.35 MBDIAG_CFG2 Register (Address = 0x3A) [Reset = 0x10]

MBDIAG_CFG2 is shown in Figure 8-107 and described in Table 8-87.

Return to the Table 8-52.

This register is the MICBIAS diagnostic configuration register 2.

Figure 8-107. MBDIAG_CFG2 Register

7	6	5	4	3	2	1	0
PD_MBIAS_FAULT1	PD_MBIAS_FAULT2	PD_MBIAS_FAULT3	PD_MBIAS_FAULT4	RESERVED	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R-000b		

Table 8-87. MBDIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PD_MBIAS_FAULT1	R/W	0b	Powerdown configuration of MICBIAS fault 1 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
6	PD_MBIAS_FAULT2	R/W	0b	Powerdown configuration of MICBIAS fault 2 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
5	PD_MBIAS_FAULT3	R/W	0b	Powerdown configuration of MICBIAS fault 3 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
4	PD_MBIAS_FAULT4	R/W	1b	Powerdown configuration of MICBIAS fault 4 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 2d. It is recommended to use this setting to protect chip from over temperature fault.
3	RESERVED	R/W	0b	Reserved bit; Write only reset value

Table 8-87. MBDIAG_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RESERVED	R	000b	Reserved bits; Write only reset value

8.6.1.2.36 BIAS_CFG Register (Address = 0x3B) [Reset = 0xD0]

BIAS_CFG is shown in Figure 8-108 and described in Table 8-88.

Return to the Table 8-52.

This register is the MICBIAS configuration register.

Figure 8-108. BIAS_CFG Register

7	6	5	4	3	2	1	0
MBIAS_VAL[3:0]				RESERVED		RESERVED	
R/W-1101b				R-00b		R/W-00b	

Table 8-88. BIAS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MBIAS_VAL[3:0]	R/W	1101b	MICBIAS value. Dont use Dont use Dont use Dont use Dont use Dont use Dont use 7d = Microphone bias is set to 5 V 8d = Microphone bias is set to 5.5 V 9d = Microphone bias is set to 6 V 10d = Microphone bias is set to 6.5 V 11d = Microphone bias is set to 7 V 12d = Microphone bias is set to 7.5 V 13d = Microphone bias is set to 8 V 14d = Microphone bias is set to 8.5 V 15d = Microphone bias is set to 9 V
3-2	RESERVED	R	00b	Reserved bits; Write only reset value
1-0	RESERVED	R/W	00b	Reserved bits; Write only reset values

8.6.1.2.37 CH1_CFG0 Register (Address = 0x3C) [Reset = 0x10]

CH1_CFG0 is shown in Figure 8-109 and described in Table 8-89.

Return to the Table 8-52.

This register is configuration register 0 for channel 1.

Figure 8-109. CH1_CFG0 Register

7	6	5	4	3	2	1	0
CH1_INTYP	CH1_INSRC[1:0]		CH1_DC	CH1_MIC_IN_RANGE	CH1_PGA_CFG[1:0]		CH1_AGCEN
R/W-0b	R/W-00b		R/W-1b	R/W-0b	R/W-00b		R/W-0b

Table 8-89. CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_INTYP	R/W	0b	Channel 1 input type. 0d = Microphone input 1d = Line input

Table 8-89. CH1_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	CH1_INSRC[1:0]	R/W	00b	Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH1_DC	R/W	1b	Channel 1 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH1_MIC_IN_RANGE	R/W	0b	Channel 1 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH1_PGA_CFG[1:0]	R/W	00b	Channel 1 CMRR Configuration. 0d = High SNR performance mode Dont use 2d = High CMRR performance mode 3d = Reserved
0	CH1_AGCEN	R/W	0b	Channel 1 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.2.38 CH1_CFG1 Register (Address = 0x3D) [Reset = 0x0]

CH1_CFG1 is shown in Figure 8-110 and described in Table 8-90.

Return to the Table 8-52.

This register is configuration register 1 for channel 1.

Figure 8-110. CH1_CFG1 Register

7	6	5	4	3	2	1	0
CH1_GAIN[5:0]						RESERVED	RESERVED
R/W-000000b						R/W-0b	R-0b

Table 8-90. CH1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH1_GAIN[5:0]	R/W	000000b	Channel 1 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.39 CH1_CFG2 Register (Address = 0x3E) [Reset = 0xC9]

CH1_CFG2 is shown in Figure 8-111 and described in Table 8-91.

Return to the Table 8-52.

This register is configuration register 2 for channel 1.

Figure 8-111. CH1_CFG2 Register

7	6	5	4	3	2	1	0
CH1_DVOL[7:0]							
R/W-11001001b							

Table 8-91. CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_DVOL[7:0]	R/W	11001001b	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.2.40 CH1_CFG3 Register (Address = 0x3F) [Reset = 0x80]

CH1_CFG3 is shown in Figure 8-112 and described in Table 8-92.

Return to the Table 8-52.

This register is configuration register 3 for channel 1.

Figure 8-112. CH1_CFG3 Register

7	6	5	4	3	2	1	0
CH1_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 8-92. CH1_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH1_GCAL[3:0]	R/W	1000b	Channel 1 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.1.2.41 CH1_CFG4 Register (Address = 0x40) [Reset = 0x0]

CH1_CFG4 is shown in Figure 8-113 and described in Table 8-93.

Return to the Table 8-52.

This register is configuration register 4 for channel 1.

Figure 8-113. CH1_CFG4 Register

7	6	5	4	3	2	1	0
CH1_PCAL[7:0]							
R/W-00000000b							

Figure 8-113. CH1_CFG4 Register (continued)

Table 8-93. CH1_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PCAL[7:0]	R/W	00000000b	Channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.2.42 CH2_CFG0 Register (Address = 0x41) [Reset = 0x10]

CH2_CFG0 is shown in Figure 8-114 and described in Table 8-94.

Return to the Table 8-52.

This register is configuration register 0 for channel 2.

Figure 8-114. CH2_CFG0 Register

7	6	5	4	3	2	1	0
CH2_INTYP	CH2_INSRC[1:0]		CH2_DC	CH2_MIC_IN_RANGE	CH2_PGA_CFG[1:0]		CH2_AGCEN
R/W-0b	R/W-00b		R/W-1b	R/W-0b	R/W-00b		R/W-0b

Table 8-94. CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_INTYP	R/W	0b	Channel 2 input type. 0d = Microphone input 1d = Line input
6-5	CH2_INSRC[1:0]	R/W	00b	Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved
4	CH2_DC	R/W	1b	Channel 2 input coupling. 0d = AC-coupled input 1d = DC-coupled input
3	CH2_MIC_IN_RANGE	R/W	0b	Channel 2 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.
2-1	CH2_PGA_CFG[1:0]	R/W	00b	Channel 2 CMRR Configuration. 0d = High SNR performance mode Dont use 2d = High CMRR performance mode 3d = Reserved
0	CH2_AGCEN	R/W	0b	Channel 2 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input

8.6.1.2.43 CH2_CFG1 Register (Address = 0x42) [Reset = 0x0]

CH2_CFG1 is shown in Figure 8-115 and described in Table 8-95.

Return to the Table 8-52.

This register is configuration register 1 for channel 2.

Figure 8-115. CH2_CFG1 Register

7	6	5	4	3	2	1	0
CH2_GAIN[5:0]						RESERVED	RESERVED
R/W-000000b						R/W-0b	R-0b

Table 8-95. CH2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CH2_GAIN[5:0]	R/W	000000b	Channel 2 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.44 CH2_CFG2 Register (Address = 0x43) [Reset = 0xC9]

CH2_CFG2 is shown in Figure 8-116 and described in Table 8-96.

Return to the Table 8-52.

This register is configuration register 2 for channel 2.

Figure 8-116. CH2_CFG2 Register

7	6	5	4	3	2	1	0
CH2_DVOL[7:0]							
R/W-11001001b							

Table 8-96. CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_DVOL[7:0]	R/W	11001001b	Channel 2 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.1.2.45 CH2_CFG3 Register (Address = 0x44) [Reset = 0x80]

CH2_CFG3 is shown in Figure 8-117 and described in Table 8-97.

Return to the Table 8-52.

This register is configuration register 3 for channel 2.

Figure 8-117. CH2_CFG3 Register

7	6	5	4	3	2	1	0
CH2_GCAL[3:0]				RESERVED			
R/W-1000b				R-0000b			

Table 8-97. CH2_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH2_GCAL[3:0]	R/W	1000b	Channel 2 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.1.2.46 CH2_CFG4 Register (Address = 0x45) [Reset = 0x0]

CH2_CFG4 is shown in Figure 8-118 and described in Table 8-98.

Return to the Table 8-52.

This register is configuration register 4 for channel 2.

Figure 8-118. CH2_CFG4 Register

7	6	5	4	3	2	1	0
CH2_PCAL[7:0]							
R/W-00000000b							

Table 8-98. CH2_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PCAL[7:0]	R/W	00000000b	Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.1.2.47 DIAG_CFG0 Register (Address = 0x64) [Reset = 0x0]

DIAG_CFG0 is shown in Figure 8-119 and described in Table 8-99.

Return to the Table 8-52.

This register is configuration register 0 for input fault diagnostics setting.

Figure 8-119. DIAG_CFG0 Register

7	6	5	4	3	2	1	0
CH1_DIAG_EN	CH2_DIAG_EN	RESERVED	RESERVED	RESERVED	RESERVED	INCL_SE_INM	INCL_AC_COUP
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-99. DIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_DIAG_EN	R/W	0b	Channel 1 input (IN1P and IN1M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
6	CH2_DIAG_EN	R/W	0b	Channel 2 input (IN2P and IN2M) scan for diagnostics. 0d = Diagnostic disabled 1d = Diagnostic enabled
5	RESERVED	R/W	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	INCL_SE_INM	R/W	0b	INxM pin diagnostics scan selection for single-ended configuration. 0d = INxM pins of single-ended channels are excluded for diagnosis 1d = INxM pins of single-ended channels are included for diagnosis
0	INCL_AC_COUP	R/W	0b	AC-coupled channels pins scan selection for diagnostics. 0d = INxP and INxM pins of AC-coupled channels are excluded for diagnosis 1d = INxP and INxM pins of AC-coupled channels are included for diagnosis

8.6.1.2.48 DIAG_CFG1 Register (Address = 0x65) [Reset = 0x37]

DIAG_CFG1 is shown in Figure 8-120 and described in Table 8-100.

Return to the Table 8-52.

This register is configuration register 1 for input fault diagnostics setting.

Figure 8-120. DIAG_CFG1 Register

7	6	5	4	3	2	1	0
DIAG_SHT_TERM[3:0]				DIAG_SHT_VBAT_IN[3:0]			
R/W-0011b				R/W-0111b			

Table 8-100. DIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_TERM[3:0]	R/W	0011b	INxP and INxM terminal short detect threshold. 0d = INxP and INxM terminal short detect threshold value is 0 mV (typ) 1d = INxP and INxM terminal short detect threshold value is 30 mV (typ) 2d = INxP and INxM terminal short detect threshold value is 60 mV (typ) 10d to 13d = INxP and INxM terminal short detect threshold value is set as per configuration 14d = INxP and INxM terminal short detect threshold value is 420 mV (typ) 15d = INxP and INxM terminal short detect threshold value is 450 mV (typ)
3-0	DIAG_SHT_VBAT_IN[3:0]	R/W	0111b	Short to VBAT_IN detect threshold. 0d = Short to VBAT_IN detect threshold value is 0 mV (typ) 1d = Short to VBAT_IN detect threshold value is 30 mV (typ) 2d = Short to VBAT_IN detect threshold value is 60 mV (typ) 10d to 13d = Short to VBAT_IN detect threshold value is set as per configuration 14d = Short to VBAT_IN detect threshold value is 420 mV (typ) 15d = Short to VBAT_IN detect threshold value is 450 mV (typ)

8.6.1.2.49 DIAG_CFG2 Register (Address = 0x66) [Reset = 0x87]

DIAG_CFG2 is shown in Figure 8-121 and described in Table 8-101.

Return to the Table 8-52.

This register is configuration register 2 for input fault diagnostics setting.

Figure 8-121. DIAG_CFG2 Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">DIAG_SHT_GND[3:0]</td><td colspan="4">DIAG_SHT_MICBIAS[3:0]</td></tr>
<tr><td colspan="4">R/W-1000b</td><td colspan="4">R/W-0111b</td></tr>
</table>

Table 8-101. DIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_GND[3:0]	R/W	1000b	Short to ground detect threshold. 0d = Short to ground detect threshold value is 0 mV (typ) 1d = Short to ground detect threshold value is 60 mV (typ) 2d = Short to ground detect threshold value is 120 mV (typ) 10d to 13d = Short to ground detect threshold value is set as per configuration 14d = Short to ground detect threshold value is 840 mV (typ) 15d = Short to ground detect threshold value is 900 mV (typ)
3-0	DIAG_SHT_MICBIAS[3:0]	R/W	0111b	Short to MICBIAS detect threshold. 0d = Short to MICBIAS detect threshold value is 0 mV (typ) 1d = Short to MICBIAS detect threshold value is 30 mV (typ) 2d = Short to MICBIAS detect threshold value is 60 mV (typ) 10d to 13d = Short to MICBIAS detect threshold value is set as per configuration 14d = Short to MICBIAS detect threshold value is 420 mV (typ) 15d = Short to MICBIAS detect threshold value is 450 mV (typ)

8.6.1.2.50 DIAG_CFG3 Register (Address = 0x67) [Reset = 0xB8]

DIAG_CFG3 is shown in Figure 8-122 and described in Table 8-102.

Return to the Table 8-52.

This register is configuration register 3 for input fault diagnostics setting.

Figure 8-122. DIAG_CFG3 Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="2">REP_RATE[1:0]</td><td colspan="2">RESERVED</td><td colspan="2">FAULT_DBNCE_SEL[1:0]</td><td>VSHORT_DBNCE</td><td>DIAG_2X_THRES</td></tr>
<tr><td colspan="2">R/W-10b</td><td colspan="2">R/W-11b</td><td colspan="2">R/W-10b</td><td>R/W-0b</td><td>R/W-0b</td></tr>
</table>

Table 8-102. DIAG_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	REP_RATE[1:0]	R/W	10b	Fault monitoring scan repetition rate. 0d = Countinuos back to back scanning of selected channels input pins without any idle time 1d = Fault monitoring repetition rate of 1 ms for selected channels input pins scanning 2d = Fault monitoring repetition rate of 4 ms for selected channels input pins scanning 3d = Fault monitoring repetition rate of 8 ms for selected channels input pins scanning
5-4	RESERVED	R/W	11b	Reserved bits; Write only reset values

Table 8-102. DIAG_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	FAULT_DBNCE_SEL[1:0]	R/W	10b	Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS). 0d = 16 counts for debounce to filter-out any false faults detection 1d = 8 counts for debounce to filter-out any false faults detection 2d = 4 counts for debounce to filter-out any false faults detection 3d = No debounce count
1	VSHORT_DBNCE	R/W	0b	VBAT_IN short debounce count only when VBAT_IN < MICBIAS. 0d = 16 counts for debounce to filter-out any false faults detection 1d = 8 counts for debounce to filter-out any false faults detection
0	DIAG_2X_THRES	R/W	0b	Diagnostic thresholds range scale. 0d = Thresholds same as configured in P0_R101 and P0_R102 1d = All the configuration thresholds gets scale by 2 times

8.6.1.2.51 DIAG_CFG4 Register (Address = 0x68) [Reset = 0x0]

DIAG_CFG4 is shown in Figure 8-123 and described in Table 8-103.

Return to the Table 8-52.

This register is configuration register 4 for input fault diagnostics setting.

Figure 8-123. DIAG_CFG4 Register

7	6	5	4	3	2	1	0
DIAG_MOV_AVG_CFG[1:0]		MOV_AVG_DIS_MBIAS_LOAD	MOV_AVG_DIS_TEMP_SENS	RESERVED			
R/W-00b		R/W-0b	R/W-0b	R-0000b			

Table 8-103. DIAG_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIAG_MOV_AVG_CFG[1:0]	R/W	00b	Moving average configuration. 0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for old scanned data and new scanned data 2d = Moving average enabled with 0.75 weightage for old scanned data and 0.25 weightage for new scanned data 3d = Reserved
5	MOV_AVG_DIS_MBIAS_LOAD	R/W	0b	Moving average configuration for MICBIAS high and low load current fault detection 0d = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for MICBIAS load current fault detection to achieve faster response time
4	MOV_AVG_DIS_TEMP_SENS	R/W	0b	Moving average configuration for over temperature fault detection 0d = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for over temperature fault detection to achieve faster response time
3-0	RESERVED	R	0000b	Reserved bits; Write only reset values

8.6.1.2.52 BOOST_CFG Register (Address = 0x6A) [Reset = 0x0]

BOOST_CFG is shown in Figure 8-124 and described in Table 8-104.

Return to the Table 8-52.

This register is configuration register for boost setting.

Figure 8-124. BOOST_CFG Register

7	6	5	4	3	2	1	0

Figure 8-124. BOOST_CFG Register (continued)

BOOST_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-000b		

Table 8-104. BOOST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOST_DIS	R/W	0b	Boost Enable/Disable 0d = Boost is enable 1d = Boost is disable/bypass
6	RESERVED	R/W	0b	Reserved bit; Write only reset value
5	RESERVED	R/W	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2-0	RESERVED	R	000b	Reserved bits; Write only reset values

8.6.1.2.53 DSP_CFG0 Register (Address = 0x6B) [Reset = 0x1]

DSP_CFG0 is shown in Figure 8-125 and described in Table 8-105.

Return to the Table 8-52.

This register is the digital signal processor (DSP) configuration register 0.

Figure 8-125. DSP_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED		DECI_FILT[1:0]		CH_SUM[1:0]		HPF_SEL[1:0]	
R-00b		R/W-00b		R/W-00b		R/W-01b	

Table 8-105. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-4	DECI_FILT[1:0]	R/W	00b	Decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency Dont use
3-2	CH_SUM[1:0]	R/W	00b	Channel summation mode for higher SNR 0d = Channel summation mode is disabled 1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 2d = Reserved 3d = Reserved
1-0	HPF_SEL[1:0]	R/W	01b	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 x f_S (384 Hz at f_S = 48 kHz) is selected

8.6.1.2.54 DSP_CFG1 Register (Address = 0x6C) [Reset = 0x48]

DSP_CFG1 is shown in Figure 8-126 and described in Table 8-106.

Return to the Table 8-52.

This register is the digital signal processor (DSP) configuration register 1.

Figure 8-126. DSP_CFG1 Register

7	6	5	4	3	2	1	0
DVOL_GANG	BIQUAD_CFG[1:0]		DISABLE_SOFT_STEP	AGC_SEL	RESERVED	RESERVED	
R/W-0b	R/W-10b		R/W-0b	R/W-1b	R/W-0b	R-00b	

Table 8-106. DSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DVOL_GANG	R/W	0b	DVOL control ganged across channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not
6-5	BIQUAD_CFG[1:0]	R/W	10b	Number of biquads per channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
4	DISABLE_SOFT_STEP	R/W	0b	Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
3	AGC_SEL	R/W	1b	AGC master enable setting. 0d = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFG0 register
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

8.6.1.2.55 AGC_CFG0 Register (Address = 0x70) [Reset = 0xE7]

AGC_CFG0 is shown in Figure 8-127 and described in Table 8-107.

Return to the Table 8-52.

This register is the automatic gain controller (AGC) configuration register 0.

Figure 8-127. AGC_CFG0 Register

7	6	5	4	3	2	1	0
AGC_LVL[3:0]				AGC_MAXGAIN[3:0]			
R/W-1110b				R/W-0111b			

Table 8-107. AGC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	AGC_LVL[3:0]	R/W	1110b	AGC output signal target level. 0d = Output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is as per configuration 14d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB

Table 8-107. AGC_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AGC_MAXGAIN[3:0]	R/W	0111b	AGC maximum gain allowed. 0d = Maximum gain allowed is 3 dB 1d = Maximum gain allowed is 6 dB 2d = Maximum gain allowed is 9 dB 3d to 11d = Maximum gain allowed is as per configuration 12d = Maximum gain allowed is 39 dB 13d = Maximum gain allowed is 42 dB 14d to 15d = Reserved

8.6.1.2.56 IN_CH_EN Register (Address = 0x73) [Reset = 0xFC]

IN_CH_EN is shown in Figure 8-128 and described in Table 8-108.

Return to the Table 8-52.

This register is the input channel enable configuration register.

Figure 8-128. IN_CH_EN Register

7	6	5	4	3	2	1	0
IN_CH1_EN	IN_CH2_EN	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W-0b

Table 8-108. IN_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_EN	R/W	1b	Input channel 1 enable setting. 0d = Channel 1 is disabled 1d = Channel 1 is enabled
6	IN_CH2_EN	R/W	1b	Input channel 2 enable setting. 0d = Channel 2 is disabled 1d = Channel 2 is enabled
5	RESERVED	R/W	1b	Reserved bit; Write only reset value
4	RESERVED	R/W	1b	Reserved bit; Write only reset value
3	RESERVED	R/W	1b	Reserved bit; Write only reset value
2	RESERVED	R/W	1b	Reserved bit; Write only reset value
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

8.6.1.2.57 ASI_OUT_CH_EN Register (Address = 0x74) [Reset = 0x0]

ASI_OUT_CH_EN is shown in Figure 8-129 and described in Table 8-109.

Return to the Table 8-52.

This register is the ASI output channel enable configuration register.

Figure 8-129. ASI_OUT_CH_EN Register

7	6	5	4	3	2	1	0
ASI_OUT_CH1_EN	ASI_OUT_CH2_EN	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-109. ASI_OUT_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_OUT_CH1_EN	R/W	0b	ASI output channel 1 enable setting. 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled
6	ASI_OUT_CH2_EN	R/W	0b	ASI output channel 2 enable setting. 0d = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled
5	RESERVED	R/W	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

8.6.1.2.58 PWR_CFG Register (Address = 0x75) [Reset = 0x0]

PWR_CFG is shown in Figure 8-130 and described in Table 8-110.

Return to the Table 8-52.

This register is the power-up configuration register.

Figure 8-130. PWR_CFG Register

7	6	5	4	3	2	1	0
MICBIAS_PDZ	ADC_PDZ	PLL_PDZ	DYN_CH_PUPD_EN	RESERVED		RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R-0b

Table 8-110. PWR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_PDZ	R/W	0b	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS
6	ADC_PDZ	R/W	0b	Power control for ADC and PDM channels. 0d = Power down all ADC and PDM channels 1d = Power up all enabled ADC and PDM channels
5	PLL_PDZ	R/W	0b	Power control for the PLL. 0d = Power down the PLL 1d = Power up the PLL
4	DYN_CH_PUPD_EN	R/W	0b	Dynamic channel power-up, power-down enable. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on. Do not powered-down channel 1 if this bit is set to '1'
3-2	RESERVED	R/W	00b	Reserved bits; Write only reset values
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.59 DEV_STS0 Register (Address = 0x76) [Reset = 0x0]

DEV_STS0 is shown in Figure 8-131 and described in Table 8-111.

Return to the Table 8-52.

This register is the device status value register 0.

Figure 8-131. DEV_STS0 Register

7	6	5	4	3	2	1	0
CH1_STATUS	CH2_STATUS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-111. DEV_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_STATUS	R	0b	ADC channel 1 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
6	CH2_STATUS	R	0b	ADC channel 2 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.2.60 DEV_STS1 Register (Address = 0x77) [Reset = 0x80]

DEV_STS1 is shown in Figure 8-132 and described in Table 8-112.

Return to the Table 8-52.

This register is the device status value register 1.

Figure 8-132. DEV_STS1 Register

7	6	5	4	3	2	1	0
MODE_STS[2:0]			BOOST_STS	MBIAS_STS	CHx_PD_FLT_STS	ALL_CHx_PD_FLT_STS	MAN_RCV_PD_FLT_CHK
R-100b			R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 8-112. DEV_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MODE_STS[2:0]	R	100b	Device mode status. 4d = Device is in sleep mode or software shutdown mode 6d = Device is in active mode with all ADC or PDM channels turned off 7d = Device is in active mode with at least one ADC or PDM channel turned on
4	BOOST_STS	R	0b	Boost power up status. 0d = Boost is powered down 1d = Boost is powered up
3	MBIAS_STS	R	0b	MICBIAS power up status. 0d = MICBIAS is powered down 1d = MICBIAS is powered up
2	CHx_PD_FLT_STS	R	0b	ADC channel power down status caused by INxx inputs faults. 0d = No ADC channel is powered down caused by INxx inputs faults 1d = Atleast a ADC channel is powered down caused by INxx inputs faults
1	ALL_CHx_PD_FLT_STS	R	0b	ADC channel power down status caused by MICBIAS faults. 0d = No ADC channel is powered down caused by MICBIAS faults 1d = All ADC channels are powered down caused by MICBIAS faults

Table 8-112. DEV_STS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MAN_RCV_PD_FLT_CHK	R/W	0b	Manual recovery (self-clearing bit). 0d = No effect 1d = Recheck all fault status and re-powerup ADC channels and/or MICBIAS if they do not have any faults. Before setting this bit, reset P0_R58 register and re-configure P0_R58 to desired setting only after manual recover gets over.

8.6.1.2.61 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x0]

I2C_CKSUM is shown in Figure 8-133 and described in Table 8-113.

Return to the Table 8-52.

This register returns the I^2C transactions checksum value

Figure 8-133. I2C_CKSUM Register

7	6	5	4	3	2	1	0
I2C_CKSUM[7:0]							
R/W-00000000b							

Table 8-113. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	00000000b	These bits return the I^2C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages.

8.6.1.3 Page 1 Registers

Table 8-114 lists the memory-mapped registers for the Page 1 registers. All register offset addresses not listed in Table 8-114 should be considered as reserved locations and the register contents should not be modified.

Table 8-114. PAGE 1 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 8.6.1.3.1
0x16	MBIAS_LOAD	MICBIAS internal load sink configuration register	0x00	Section 8.6.1.3.2
0x2C	INT_LIVE0	Live interrupt readback register 0	0x00	Section 8.6.1.3.3
0x2D	CHx_LIVE	Channel diagnostic summary live status register	0x00	Section 8.6.1.3.4
0x2E	CH1_LIVE	Channel 1 diagnostic live status register	0x00	Section 8.6.1.3.5
0x2F	CH2_LIVE	Channel 2 diagnostic live status register	0x00	Section 8.6.1.3.6
0x35	INT_LIVE1	Live interrupt readback register 1	0x00	Section 8.6.1.3.7
0x37	INT_LIVE3	Live interrupt readback register 3	0x00	Section 8.6.1.3.8
0x55	MBIAS_OV_CFG	MICBIAS overvoltage threshold register	0x40	Section 8.6.1.3.9
0x59	DIAGDATA_CFG	Diagnostic data configuration register	0x00	Section 8.6.1.3.10
0x5A	DIAG_MON_MSB_VBAT	Diagnostic VBAT_IN data MSB byte register	0x00	Section 8.6.1.3.11
0x5B	DIAG_MON_LSB_VBAT	Diagnostic VBAT_IN data LSB nibble register	0x00	Section 8.6.1.3.12
0x5C	DIAG_MON_MSB_MBIAS	Diagnostic MICBIAS data MSB byte register	0x00	Section 8.6.1.3.13
0x5D	DIAG_MON_LSB_MBIAS	Diagnostic MICBIAS data LSB nibble register	0x01	Section 8.6.1.3.14
0x5E	DIAG_MON_MSB_IN1P	Diagnostic IN1P data MSB byte register	0x00	Section 8.6.1.3.15
0x5F	DIAG_MON_LSB_IN1P	Diagnostic IN1P data LSB nibble register	0x02	Section 8.6.1.3.16
0x60	DIAG_MON_MSB_IN1M	Diagnostic IN1M data MSB byte register	0x00	Section 8.6.1.3.17
0x61	DIAG_MON_LSB_IN1M	Diagnostic IN1M data LSB nibble register	0x03	Section 8.6.1.3.18
0x62	DIAG_MON_MSB_IN2P	Diagnostic IN2P data MSB byte register	0x00	Section 8.6.1.3.19
0x63	DIAG_MON_LSB_IN2P	Diagnostic IN2P data LSB nibble register	0x04	Section 8.6.1.3.20
0x64	DIAG_MON_MSB_IN2M	Diagnostic IN2M data MSB byte register	0x00	Section 8.6.1.3.21
0x65	DIAG_MON_LSB_IN2M	Diagnostic IN2M data LSB nibble register	0x05	Section 8.6.1.3.22
0x76	DIAG_MON_MSB_TEMP	Diagnostic temperature data MSB byte register	0x00	Section 8.6.1.3.23
0x77	DIAG_MON_LSB_TEMP	Diagnostic temperature data LSB nibble register	0x0E	Section 8.6.1.3.24
0x78	DIAG_MON_MSB_LOAD	Diagnostic MICBIAS load current data MSB byte register	0x00	Section 8.6.1.3.25
0x79	DIAG_MON_LSB_LOAD	Diagnostic MICBIAS load current data LSB nibble register	0x0F	Section 8.6.1.3.26
0x7E	REV_ID	Silicon revision ID register	0x20	Section 8.6.1.3.27

8.6.1.3.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x0]

PAGE_CFG is shown in Figure 8-134 and described in Table 8-115.

Return to the Table 8-114.

The device memory map is divided into pages. This register sets the page.

Figure 8-134. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

Table 8-115. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 … 255d = Page 255

8.6.1.3.2 MBIAS_LOAD Register (Address = 0x16) [Reset = 0x0]

MBIAS_LOAD is shown in Figure 8-135 and described in Table 8-116.

Return to the Table 8-114.

This register is the MICBIAS internal load sink configuration register.

Figure 8-135. MBIAS_LOAD Register

7	6	5	4	3	2	1	0
MICBIAS_INT_LOAD_SINK_EN	MICBIAS_INT_LOAD_SINK_VAL[2:0]			RESERVED			
R/W-0b	R/W-000b			R-0000b			

Table 8-116. MBIAS_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_INT_LOAD_SINK_EN	R/W	0b	MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing
6-4	MICBIAS_INT_LOAD_SINK_VAL[2:0]	R/W	000b	MICBIAS internal load sink current value. 0d = MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 8.6 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 30.1 mA (typ)
3-0	RESERVED	R	0000b	Reserved bits; Write only reset values

8.6.1.3.3 INT_LIVE0 Register (Address = 0x2C) [Reset = 0x0]

INT_LIVE0 is shown in Figure 8-136 and described in Table 8-117.

Return to the Table 8-114.

This register is the live Interrupt readback register 0.

Figure 8-136. INT_LIVE0 Register

7	6	5	4	3	2	1	0
INT_LIVE0	INT_LIVE0	INT_LIVE0	INT_LIVE0	RESERVED	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-117. INT_LIVE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE0	R	0b	Fault status for an ASI bus clock error. 0d = No fault detected 1d = Fault detected
6	INT_LIVE0	R	0b	Status of PLL lock. 0d = No PLL lock detected 1d = PLL lock detected
5	INT_LIVE0	R	0b	Fault status for boost or MICBIAS over temperature. 0d = No fault detected 1d = Fault detected
4	INT_LIVE0	R	0b	Fault status for boost or MICBIAS over current. 0d = No fault detected 1d = Fault detected
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.3.4 CHx_LIVE Register (Address = 0x2D) [Reset = 0x0]

CHx_LIVE is shown in Figure 8-137 and described in Table 8-118.

Return to the Table 8-114.

This register is the live Interrupt status register for channel level diagnostic summary.

Figure 8-137. CHx_LIVE Register

7	6	5	4	3	2	1	0
STS_CHx_LIVE	STS_CHx_LIVE	RESERVED	RESERVED	RESERVED	RESERVED	STS_CHx_LIVE	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-118. CHx_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LIVE	R	0b	Status of CH1_LIVE. 0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1
6	STS_CHx_LIVE	R	0b	Status of CH2_LIVE. 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	STS_CHx_LIVE	R	0b	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS. 0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.1.3.5 CH1_LIVE Register (Address = 0x2E) [Reset = 0x0]

CH1_LIVE is shown in Figure 8-138 and described in Table 8-119.

Return to the Table 8-114.

This register is the live Interrupt status register for channel 1 fault diagnostic

Figure 8-138. CH1_LIVE Register

7	6	5	4	3	2	1	0
CH1_LIVE	CH1_LIVE	CH1_LIVE	CH1_LIVE	CH1_LIVE	CH1_LIVE	CH1_LIVE	CH1_LIVE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-119. CH1_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_LIVE	R	0b	Channel 1 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH1_LIVE	R	0b	Channel 1 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected
5	CH1_LIVE	R	0b	Channel 1 IN1P short to ground fault status. 0d = IN1P no short to ground detected 1d = IN1P short to ground detected
4	CH1_LIVE	R	0b	Channel 1 IN1M short to ground fault status. 0d = IN1M no short to ground detected 1d = IN1M short to ground detected
3	CH1_LIVE	R	0b	Channel 1 IN1P short to MICBIAS fault status. 0d = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected
2	CH1_LIVE	R	0b	Channel 1 IN1M short to MICBIAS fault status. 0d = IN1M no short to MICBIAS detected 1d = IN1M short to MICBIAS detected
1	CH1_LIVE	R	0b	Channel 1 IN1P short to VBAT_IN fault status. 0d = IN1P no short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected
0	CH1_LIVE	R	0b	Channel 1 IN1M short to VBAT_IN fault status. 0d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected

8.6.1.3.6 CH2_LIVE Register (Address = 0x2F) [Reset = 0x0]

CH2_LIVE is shown in Figure 8-139 and described in Table 8-120.

Return to the Table 8-114.

This register is the live Interrupt status register for channel 2 fault diagnostic.

Figure 8-139. CH2_LIVE Register

7	6	5	4	3	2	1	0
CH2_LIVE	CH2_LIVE	CH2_LIVE	CH2_LIVE	CH2_LIVE	CH2_LIVE	CH2_LIVE	CH2_LIVE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-120. CH2_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_LIVE	R	0b	Channel 2 open input fault status. 0d = No open input detected 1d = Open input detected
6	CH2_LIVE	R	0b	Channel 2 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected

Table 8-120. CH2_LIVE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH2_LIVE	R	0b	Channel 2 IN2P short to ground fault status. 0d = IN2P no short to ground detected 1d = IN2P short to ground detected
4	CH2_LIVE	R	0b	Channel 2 IN2M short to ground fault status. 0d = IN2M no short to ground detected 1d = IN2M short to ground detected
3	CH2_LIVE	R	0b	Channel 2 IN2P short to MICBIAS fault status. 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected
2	CH2_LIVE	R	0b	Channel 2 IN2M short to MICBIAS fault status. 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected
1	CH2_LIVE	R	0b	Channel 2 IN2P short to VBAT_IN fault status. 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected
0	CH2_LIVE	R	0b	Channel 2 IN2M short to VBAT_IN fault status. 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected

8.6.1.3.7 INT_LIVE1 Register (Address = 0x35) [Reset = 0x0]

INT_LIVE1 is shown in Figure 8-140 and described in Table 8-121.

Return to the Table 8-114.

This register is the live Interrupt readback register 1.

Figure 8-140. INT_LIVE1 Register

7	6	5	4	3	2	1	0
INT_LIVE1	INT_LIVE1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

Table 8-121. INT_LIVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE1	R	0b	Channel 1 IN1P over voltage fault status. 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected
6	INT_LIVE1	R	0b	Channel 2 IN2P over voltage fault status. 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault has detected
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R	0b	Reserved bit; Write only reset value
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

8.6.1.3.8 INT_LIVE3 Register (Address = 0x37) [Reset = 0x0]

INT_LIVE3 is shown in Figure 8-141 and described in Table 8-122.

Return to the Table 8-114.

This register is the live Interrupt readback register 3.

Figure 8-141. INT_LIVE3 Register

7	6	5	4	3	2	1	0
INT_LIVE3	INT_LIVE3	INT_LIVE3	RESERVED				
R-0b	R-0b	R-0b	R-00000b				

Table 8-122. INT_LIVE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE3	R	0b	Fault status for MICBIAS high current. 0d = No fault detected 1d = Fault detected
6	INT_LIVE3	R	0b	Fault status for MICBIAS low current. 0d = No fault detected 1d = Fault detected
5	INT_LIVE3	R	0b	Fault status for MICBIAS over voltage. 0d = No fault detected 1d = Fault detected
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.1.3.9 MBIAS_OV_CFG Register (Address = 0x55) [Reset = 0x40]

MBIAS_OV_CFG is shown in Figure 8-142 and described in Table 8-123.

Return to the Table 8-114.

This register is the MICBIAS overvoltage configuration register.

Figure 8-142. MBIAS_OV_CFG Register

7	6	5	4	3	2	1	0
MBIAS_OV_THRES[2:0]			RESERVED				
R/W-010b			R-00000b				

Table 8-123. MBIAS_OV_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MBIAS_OV_THRES[2:0]	R/W	010b	MICBIAS overvoltage fault detection threshold above MICBIAS programmed voltage. 0d = No threshold over programmed voltage 1d = 10mV (typ) threshold over programmed voltage 2d = 40mV (typ) threshold over programmed voltage (default) 3d to 6d = Threshold value is set as per configuration with step size of 30mV (typ) 7d = 190mV (typ) threshold over programmed voltage (default)
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.1.3.10 DIAGDATA_CFG Register (Address = 0x59) [Reset = 0x0]

DIAGDATA_CFG is shown in Figure 8-143 and described in Table 8-124.

Return to the Table 8-114.

This register is the diagnostic data configuration register.

Figure 8-143. DIAGDATA_CFG Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			HOLD_SAR_DATA
R/W-0000b				R-000b			R/W-0b

Table 8-124. DIAGDATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000b	Reserved bits; Write only reset values
3-1	RESERVED	R	000b	Reserved bits; Write only reset values
0	HOLD_SAR_DATA	R/W	0b	Hold SAR data update during register readback. 0d = Data update is not held, data register is continuously updated; this setting must be used when moving average is enabled for fault detection 1d = Data update is held, data register readback can be done

8.6.1.3.11 DIAG_MON_MSB_VBAT Register (Address = 0x5A) [Reset = 0x0]

DIAG_MON_MSB_VBAT is shown in Figure 8-144 and described in Table 8-125.

Return to the Table 8-114.

This register is the MSB data byte of VBAT_IN monitoring.

Figure 8-144. DIAG_MON_MSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_VBAT[7:0]							
R-00000000b							

Table 8-125. DIAG_MON_MSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_VBAT[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.12 DIAG_MON_LSB_VBAT Register (Address = 0x5B) [Reset = 0x0]

DIAG_MON_LSB_VBAT is shown in Figure 8-145 and described in Table 8-126.

Return to the Table 8-114.

This register is the LSB data nibble of VBAT_IN monitoring.

Figure 8-145. DIAG_MON_LSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_VBAT[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-0000b			

Table 8-126. DIAG_MON_LSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_VBAT[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0000b	Channel ID value.

8.6.1.3.13 DIAG_MON_MSB_MBIAS Register (Address = 0x5C) [Reset = 0x0]

DIAG_MON_MSB_MBIAS is shown in Figure 8-146 and described in Table 8-127.

Return to the Table 8-114.

This register is the MSB data byte of MICBIAS monitoring.

Figure 8-146. DIAG_MON_MSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_MBIAS[7:0]							
R-00000000b							

Table 8-127. DIAG_MON_MSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_MBIAS[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.14 DIAG_MON_LSB_MBIAS Register (Address = 0x5D) [Reset = 0x1]

DIAG_MON_LSB_MBIAS is shown in Figure 8-147 and described in Table 8-128.

Return to the Table 8-114.

This register is the LSB data nibble of MICBIAS monitoring.

Figure 8-147. DIAG_MON_LSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_MBIAS[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-0001b			

Table 8-128. DIAG_MON_LSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_MBIAS[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0001b	Channel ID value.

8.6.1.3.15 DIAG_MON_MSB_IN1P Register (Address = 0x5E) [Reset = 0x0]

DIAG_MON_MSB_IN1P is shown in Figure 8-148 and described in Table 8-129.

Return to the Table 8-114.

This register is the MSB data byte of IN1P monitoring.

Figure 8-148. DIAG_MON_MSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH1P[7:0]							
R-00000000b							

Table 8-129. DIAG_MON_MSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH1P[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.16 DIAG_MON_LSB_IN1P Register (Address = 0x5F) [Reset = 0x2]

DIAG_MON_LSB_IN1P is shown in Figure 8-149 and described in Table 8-130.

Return to the Table 8-114.

This register is the LSB data nibble of IN1P monitoring.

Figure 8-149. DIAG_MON_LSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH1P[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-0010b			

Table 8-130. DIAG_MON_LSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH1P[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0010b	Channel ID value.

8.6.1.3.17 DIAG_MON_MSB_IN1M Register (Address = 0x60) [Reset = 0x0]

DIAG_MON_MSB_IN1M is shown in Figure 8-150 and described in Table 8-131.

Return to the Table 8-114.

This register is the MSB data byte of IN1M monitoring.

Figure 8-150. DIAG_MON_MSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_CH1N[7:0]							
R-00000000b							

Table 8-131. DIAG_MON_MSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH1N[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.18 DIAG_MON_LSB_IN1M Register (Address = 0x61) [Reset = 0x3]

DIAG_MON_LSB_IN1M is shown in Figure 8-151 and described in Table 8-132.

Return to the Table 8-114.

This register is the LSB data nibble of IN1M monitoring.

Figure 8-151. DIAG_MON_LSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH1N[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-0011b			

Table 8-132. DIAG_MON_LSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH1N[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0011b	Channel ID value.

8.6.1.3.19 DIAG_MON_MSB_IN2P Register (Address = 0x62) [Reset = 0x0]

DIAG_MON_MSB_IN2P is shown in Figure 8-152 and described in Table 8-133.

Return to the Table 8-114.

This register is the MSB data byte of IN2P monitoring.

Figure 8-152. DIAG_MON_MSB_IN2P Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">DIAG_MON_MSB_CH2P[7:0]</td></tr>
<tr><td colspan="8">R-00000000b</td></tr>
</table>

Table 8-133. DIAG_MON_MSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH2P[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.20 DIAG_MON_LSB_IN2P Register (Address = 0x63) [Reset = 0x4]

DIAG_MON_LSB_IN2P is shown in Figure 8-153 and described in Table 8-134.

Return to the Table 8-114.

This register is the LSB data nibble of IN2P monitoring.

Figure 8-153. DIAG_MON_LSB_IN2P Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">DIAG_MON_LSB_CH2P[3:0]</td><td colspan="4">CHANNEL_ID[3:0]</td></tr>
<tr><td colspan="4">R-0000b</td><td colspan="4">R-0100b</td></tr>
</table>

Table 8-134. DIAG_MON_LSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH2P[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0100b	Channel ID value.

8.6.1.3.21 DIAG_MON_MSB_IN2M Register (Address = 0x64) [Reset = 0x0]

DIAG_MON_MSB_IN2M is shown in Figure 8-154 and described in Table 8-135.

Return to the Table 8-114.

This register is the MSB data byte of IN2M monitoring.

Figure 8-154. DIAG_MON_MSB_IN2M Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">DIAG_MON_MSB_CH2N[7:0]</td></tr>
<tr><td colspan="8">R-00000000b</td></tr>
</table>

Table 8-135. DIAG_MON_MSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_CH2N[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.22 DIAG_MON_LSB_IN2M Register (Address = 0x65) [Reset = 0x5]

DIAG_MON_LSB_IN2M is shown in Figure 8-155 and described in Table 8-136.

Return to the Table 8-114.

This register is the LSB data nibble of IN2M monitoring.

Figure 8-155. DIAG_MON_LSB_IN2M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_CH2N[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-0101b			

Table 8-136. DIAG_MON_LSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_CH2N[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	0101b	Channel ID value.

8.6.1.3.23 DIAG_MON_MSB_TEMP Register (Address = 0x76) [Reset = 0x0]

DIAG_MON_MSB_TEMP is shown in Figure 8-156 and described in Table 8-137.

Return to the Table 8-114.

This register is the MSB data byte of temperature monitoring.

Figure 8-156. DIAG_MON_MSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_TEMP[7:0]							
R-00000000b							

Table 8-137. DIAG_MON_MSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_TEMP[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.24 DIAG_MON_LSB_TEMP Register (Address = 0x77) [Reset = 0xE]

DIAG_MON_LSB_TEMP is shown in Figure 8-157 and described in Table 8-138.

Return to the Table 8-114.

This register is the LSB data nibble of temperature monitoring.

Figure 8-157. DIAG_MON_LSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_TEMP[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-1110b			

Table 8-138. DIAG_MON_LSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_TEMP[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	1110b	Channel ID value.

8.6.1.3.25 DIAG_MON_MSB_LOAD Register (Address = 0x78) [Reset = 0x0]

DIAG_MON_MSB_LOAD is shown in Figure 8-158 and described in Table 8-139.

Return to the Table 8-114.

This register is the MSB data byte of MICBIAS load current monitoring.

Figure 8-158. DIAG_MON_MSB_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_LOAD[7:0]							
R-00000000b							

Table 8-139. DIAG_MON_MSB_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_LOAD[7:0]	R	00000000b	Diagnostic SAR monitor data MSB byte.

8.6.1.3.26 DIAG_MON_LSB_LOAD Register (Address = 0x79) [Reset = 0xF]

DIAG_MON_LSB_LOAD is shown in Figure 8-159 and described in Table 8-140.

Return to the Table 8-114.

This register is the LSB data nibble of MICBIAS load current monitoring.

Figure 8-159. DIAG_MON_LSB_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_LOAD[3:0]				CHANNEL_ID[3:0]			
R-0000b				R-1111b			

Table 8-140. DIAG_MON_LSB_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_LOAD[3:0]	R	0000b	Diagnostic SAR monitor data LSB nibble.
3-0	CHANNEL_ID[3:0]	R	1111b	Channel ID value.

8.6.1.3.27 REV_ID Register (Address = 0x7E) [Reset = 0x20]

REV_ID is shown in Figure 8-160 and described in Table 8-141.

Return to the Table 8-114.

This register is the silicon revision ID register.

Figure 8-160. REV_ID Register

7	6	5	4	3	2	1	0
REV_ID[3:0]				RESERVED			
R-0010b				R-0000b			

Table 8-141. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID[3:0]	R	0010b	Returns the revision ID.
3-0	RESERVED	R	0000b	Reserved bits; Write only reset values

8.6.2 Programmable Coefficient Registers

8.6.2.1 Programmable Coefficient Registers: Page 2

This register page (shown in Table 8-142) consists of the programmable coefficients for the biquad 1 to biquad 6 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C and SPI burst writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value. These programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transmits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

Table 8-142. Page 2 Programmable Coefficient Registers

ADDRESS	ACRONYM	RESET VALUE	REGISTER DESCRIPTION
0x00	PAGE[7:0]	0x00	Section 8.6.1.2.1
0x08	BQ1_N0_BYT1[7:0]	0x7F	Programmable biquad 1, N0 coefficient byte[31:24]
0x09	BQ1_N0_BYT2[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[23:16]
0x0A	BQ1_N0_BYT3[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[15:8]
0x0B	BQ1_N0_BYT4[7:0]	0xFF	Programmable biquad 1, N0 coefficient byte[7:0]
0x0C	BQ1_N1_BYT1[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[31:24]
0x0D	BQ1_N1_BYT2[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[23:16]
0x0E	BQ1_N1_BYT3[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[15:8]
0x0F	BQ1_N1_BYT4[7:0]	0x00	Programmable biquad 1, N1 coefficient byte[7:0]
0x10	BQ1_N2_BYT1[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[31:24]
0x11	BQ1_N2_BYT2[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[23:16]
0x12	BQ1_N2_BYT3[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[15:8]
0x13	BQ1_N2_BYT4[7:0]	0x00	Programmable biquad 1, N2 coefficient byte[7:0]
0x14	BQ1_D1_BYT1[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[31:24]
0x15	BQ1_D1_BYT2[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[23:16]
0x16	BQ1_D1_BYT3[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[15:8]
0x17	BQ1_D1_BYT4[7:0]	0x00	Programmable biquad 1, D1 coefficient byte[7:0]
0x18	BQ1_D2_BYT1[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[31:24]
0x19	BQ1_D2_BYT2[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[23:16]
0x1A	BQ1_D2_BYT3[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[15:8]
0x1B	BQ1_D2_BYT4[7:0]	0x00	Programmable biquad 1, D2 coefficient byte[7:0]
0x1C	BQ2_N0_BYT1[7:0]	0x7F	Programmable biquad 2, N0 coefficient byte[31:24]
0x1D	BQ2_N0_BYT2[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[23:16]
0x1E	BQ2_N0_BYT3[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[15:8]
0x1F	BQ2_N0_BYT4[7:0]	0xFF	Programmable biquad 2, N0 coefficient byte[7:0]
0x20	BQ2_N1_BYT1[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[31:24]
0x21	BQ2_N1_BYT2[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[23:16]
0x22	BQ2_N1_BYT3[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[15:8]
0x23	BQ2_N1_BYT4[7:0]	0x00	Programmable biquad 2, N1 coefficient byte[7:0]
0x24	BQ2_N2_BYT1[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[31:24]
0x25	BQ2_N2_BYT2[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[23:16]
0x26	BQ2_N2_BYT3[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[15:8]
0x27	BQ2_N2_BYT4[7:0]	0x00	Programmable biquad 2, N2 coefficient byte[7:0]
0x28	BQ2_D1_BYT1[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[31:24]
0x29	BQ2_D1_BYT2[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[23:16]
0x2A	BQ2_D1_BYT3[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[15:8]
0x2B	BQ2_D1_BYT4[7:0]	0x00	Programmable biquad 2, D1 coefficient byte[7:0]

Table 8-142. Page 2 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	RESET VALUE	REGISTER DESCRIPTION
0x2C	BQ2_D2_BYT1[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[31:24]
0x2D	BQ2_D2_BYT2[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[23:16]
0x2E	BQ2_D2_BYT3[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[15:8]
0x2F	BQ2_D2_BYT4[7:0]	0x00	Programmable biquad 2, D2 coefficient byte[7:0]
0x58	BQ5_N0_BYT1[7:0]	0x7F	Programmable biquad 5, N0 coefficient byte[31:24]
0x59	BQ5_N0_BYT2[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[23:16]
0x5A	BQ5_N0_BYT3[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[15:8]
0x5B	BQ5_N0_BYT4[7:0]	0xFF	Programmable biquad 5, N0 coefficient byte[7:0]
0x5C	BQ5_N1_BYT1[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[31:24]
0x5D	BQ5_N1_BYT2[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[23:16]
0x5E	BQ5_N1_BYT3[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[15:8]
0x5F	BQ5_N1_BYT4[7:0]	0x00	Programmable biquad 5, N1 coefficient byte[7:0]
0x60	BQ5_N2_BYT1[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[31:24]
0x61	BQ5_N2_BYT2[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[23:16]
0x62	BQ5_N2_BYT3[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[15:8]
0x63	BQ5_N2_BYT4[7:0]	0x00	Programmable biquad 5, N2 coefficient byte[7:0]
0x64	BQ5_D1_BYT1[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[31:24]
0x65	BQ5_D1_BYT2[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[23:16]
0x66	BQ5_D1_BYT3[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[15:8]
0x67	BQ5_D1_BYT4[7:0]	0x00	Programmable biquad 5, D1 coefficient byte[7:0]
0x68	BQ5_D2_BYT1[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[31:24]
0x69	BQ5_D2_BYT2[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[23:16]
0x6A	BQ5_D2_BYT3[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[15:8]
0x6B	BQ5_D2_BYT4[7:0]	0x00	Programmable biquad 5, D2 coefficient byte[7:0]
0x6C	BQ6_N0_BYT1[7:0]	0x7F	Programmable biquad 6, N0 coefficient byte[31:24]
0x6D	BQ6_N0_BYT2[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[23:16]
0x6E	BQ6_N0_BYT3[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[15:8]
0x6F	BQ6_N0_BYT4[7:0]	0xFF	Programmable biquad 6, N0 coefficient byte[7:0]
0x70	BQ6_N1_BYT1[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[31:24]
0x71	BQ6_N1_BYT2[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[23:16]
0x72	BQ6_N1_BYT3[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[15:8]
0x73	BQ6_N1_BYT4[7:0]	0x00	Programmable biquad 6, N1 coefficient byte[7:0]
0x74	BQ6_N2_BYT1[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[31:24]
0x75	BQ6_N2_BYT2[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[23:16]
0x76	BQ6_N2_BYT3[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[15:8]
0x77	BQ6_N2_BYT4[7:0]	0x00	Programmable biquad 6, N2 coefficient byte[7:0]
0x78	BQ6_D1_BYT1[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[31:24]
0x79	BQ6_D1_BYT2[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[23:16]
0x7A	BQ6_D1_BYT3[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[15:8]
0x7B	BQ6_D1_BYT4[7:0]	0x00	Programmable biquad 6, D1 coefficient byte[7:0]
0x7C	BQ6_D2_BYT1[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[31:24]
0x7D	BQ6_D2_BYT2[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[23:16]
0x7E	BQ6_D2_BYT3[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[15:8]
0x7F	BQ6_D2_BYT4[7:0]	0x00	Programmable biquad 6, D2 coefficient byte[7:0]

8.6.2.2 Programmable Coefficient Registers: Page 3

This register page (shown in Table 8-143) consists of the programmable coefficients for the biquad 9 and biquad 10 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^{2}C and SPI burst writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value. These programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transmits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

Table 8-143. Page 3 Programmable Coefficient Registers

ADDRESS	ACRONYM	RESET VALUE	REGISTER DESCRIPTION
0x00	PAGE[7:0]	0x00	Section 8.6.1.2.1
0x30	BQ9_N0_BYT1[7:0]	0x7F	Programmable biquad 9, N0 coefficient byte[31:24]
0x31	BQ9_N0_BYT2[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[23:16]
0x32	BQ9_N0_BYT3[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[15:8]
0x33	BQ9_N0_BYT4[7:0]	0xFF	Programmable biquad 9, N0 coefficient byte[7:0]
0x34	BQ9_N1_BYT1[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[31:24]
0x35	BQ9_N1_BYT2[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[23:16]
0x36	BQ9_N1_BYT3[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[15:8]
0x37	BQ9_N1_BYT4[7:0]	0x00	Programmable biquad 9, N1 coefficient byte[7:0]
0x38	BQ9_N2_BYT1[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[31:24]
0x39	BQ9_N2_BYT2[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[23:16]
0x3A	BQ9_N2_BYT3[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[15:8]
0x3B	BQ9_N2_BYT4[7:0]	0x00	Programmable biquad 9, N2 coefficient byte[7:0]
0x3C	BQ9_D1_BYT1[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[31:24]
0x3D	BQ9_D1_BYT2[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[23:16]
0x3E	BQ9_D1_BYT3[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[15:8]
0x3F	BQ9_D1_BYT4[7:0]	0x00	Programmable biquad 9, D1 coefficient byte[7:0]
0x40	BQ9_D2_BYT1[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[31:24]
0x41	BQ9_D2_BYT2[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[23:16]
0x42	BQ9_D2_BYT3[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[15:8]
0x43	BQ9_D2_BYT4[7:0]	0x00	Programmable biquad 9, D2 coefficient byte[7:0]
0x44	BQ10_N0_BYT1[7:0]	0x7F	Programmable biquad 10, N0 coefficient byte[31:24]
0x45	BQ10_N0_BYT2[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[23:16]
0x46	BQ10_N0_BYT3[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[15:8]
0x47	BQ10_N0_BYT4[7:0]	0xFF	Programmable biquad 10, N0 coefficient byte[7:0]
0x48	BQ10_N1_BYT1[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[31:24]
0x49	BQ10_N1_BYT2[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[23:16]
0x4A	BQ10_N1_BYT3[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[15:8]
0x4B	BQ10_N1_BYT4[7:0]	0x00	Programmable biquad 10, N1 coefficient byte[7:0]
0x4C	BQ10_N2_BYT1[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[31:24]
0x4D	BQ10_N2_BYT2[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[23:16]
0x4E	BQ10_N2_BYT3[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[15:8]
0x4F	BQ10_N2_BYT4[7:0]	0x00	Programmable biquad 10, N2 coefficient byte[7:0]
0x50	BQ10_D1_BYT1[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[31:24]
0x51	BQ10_D1_BYT2[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[23:16]
0x52	BQ10_D1_BYT3[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[15:8]
0x53	BQ10_D1_BYT4[7:0]	0x00	Programmable biquad 10, D1 coefficient byte[7:0]
0x54	BQ10_D2_BYT1[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[31:24]

Table 8-143. Page 3 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	RESET VALUE	REGISTER DESCRIPTION
0x55	BQ10_D2_BYT2[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[23:16]
0x56	BQ10_D2_BYT3[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[15:8]
0x57	BQ10_D2_BYT4[7:0]	0x00	Programmable biquad 10, D2 coefficient byte[7:0]

8.6.2.3 Programmable Coefficient Registers: Page 4

This register page (shown in Table 8-144) consists of the programmable coefficients for mixer 1 and mixer 2 and the first-order IIR filter. All mixer coefficients are 32-bit, two's complement numbers using a 1.31 number format. The value of 0x7FFFFFFF is equivalent to +1 (0-dB gain), the value 0x00000000 is equivalent to mute (zero data) and all values in between set the mixer attenuation computed using Equation 4. If the MSB is set to '1' then the attenuation remains the same but the signal phase is inverted. All IIR filter programmable coefficients are 32-bit, two's complement numbers. For a successful coefficient register transaction, the host device must write and read all four bytes starting with the most significant byte (BYT1) for a target coefficient register transaction. When using SPI for a coefficient register read transaction, the device transits the first byte as a dummy read byte; therefore, the host must read five bytes, including the first dummy read byte and the last four bytes corresponding to the coefficient register value starting with the most significant byte (BYT1).

$$\text{hex2dec (value)} / 2^{31} \tag{4}$$

Table 8-144. Page 4 Programmable Coefficient Registers

ADDRESS	ACRONYM	RESET VALUE	REGISTER DESCRIPTION
0x00	PAGE[7:0]	0x00	Section 8.6.1.2.1
0x08	MIX1_CH1_BYT1[7:0]	0x7F	Digital mixer 1, channel 1 coefficient byte[31:24]
0x09	MIX1_CH1_BYT2[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[23:16]
0x0A	MIX1_CH1_BYT3[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[15:8]
0x0B	MIX1_CH1_BYT4[7:0]	0xFF	Digital mixer 1, channel 1 coefficient byte[7:0]
0x0C	MIX1_CH2_BYT1[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[31:24]
0x0D	MIX1_CH2_BYT2[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[23:16]
0x0E	MIX1_CH2_BYT3[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[15:8]
0x0F	MIX1_CH2_BYT4[7:0]	0x00	Digital mixer 1, channel 2 coefficient byte[7:0]
0x18	MIX2_CH1_BYT1[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[31:24]
0x19	MIX2_CH1_BYT2[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[23:16]
0x1A	MIX2_CH1_BYT3[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[15:8]
0x1B	MIX2_CH1_BYT4[7:0]	0x00	Digital mixer 2, channel 1 coefficient byte[7:0]
0x1C	MIX2_CH2_BYT1[7:0]	0x7F	Digital mixer 2, channel 2 coefficient byte[31:24]
0x1D	MIX2_CH2_BYT2[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[23:16]
0x1E	MIX2_CH2_BYT3[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[15:8]
0x1F	MIX2_CH2_BYT4[7:0]	0xFF	Digital mixer 2, channel 2 coefficient byte[7:0]
0x48	IIR_N0_BYT1[7:0]	0x7F	Programmable first-order IIR, N0 coefficient byte[31:24]
0x49	IIR_N0_BYT2[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[23:16]
0x4A	IIR_N0_BYT3[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[15:8]
0x4B	IIR_N0_BYT4[7:0]	0xFF	Programmable first-order IIR, N0 coefficient byte[7:0]
0x4C	IIR_N1_BYT1[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[31:24]
0x4D	IIR_N1_BYT2[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[23:16]
0x4E	IIR_N1_BYT3[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[15:8]
0x4F	IIR_N1_BYT4[7:0]	0x00	Programmable first-order IIR, N1 coefficient byte[7:0]
0x50	IIR_D1_BYT1[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[31:24]
0x51	IIR_D1_BYT2[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[23:16]
0x52	IIR_D1_BYT3[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[15:8]
0x53	IIR_D1_BYT4[7:0]	0x00	Programmable first-order IIR, D1 coefficient byte[7:0]

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The PCM6020-Q1 is a stereo, automotive-qualified audio analog-to-digital converter (ADC) that supports output sample rates of up to 768 kHz. The PCM6020-Q1 supports up to two analog microphones for simultaneous recording applications. The PCM6020-Q1 is intended for automotive applications such as vehicle cabin active noise cancellation, hands-free in-vehicle communication, emergency call, and multi-media applications. This device integrates a host of features to reduce cost, board space, and power consumption in space-constrained automotive subsystem designs.

Communication to the PCM6020-Q1 for configuration of the control registers is supported using an I^2C or SPI interface. The device supports a highly flexible audio serial interface (TDM, I^2S, or LJ) to transmit audio data seamlessly in the system across devices.

9.2 Typical Applications

9.2.1 2-Channel Analog Microphone Recording Using the PCM6020-Q1

Figure 9-1 shows a typical configuration of the PCM6020-Q1 for an application using two analog microphones for simultaneous recording operation with an I^{2}C control interface and the TDM audio data slave interface.

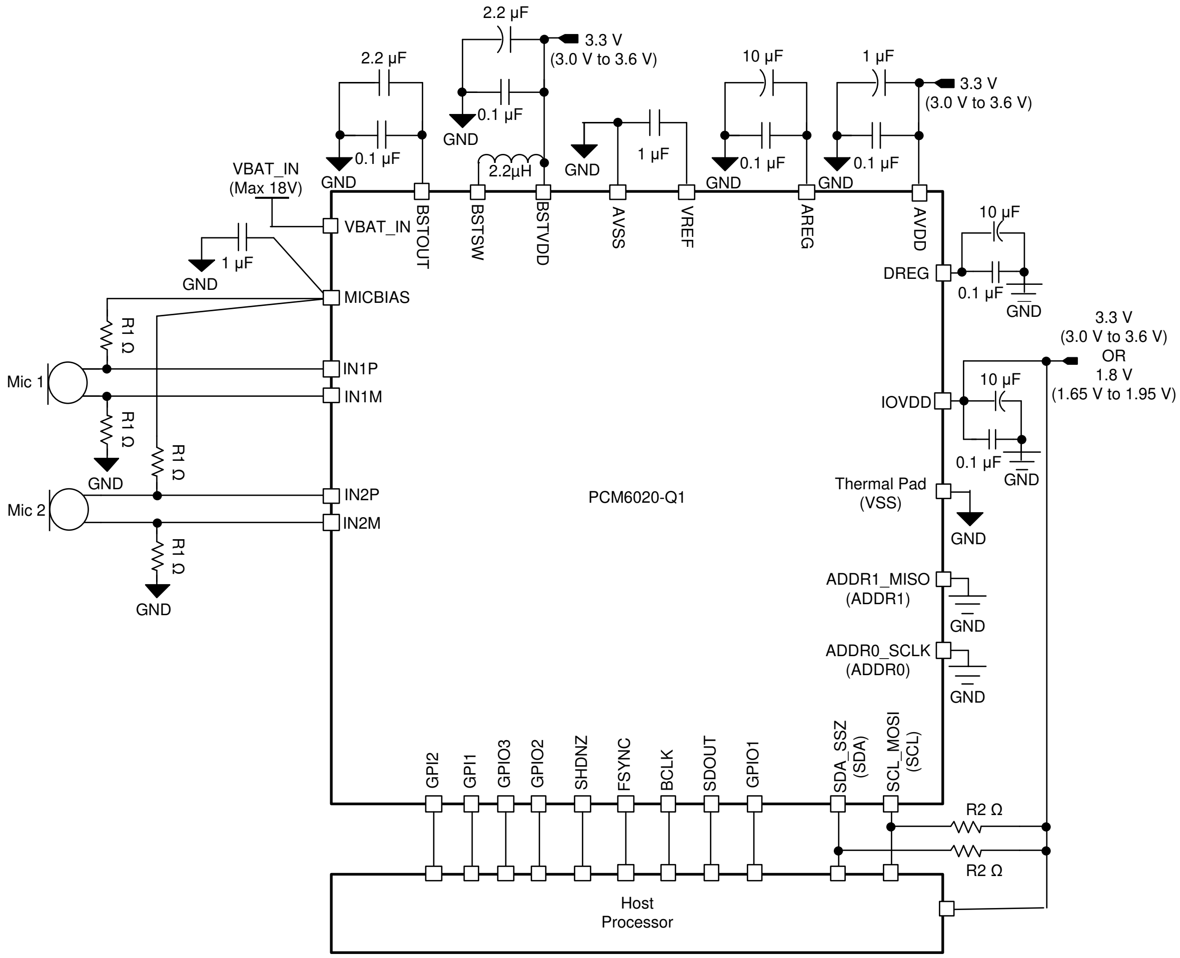


Figure 9-1. 2-Channel Analog Microphone Recording

9.2.1.1 Design Requirements

Table 9-1 lists the design parameters for this application.

Table 9-1. Design Parameters

KEY PARAMETER	SPECIFICATION
AVDD, BSTVDD	3.3 V
AVDD supply current	15 mA (PLL on, 2-channel record, f_S = 44.1 kHz)
IOVDD	1.8 V or 3.3 V
Maximum MICBIAS current	< 28 mA (MICBIAS voltage = 8 V, microphone impedance = 680 Ω and R1 = 340 Ω)

9.2.1.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM6020-Q1 for this specific application. The following steps give a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to other mode of operation.

1. **Apply power to the device:**
   a. Power up the IOVDD, AVDD, and BSTVDD power supplies, keeping the SHDNZ pin voltage low
   b. The device now goes into hardware shutdown mode (ultra-low-power mode < 1 µA)
2. **Transition from hardware shutdown mode to sleep mode (or software shutdown mode):**
   a. Release SHDNZ only when the IOVDD, AVDD, and BSTVDD power supplies settle to the steady-state operating voltage
   b. Wait for at least 1 ms to allow the device to initialize the internal registers
   c. The device now goes into sleep mode (low-power mode < 20 µA)
3. **Transition from sleep mode to active mode whenever required for the record operation:**
   a. Wake-up the device by writing P0_R2 to disable sleep mode
   b. Wait for at least 1ms to allow the device internal wake-up sequence to complete
   c. *Override the default configuration registers or programmable coefficients value as required (optional)*
   d. Enable all desired input channels by writing P0_R115
   e. Enable all desired audio serial interface output channels by writing P0_R116
   f. Power-up the ADC, MICBIAS, and PLL by writing P0_R117
   g. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a

      See the *Phase-Locked Loop (PLL) and Clock Generation* section for the supported sample rates and the BCLK to FSYNC ratio
   h. The device recording data are now sent to the host processor via the TDM audio serial data bus
   i. Wait for at least 10 ms to allow the MICBIAS to power up
   j. Enable the fault diagnostics for all desired input channels by writing P0_R100
4. **Transition from active mode to sleep mode (again) as required in the system low power:**
   a. Disable the fault diagnostics for all desired input channels by writing P0_R100
   b. Go to sleep mode by writing P0_R2 to enable sleep mode
   c. Wait at least 20 ms to allow the volume to gradually ramp down and for all blocks to power down
   d. Read P0_R119 to check the device shutdown and sleep mode status
   e. If the device P0_R119_D7 status bit is 1'b1, then stop FSYNC and BCLK in the system
   f. The device now goes into sleep mode (low-power mode < 20 µA) and retains all register values
5. **Transition from sleep mode to active mode (again) as required for the record operation:**
   a. Wake-up the device by writing P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device internal wake-up sequence to complete
   c. Apply FSYNC and BCLK with the desired output sample rates and BCLK to FSYNC ratio

   d. The device recording data are now sent to the host processor via the TDM audio serial data bus
   e. Wait for at least 10 ms to allow the MICBIAS to power up
   f. Enable the fault diagnostics for all desired input channels by writing P0_R100
6. **Repeat step 4 and step 5 as required for mode transitions**
7. **Assert the SHDNZ pin low to enter hardware shutdown mode (again) at any time**
8. **Follow step 2 onwards to exit hardware shutdown mode (again)**

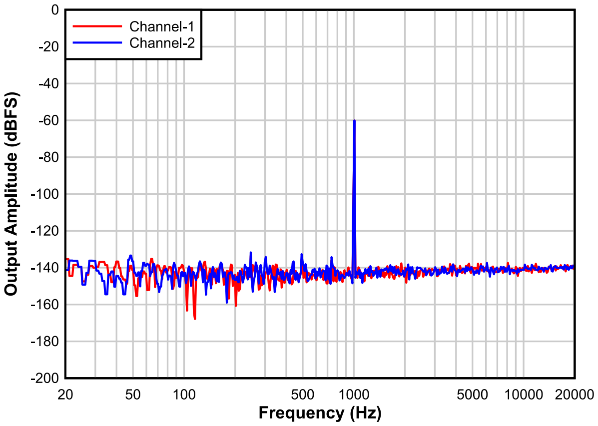
9.2.1.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I^{2}C register control script that shows how to set up the PCM6020-Q1 in a two-channel analog microphone record mode with differential inputs.

```
#
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the PCM6xx0-Q1 EVM user guide for key jumper settings and audio connections.
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# High swing mode enabled
# FSYNC = 44.1 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power up IOVDD, AVDD and BSTVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD, AVDD and BSTVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
#
# Wake-up device by I2C write into P0_R2 using internal AREG
w 90 02 81
#
# Powerdown MICBIAS and ADC channels on fault detection (overtemperature, and so forth)
w 90 28 10
#
# Configure channel 1 DC-coupled, differential microphone input with high-swing mode
w 90 3C 18
#
# Configure channel 2 DC-coupled, differential microphone input with high-swing mode
w 90 41 18
#
# Enable input channel 1 to channel 2 by I2C write into P0_R115
w 90 73 C0
#
# Enable ASI output channel 1 to channel 2 slots by I2C write into P0_R116
w 90 74 C0
#
# Power-up ADC,MICBIAS and PLL by I2C write into P0_R117
w 90 75 E0
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data by host on ASI bus with TDM protocol 32-bit channel word length
#
# Wait for 10 ms.
# Enable diagnostics for channel 1 to channel 2 by I2C write into P0_R100
w 90 64 C0
#
```

9.2.1.3 Application Curves

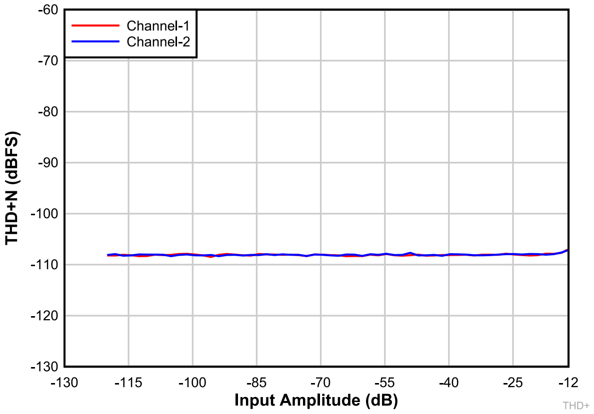
at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 44.1 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, channel gain = 0 dB, linear phase decimation filter, and MICBIAS programmed voltage = 8 V (unless otherwise noted); all measurements are done on the EVM with a 20-kHz, low-pass filter and an A-weighted filter (unless otherwise noted)



EVM_MIC_FFT_m60dB.grf

DC-coupled differential microphone input with DC common-mode 1NxP = ~6 V and INxM = ~2 V, high swing mode enabled, measured using an external audio input source

Figure 9-2. FFT With a –60-dBr Input (non A-weighted)



EVM_MIC_THDN_VS_AMPL.grf

DC-coupled differential microphone input with DC common-mode 1NxP = ~6 V and INxM = ~2 V, high swing mode enabled, measured using an external audio input source

Figure 9-3. THD+N vs Input Amplitude

9.3 What To Do and What Not To Do

In master mode operation with I^2S or LJ format, the device generates FSYNC half a cycle earlier than the normal protocol timing behavior expected. This timing behavior can still function for most of the system, however for further details and a suggested workaround for this weakness, see the *Configuring and Operating the PCM6xx0-Q1 as an Audio Bus Master* application report.

The automatic gain controller (AGC) feature has some limitation when using sampling rates lower than 44.1 kHz. For further details about this limitation, see the *Using the Automatic Gain Controller (AGC) in PCM6xx0-Q1* application report.

For I^2C operation, if the ADDR0_SCLK pin is tied high, then the I^2C bus must remain idle (which means the SDA_SSZ and SCL_MOSI pins must be high) when the SHDNZ pin is released from low to high.

10 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, keep the SHDNZ pin low until the IOVDD supply voltage settles to a stable and supported operating voltage range. After the IOVDD and AVDD supplies are stable, set the SHDNZ pin high to initialize the device. BSTVDD can be either applied along with AVDD or later but before turning on the MICBIAS. Figure 10-1 shows the power-supply sequencing requirements.

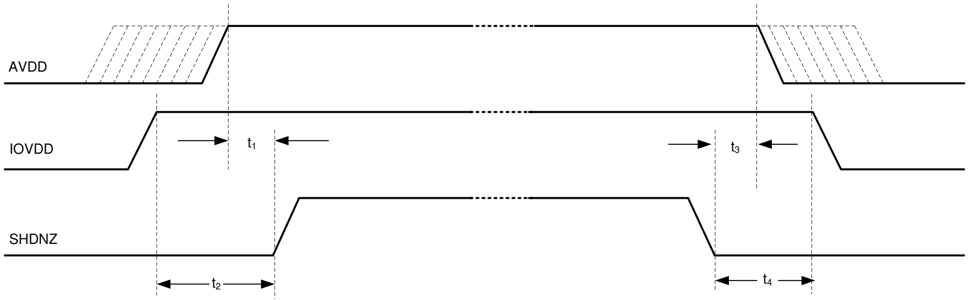


Figure 10-1. Power-Supply Sequencing Requirement

For the supply power-up requirement, t_1 and t_2 must be at least 100 µs. For the supply power-down requirement, t_3 and t_4 must be at least 10 ms. This time allows the device to ramp down the volume on the record data, and power down the analog and digital blocks, and lastly put the device into hardware shutdown mode. The device can also be immediately put into hardware shutdown mode from active mode if SHDNZ_CFG[1:0] is set to 2'b00 using the P0_R5_D[3:2] bits. In that case, t_3 and t_4 are required to be at least 100 µs.

Make sure that the supply ramp rate is slower than 1 V/µs and that the wait time between a power-down and a power-up event is at least 100 ms. For a supply ramp rate slower than 0.1 V/ms, the host device must apply a software reset as the first transaction before configuring the device.

After the releasing SHDNZ, or after a software reset, delay any additional I^2C or SPI transactions to the device for at least 2 ms to allow the device to initialize the internal registers. See the *Device Functional Modes* section to operate the device in various modes after the device power supplies are settled to the recommended operating voltage levels.

11 Layout

11.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- The supply decoupling capacitors used must be of a ceramic type with low ESR.
- The boost converter inductor and decoupling capacitors for the power supplies must be placed close to the device pins.
- Route analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to avoid undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply for multiple microphones to avoid coupling across microphones.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use MICBIAS and BSTOUT capacitors with a high voltage rating (> 25V) to support higher voltage MICBIAS operation.
- An external circuit must be used to suppress or filter the amount of high-frequency electromagnetic interference (EMI) noise found in the microphone input path resulting from long cables (if used) in the system.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

11.2 Layout Example

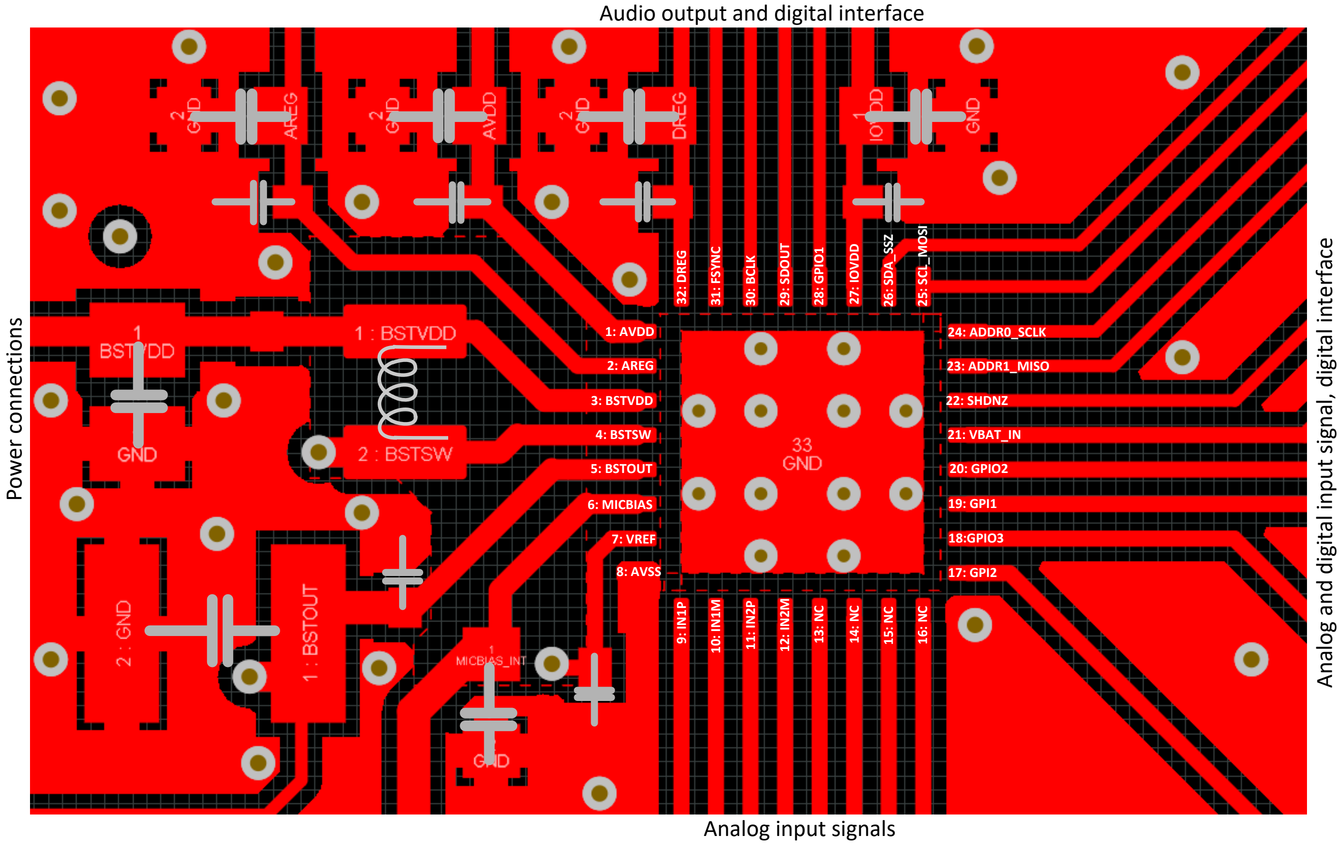


Figure 11-1. Layout Example of the PCM6020-Q1

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

PurePath™ console graphical development suite

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Multiple PCM6xx0-Q1 Devices With Shared TDM and I^2C Bus* application report
- Texas Instruments, *PCM6xx0-Q1 Programmable Biquad Filter Configuration and Applications* application report
- Texas Instruments, *PCM6xx0-Q1 Sampling Rates and Programmable Processing Blocks Supported* application report
- Texas Instruments, *PCM6xx0-Q1 Integrated Analog Anti-Aliasing Filter and Flexible Digital Filter* application report
- Texas Instruments, *Configuring and Operating TLV320ADCx140 as Audio Bus Master* application report
- Texas Instruments, *Using the Automatic Gain Controller in PCM6xx0-Q1* application report
- Texas Instruments, *PCM6xx0-Q1 Fault Diagnostics Features* application report
- Texas Instruments, *Scalable Automotive Audio Solutions Using the PCM6xx0-Q1 Family of Products* application report
- Texas Instruments, *PCM6xx0-Q1 Use-Case Scenarios in Automotive Audio Applications* application report
- Texas Instruments, *PCM6xx0-Q1 AC-Coupled External Resistor Calculator*
- Texas Instruments, *PCM6xx0-Q1 SIMULATION IBIS Models*
- Texas Instruments, *PCM6xx0Q1EVM-PDK Evaluation Module* user's guide
- Texas Instruments, *PurePath™ Console Graphical Development Suite for Audio System Design and Development* development suite

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

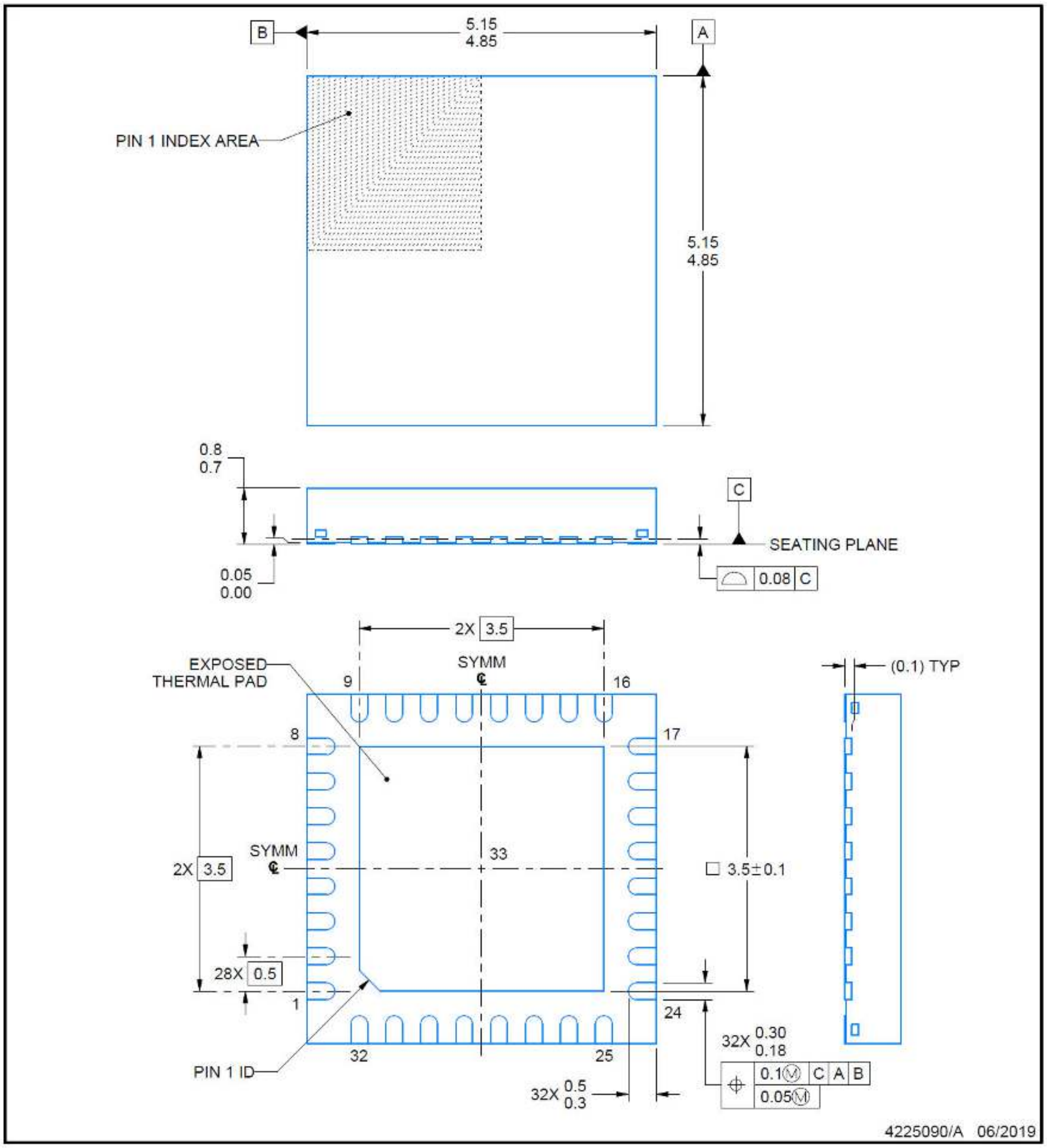
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RTV0032T

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

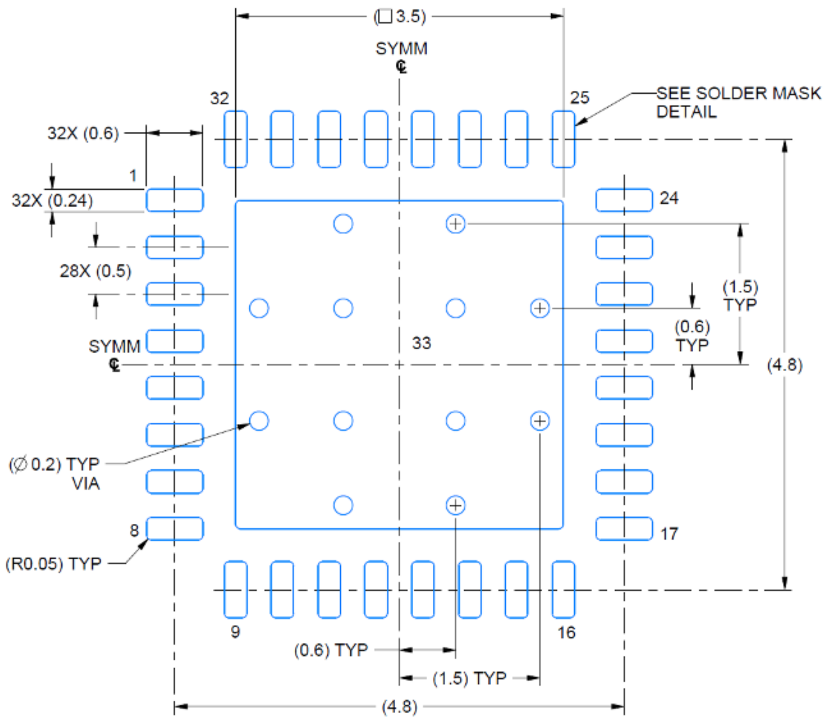
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

www.ti.com

EXAMPLE BOARD LAYOUT

RTV0032T **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225090/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

TEXAS INSTRUMENTS
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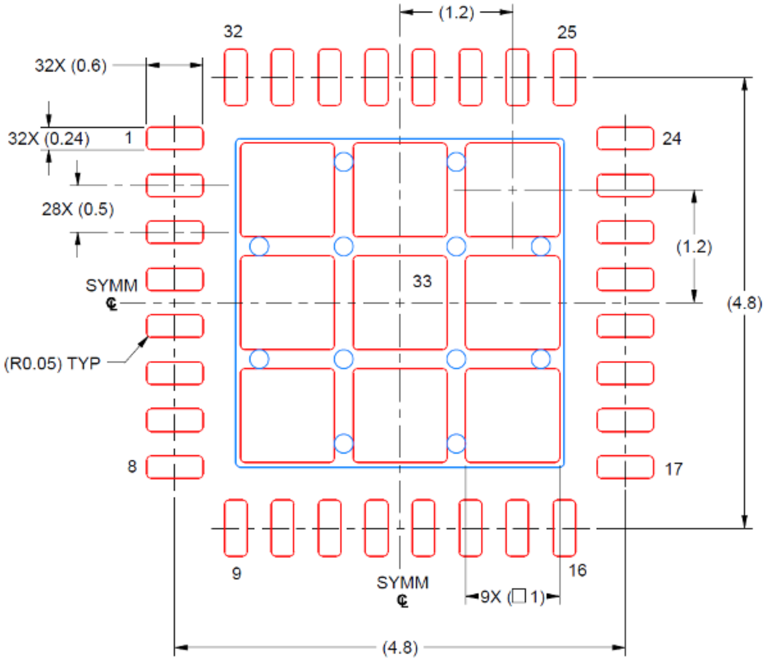
EXAMPLE STENCIL DESIGN

RTV0032T

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 33
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225090/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM6020QRTVRQ1	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM6020	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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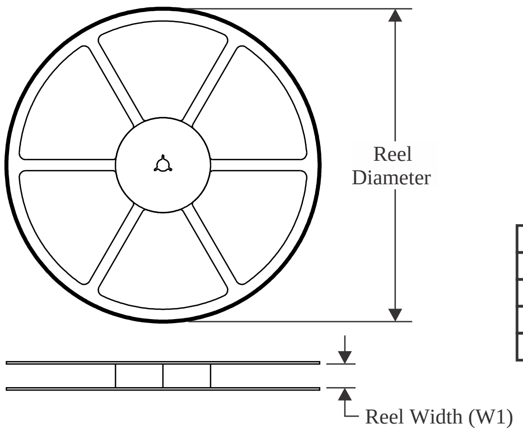
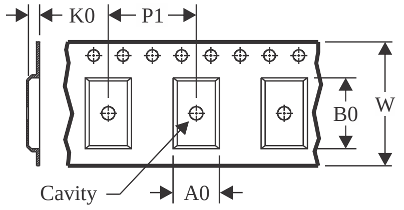
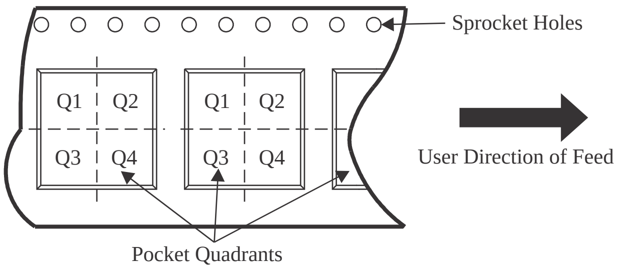
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

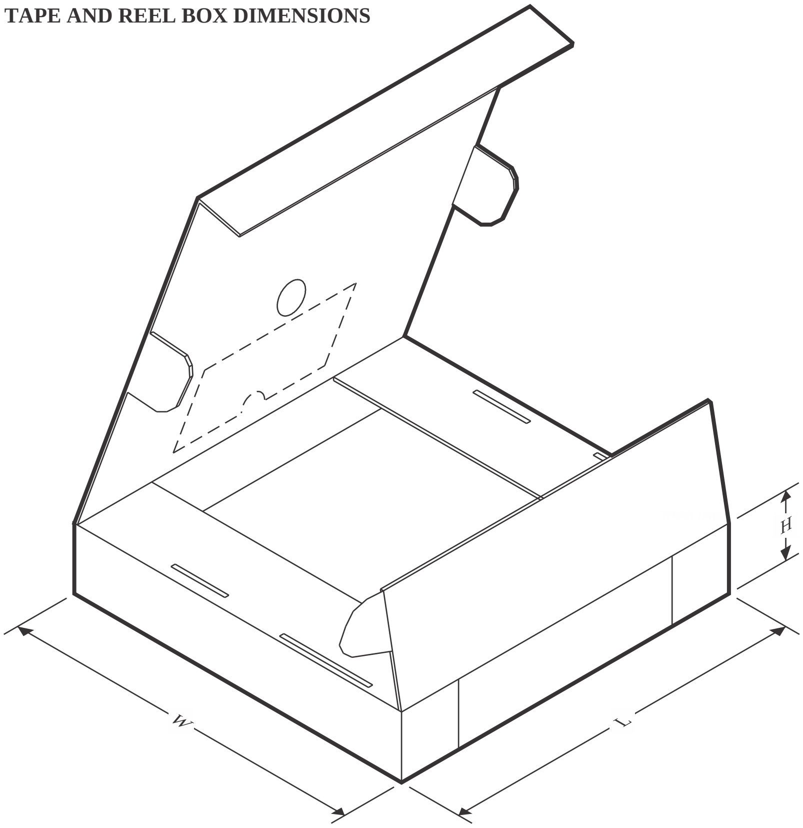
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM6020QRTVRQ1	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

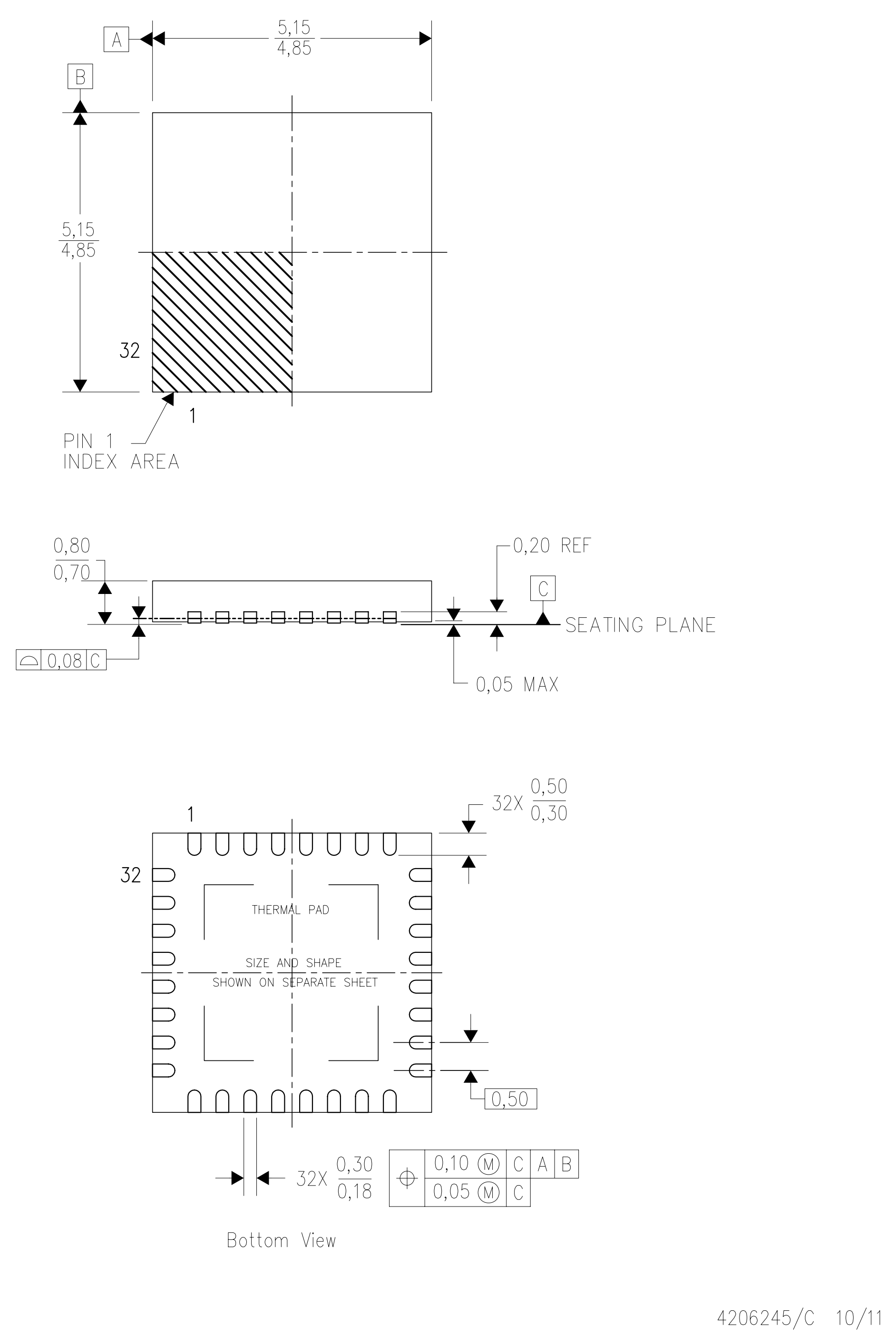
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM6020QRTVRQ1	WQFN	RTV	32	3000	367.0	367.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

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