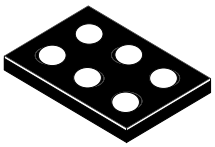
ST1S15

500 mA, 6 MHz synchronous step-down converter

Datasheet - production data



Flip Chip 6

Features

- 85% typical efficiency
- 500 mA output current capability
- 45 µA typical quiescent current
- PFM or PWM operation for best efficiency over whole load range
- Ultra-fast load and line transient
- Short-circuit and thermal protection
- Small external components
- Auto or forced PWM selection with dedicated pin
- Available in Flip Chip 6 package

Applications

- DSP and multimedia processor core supply
- Cell phones
- PDAs

Description

The ST1S15 is a high efficiency miniaturized step-down converter able to provide 500 mA output current from an input voltage from 2.3 V to 5.5 V. This converter is specifically designed for applications where high efficiency and small application area are the key factors. Thanks to 6 MHz switching frequency, the ST1S15 can use 470 nH nominal values for the inductor and 4.7 µF for the output capacitor providing, at the same time, very good performance in terms of load and line transients. A PFM mode can be selected for high efficiency under light load conditions or PWM mode for tight regulation and best dynamic performance. Short-circuit and thermal protection are also included.

Table 1: Device summary

Order code	Output voltage (V)	Package
ST1S15J18R	1.82	Flip Chip 6

This is information on a product in full production.

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1 Application schematic

Figure 1: ST1S15 application schematic

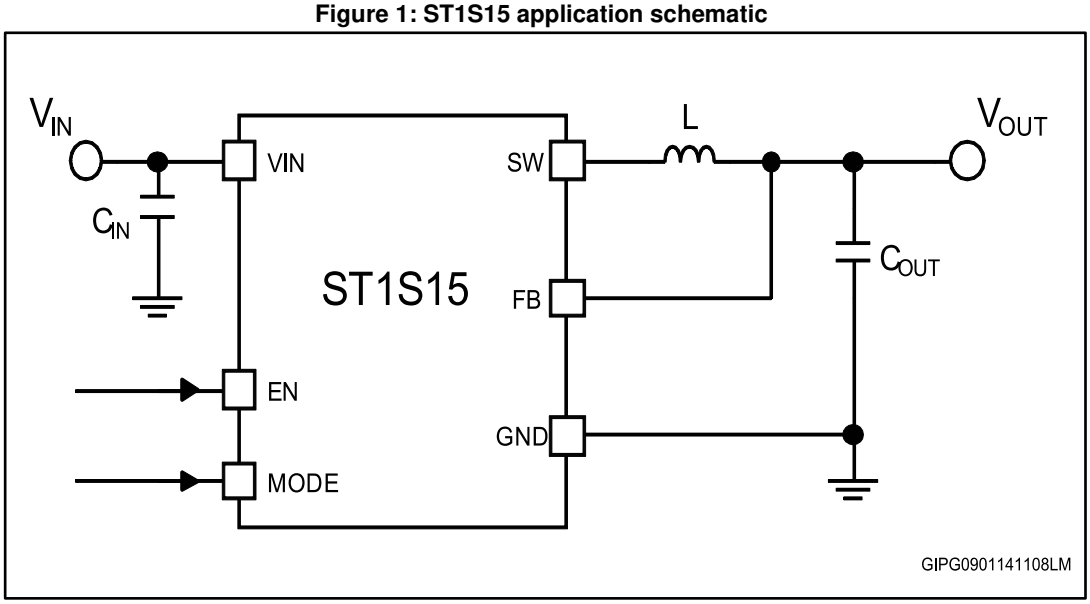


Table 2: Typical external components

Component	Manufacturer	Part number	Value	Size
C_{IN}	Murata	GRM155R60J475ME87	4.7 µF	0402
C_{OUT}		GRM155R60G475ME87 (1)		
		GRM155R60J475ME87		
L		LQM21PNR47MC0D	470 nH	2.0 x 1.25 x 0.5 mm

Notes:

(1) $V_{OUT} \leq 1.82$ V

All the above components refer to a typical application. The ST1S15 operation is not limited to the choice of these external components.

2 Pin configuration

Figure 2: Pin connections (top view)

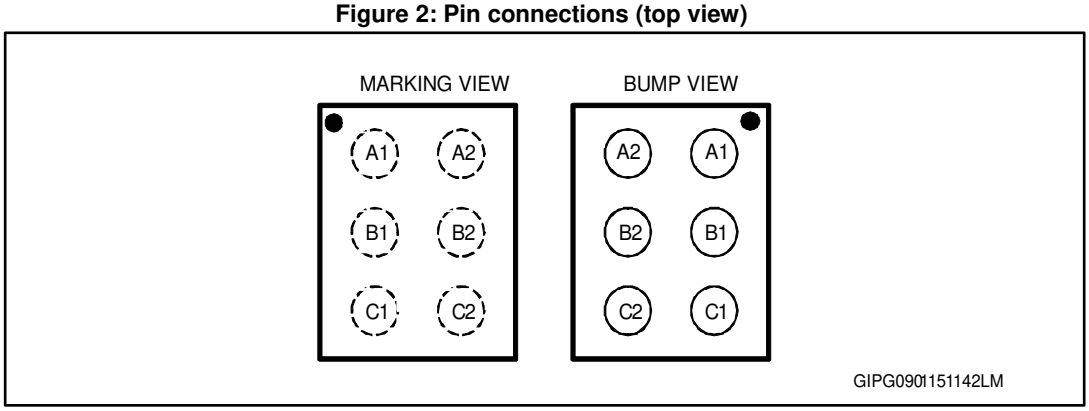


Table 3: Pin description

Pin	Flip Chip	Description
V_{IN}	A2	High-side switch connection and IC supply.
EN	B2	ENABLE pin with positive logic. The IC shuts down if pulled low. Do not leave this pin floating.
GND	C2	Power and IC supply ground.
FB	C1	Feedback input.
SW	B1	Inductor connection to internal PFET and NFET.
MODE	A1	Operation mode selection: LOW = automatic operation PFM or PWM according to output load. HIGH = forced PWM operation. Do not leave this pin floating.

3 Maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power and signal supply voltage	- 0.3 to + 6.0	V
EN, MODE	Logic input pins	- 0.3 to + 6.0	V
FB, SW	Feedback and switching pins	-0.3 to V_{IN} + 0.3	V
T_{AMB}	Operating ambient temperature	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5: Thermal data

Symbol	Parameter	Flip Chip	Unit
R_{thJA}	Thermal resistance junction-ambient	130	°C/W

Table 6: ESD performance

Symbol	Parameter	Flip Chip	Unit
ESD	Human body model	±2000	V
	Machine model	±100	

4 Electrical characteristics

- 40 °C < T_A < 85 °C, C_{IN} = 4.7 µF nominal, C_{OUT} = 4.7 µF nominal, L = 470 nH, typical values are at T_A = 25 °C, V_{EN} = V_{IN} unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Operating input voltage range		2.3		5.5	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising		2.1	2.2	V
		V_{IN} falling	1.8	1.9		
I_Q	PFM mode quiescent current	No load		45	60	µA
	PWM mode quiescent current	No load		15		mA
	Shutdown current	V_{EN} = 0		0.5	5	µA
f_{SW}	Switching frequency		5.4	6	6.6	MHz
I_{OUT}	Continuous output current (1)	V_{IN} ≥ V_{OUT} + 0.40 V	500			mA
I_{SC}	Short-circuit current (2)				1200	mA
$I_{PFM-PWM}$	PFM to PWM transition	V_{IN} = 3.6 V, V_{OUT} = 1.82 V		200		mA
	PWM to PFM transition			100		
h	Efficiency (V_{IN} = 3.6 V, V_{OUT} = 1.82 V)	I_{OUT} = 10 mA PFM mode		80		%
		I_{OUT} = 150 mA		83		
t_{ON}	Start-up time	V_{EN} from low to high, V_{IN} = 3.6 V, V_{OUT} = 1.82 V		260		µs
T_{SHDN}	Thermal shutdown			125		°C
	Hysteresis			30		°C
Output voltage						
V_{OUT}	Accuracy (ST1S15J18)	2.3 ≤ V_{IN} ≤ 5.5 V, I_{OUT}= 10 mA, PWM mode, -40 ≤ T_A ≤ 85 °C	1.78	1.82	1.86	V
		2.3 ≤ V_{IN} ≤ 5.5 V, I_{OUT}= 10 mA, PFM mode, -40 ≤ T_A ≤ 85 °C	1.78	1.82	1.86	
	Load regulation	2.3 ≤ V_{IN} ≤ 5.5 V, V_{OUT}=1.82 V, I_{OUT} = 0 to 500 mA, PWM mode, -40 ≤ T_A ≤ 85 °C		-1.5		%
V_{OUT_Ripple}	Peak-to-peak output voltage ripple	PWM mode, I_{OUT} = 150 mA, V_{IN} = 3.6 V, V_{OUT} = 1.82 V		10		mV
		PFM mode, I_{OUT} = 150 mA, V_{IN} = 3.6 V, V_{OUT} = 1.82 V		30		mV
I_{LKFB}	FB pin leakage current	V_{FB} = 5.5 V			9	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN_TR}	Line transient response. Output voltage variation over the nominal DC level $t_R = t_F = 10$ µs case 1: $V_{IN} = 2.5$ to 3.1 V case 2: $V_{IN} = 3.9$ to 4.5 V	$I_{OUT} = 50$ mA, $V_{OUT} = 1.82$ V		±50		mV
		$I_{OUT} = 250$ mA, $V_{OUT} = 1.82$ V				
I_{OUT_TR}	Load transient response $t_R = t_F = 0.1$ µs case 1: $V_{IN} = 2.5$ V case 2: $V_{IN} = 3.6$ V case 3: $V_{IN} = 4.5$ V	$I_{OUT} = 0$ to 150 mA, $V_{OUT} = 1.82$ V		±50		mV
		$I_{OUT} = 50$ to 250 mA, $V_{OUT} = 1.82$ V		±70		
		$I_{OUT} = 150$ to 400 mA, $V_{OUT} = 1.82$ V		±70		
Logic inputs						
V_{IL}	Low-level input voltage (EN, MODE pins)				0.4	V
V_{IH}	High-level input voltage (EN, MODE pins)		1.2			V
I_{LK-I}	Input leakage current (EN, MODE pins)	$V_{EN} = V_{MODE} = 5.5$ V		0.01	1	µA
Power switches						
$R_{DS(on)}$	P-channel MOSFET on-resistance			300	400	mΩ
	N-channel MOSFET on-resistance			350	450	
I_{LPEAK}	P-channel peak current limit	Over the input voltage range	900	1000	1200	mA
I_{LKG-P}	P-channel leakage current	$V_{IN} = 5.5$ V, $V_{EN} = 0$			1	µA
I_{LKG-N}	N-channel leakage current	$V_{SW} = 5.5$ V, $V_{EN} = 0$			1	µA

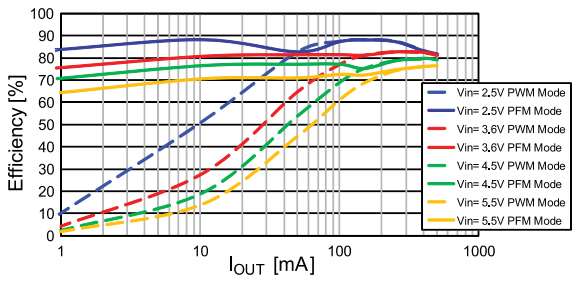
Notes:

(1)Not tested in production. This value is guaranteed by correlation with $R_{DS(on)}$, peak current limit and operating input voltage.

(2)Not tested in production. This parameter is guaranteed by peak current limit.

5 Typical performance characteristics

Figure 3: Efficiency vs. output current (V_{OUT} = 1.82 V)



$V_{EN}=V_{IN}$ I_{OUT} =1 mA to 500 mA

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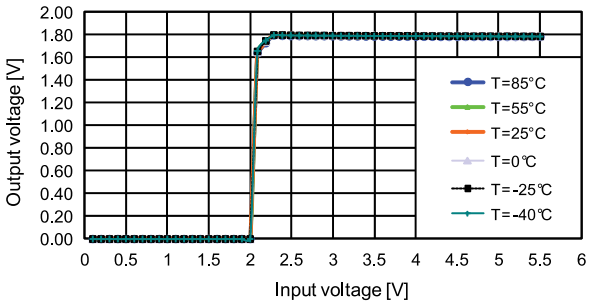
Figure 4: Output voltage vs. input voltage



V_{IN} = 0 to 5.5 V (step 0.1 V), I_{OUT} = 500 mA, Mode = GND, VEN = VIN

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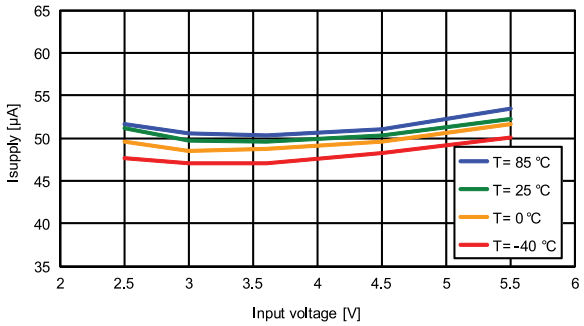
Figure 5: Supply current vs. input voltage in auto mode



VIN = 2.5 V to 5.5 V, mode = GND, VOUT = 1.82 V, VEN = VIN

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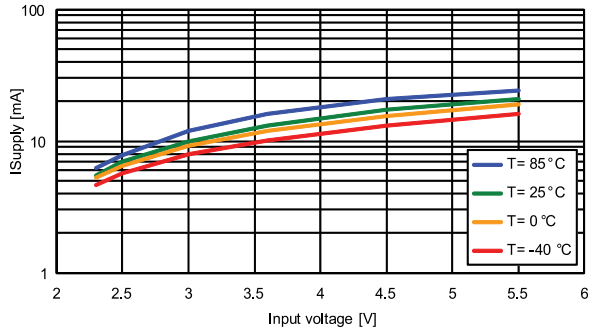
Figure 6: Supply current vs. input voltage in PWM mode



VIN = 2.3 V to 5.5 V, mode = VIN, VOUT = 1.82 V, VEN = VIN

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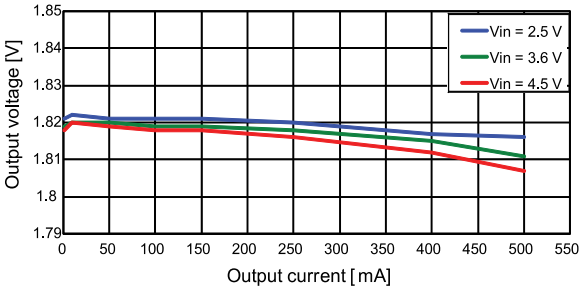
Figure 7: Output voltage vs. output current



VEN = VIN, mode = VIN, VOUT = 1.82 V

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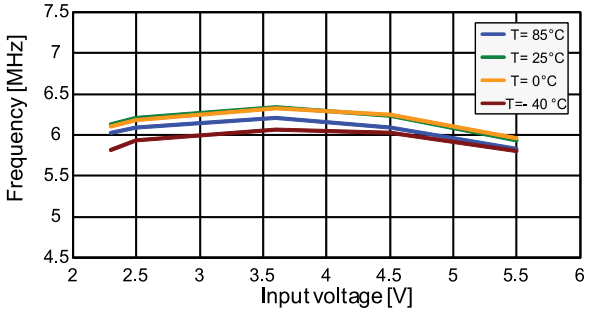
Figure 8: Frequency vs. input voltage



VIN = 2.3 V to 5.5 V, IOUT = 10 mA, Mode = VIN, VEN = VIN

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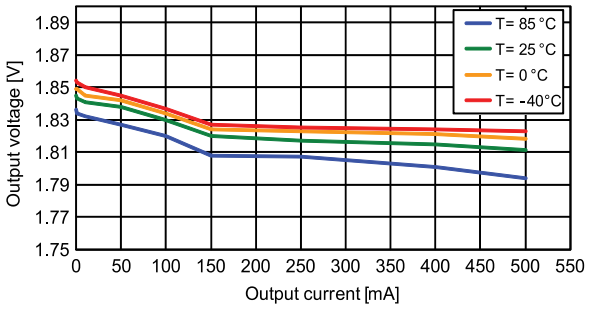
Figure 9: Output voltage vs. output current V_{IN}=3.6 V



VIN = 2.3 V to 5.5 V, IOUT = 10 mA,
Mode = VIN, VEN = VIN

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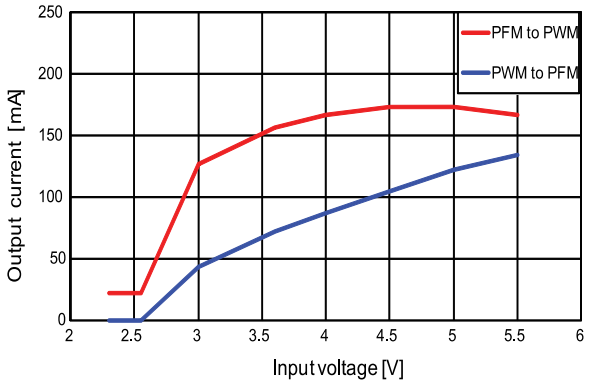
Figure 10: Mode transition vs. input voltage



VIN = enable, VOUT = 1.82 V, mode = GND

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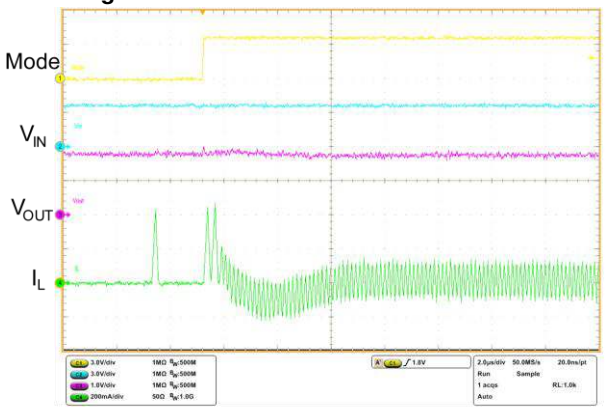
Figure 11: Mode transition PFM to PWM



VIN = 3.6 V, VOUT = 1.82 V, mode = 0 to 3.6 V, load = 180 Ω

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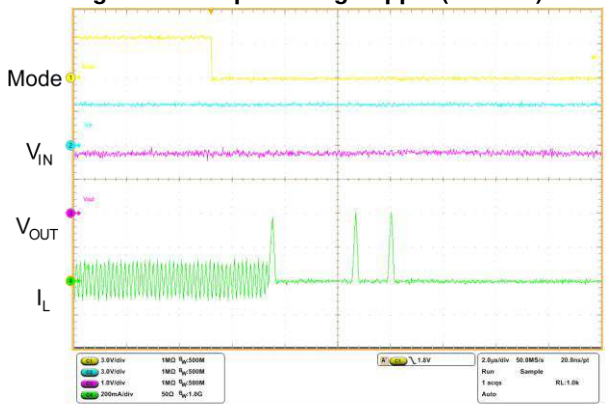
Figure 12: Output voltage ripple (no-load)



VIN = 3.6 V, VOUT = 1.82 V, mode = 3.6 to 0 V, load = 180 Ω

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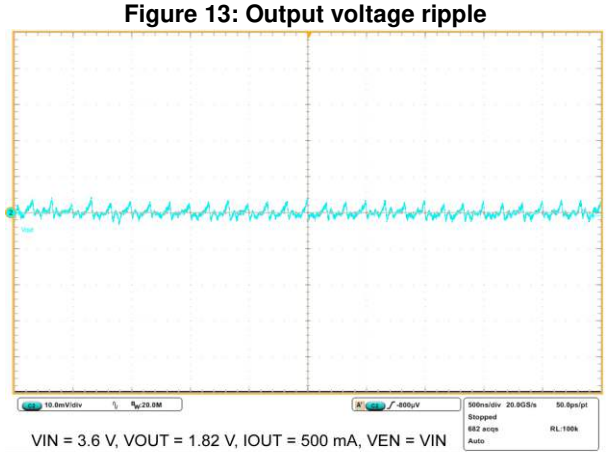
Figure 13: Output voltage ripple



VIN = 3.6 V, VOUT = 1.82 V, IOUT = 500 mA, VEN = VIN

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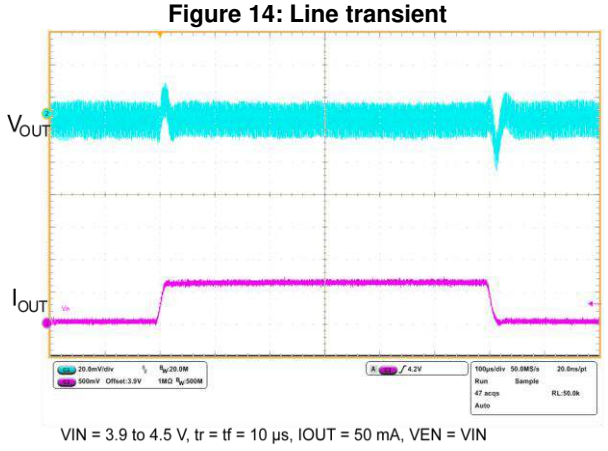
Figure 14: Line transient



VIN = 3.9 to 4.5 V, tr = tf = 10 µs, IOUT = 50 mA, VEN = VIN

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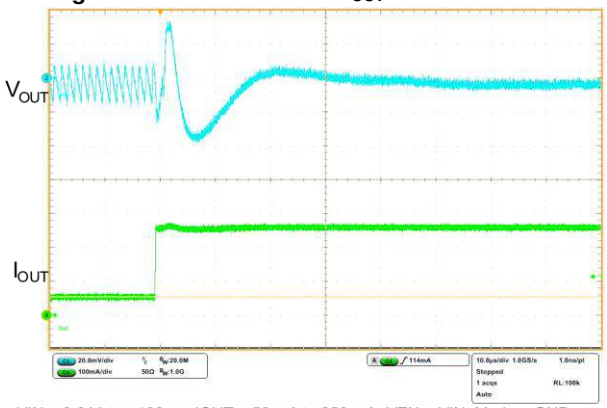
Figure 15: Load transient I_{OUT} = 50 to 250 mA



VIN = 3.6 V, tr = 100 ns, IOUT = 50 mA to 250 mA, VEN = VIN, Mode = GND

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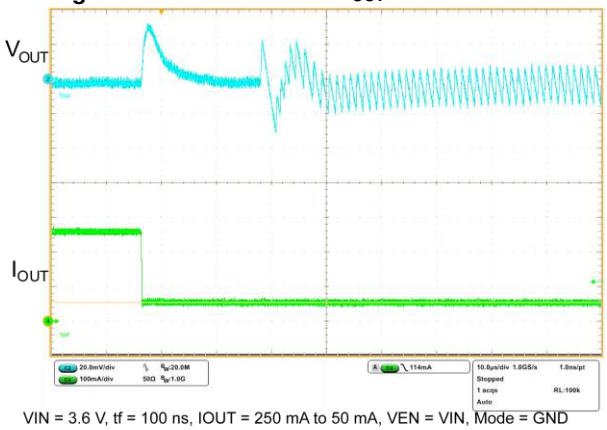
Figure 16: Load transient I_{OUT} = 250 to 50 mA



VIN = 3.6 V, tf = 100 ns, IOUT = 250 mA to 50 mA, VEN = VIN, Mode = GND

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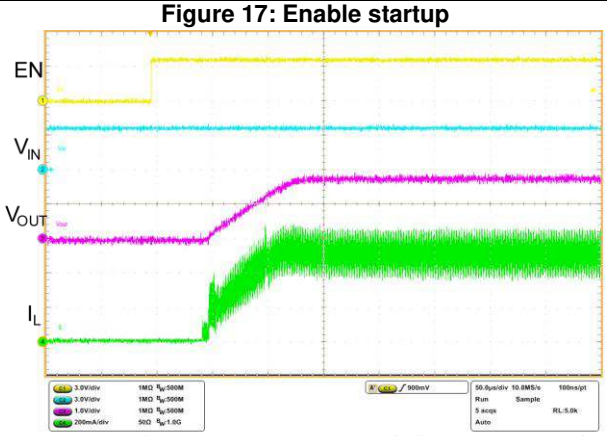
Figure 17: Enable startup



VIN = 3.6 V, Enable = 0 to 3.6 V, Mode = VIN, VOUT = 1.82 V, Load = 3.6 Ω

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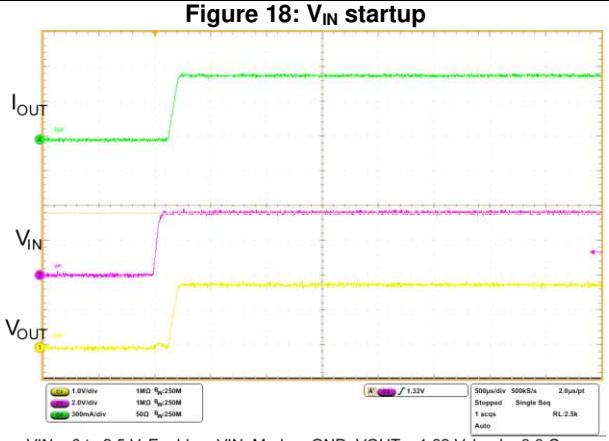
Figure 18: V_{IN} startup



VIN = 0 to 2.5 V, Enable = VIN, Mode = GND, VOUT = 1.82 V, load = 3.3 Ω

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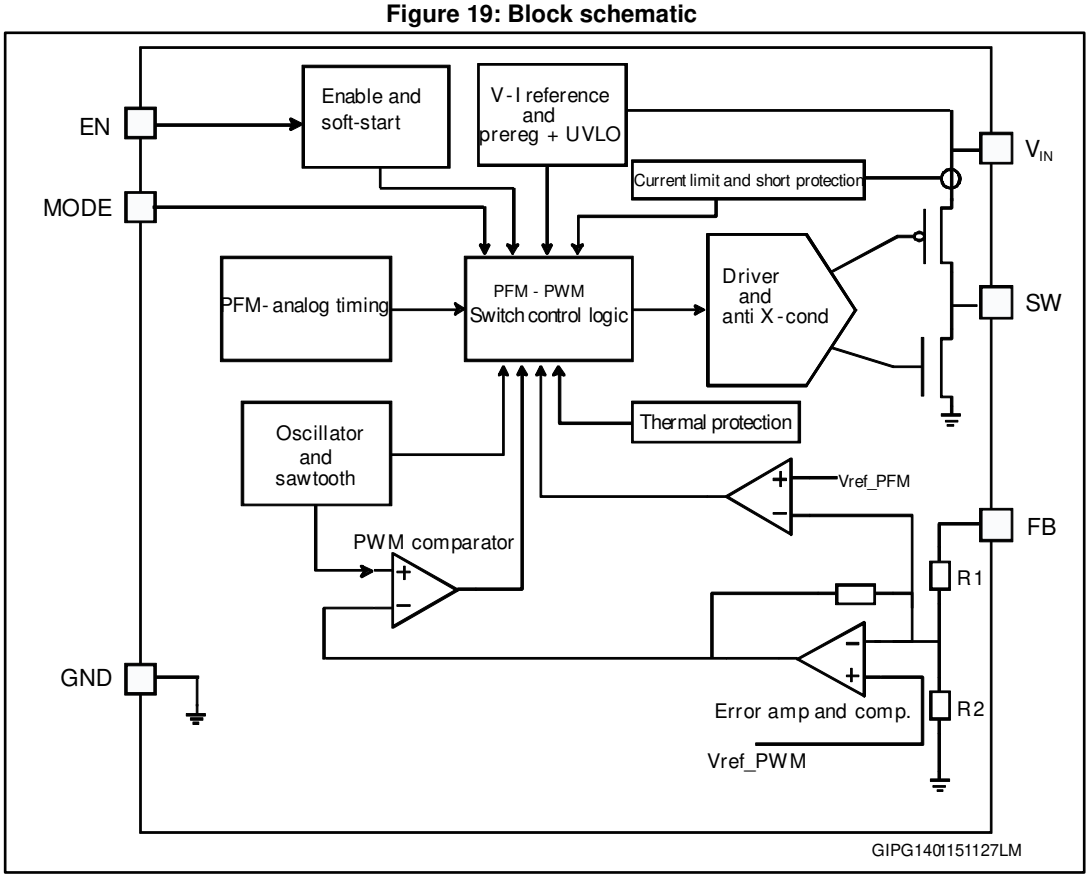
6 Block schematic

Figure 19: Block schematic



7 Detailed description

7.1 General description

The ST1S15 is a fixed voltage mode PWM step-down DC-DC converter, which operates with typically 6 MHz fixed frequency pulse width modulation (PWM) at moderate and heavy load currents. At light load currents the converter can automatically enter PFM (pulse frequency mode) mode.

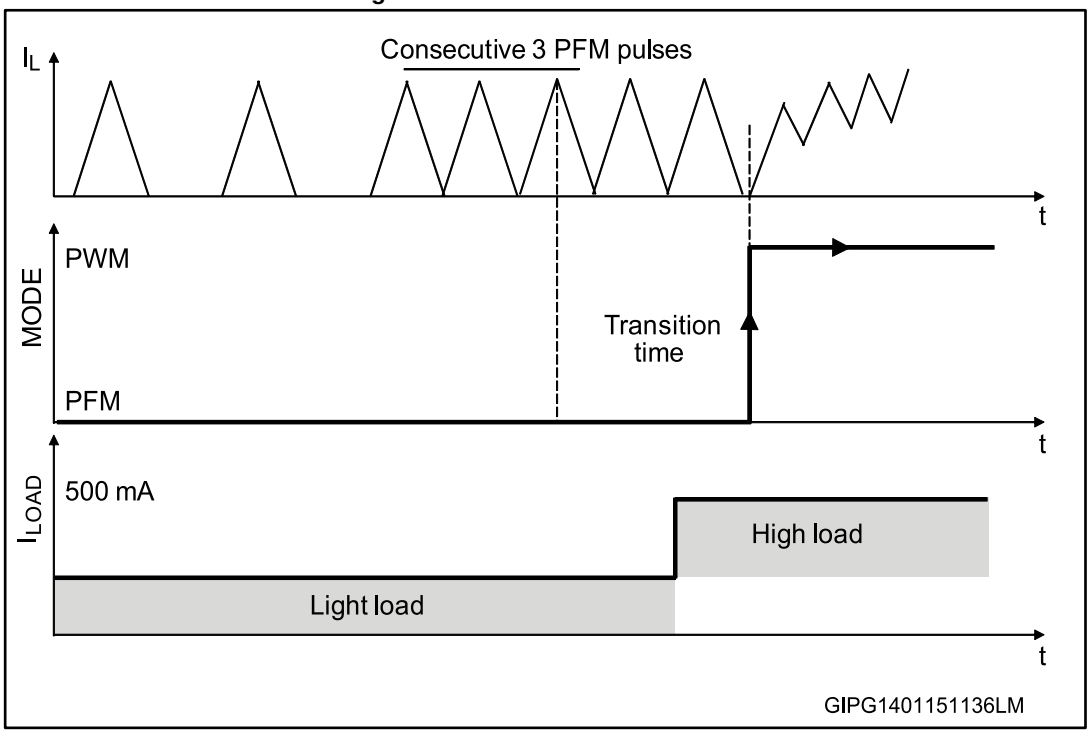
Few components are required: an inductor and two capacitors. It can work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These kinds of capacitors, thanks to their very low series resistance (ESR), minimize the output voltage ripple. In addition, the chosen inductor must not saturate at the peak current level.

7.2 Mode transition

The ST1S15 can work in PWM mode or in PFM mode according to the different operating conditions. If the MODE pin is pulled high, the device works in PWM mode only even at light or no-load. If the MODE pin is low, the operation changes according to the average input current handled by the device. At low output current the device works in PFM mode so to obtain very low power consumption and very good efficiency. When the output current increases, the device automatically switches to PWM mode in order to deliver the power needed by the load.

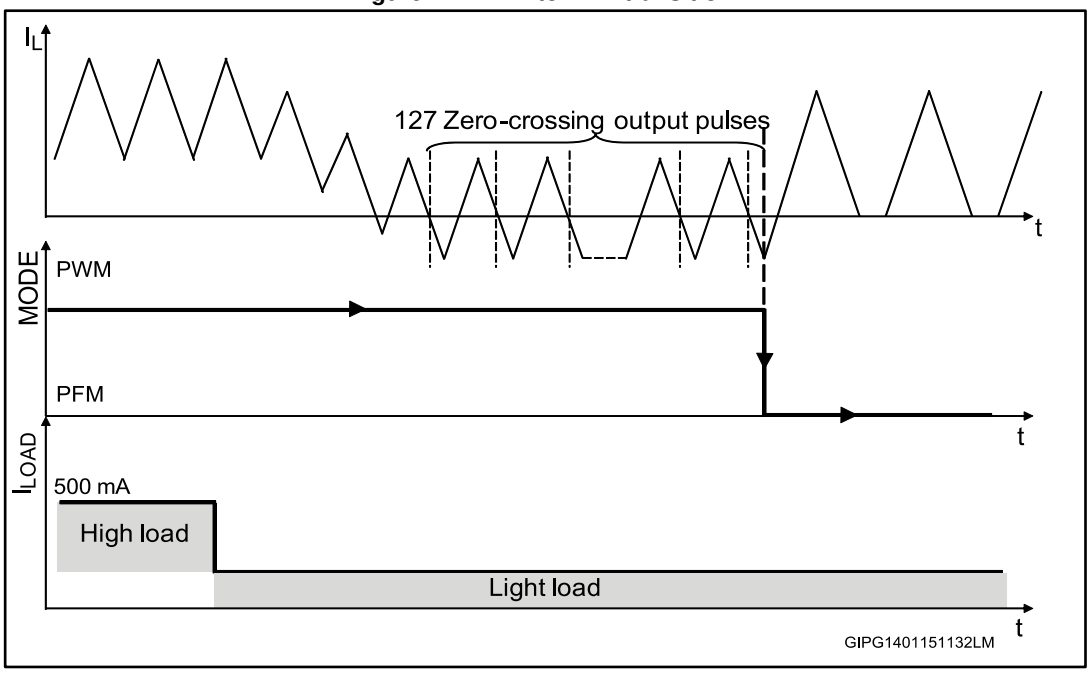
The ST1S15 passes from PFM to PWM when 3 consecutive PFM pulses occur. This means that the PFM has reached its maximum current capability and the device needs to go into PWM mode. The whole PWM circuitry starts after a transition time. During this time the duration of the PFM pulses rises about 350 ns so to provide higher current capability. After the PWM circuitry startup, the ST1S15 switches to PWM operation.

Figure 20: PFM to PWM transition



The transition from PWM to PFM mode occurs when the load current decreases and the coil current becomes negative. After the zero-crossing output goes up for 127 consecutive times the device switches to PFM mode.

Figure 21: PWM to PFM transition



7.3 Soft-start

The internal soft-start is enabled after V_{IN} reaches the UVLO threshold and the EN pin is high or for startup after enable. An overtemperature shutdown event or over short-circuit event also activates the soft-start sequence.

It eliminates the in-rush current problem during the start-up phase. During the soft-start the device always works in PWM regardless of the status of the MODE pin.

7.4 Short-circuit protection

The short-circuit protection begins when there is a short between the device output and ground. In this case the output voltage value is lower than the voltage reference and the overcurrent protection comparator output is high.

When this happens the power stage (P-channel and N-channel) turns off and a soft-start phase starts. The device repeats the soft-start sequence during the short-circuit condition.

7.5 Undervoltage lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning when the input voltage is not high enough. The device is in shutdown mode, when the input voltage is below the UVLO threshold. The hysteresis of 200 mV prevents unstable operation when the input voltage is close to the UVLO threshold.

7.6 Thermal protection

The device also has thermal shutdown protection, which is active when the junction temperature reaches 125 °C. In this case both the high and low-side MOSFETs turn off. Once the junction temperature goes back below 95 °C, the device resumes normal operation.

7.7 Overcurrent protection

The overcurrent protection limits the maximum inductor current. This current, flowing through the P-channel of the power stage, causes a voltage drop, across its $R_{DS(on)}$, at the switching node. A comparator compares the switching node voltage with a reference voltage VR. To generate the VR voltage a current generator is used, which causes a drop across a P-channel of the same kind as the power stage. When the switching node voltage is lower than VR, the comparator output goes high and the power P-channel turns off.

7.8 Enable function

The ST1S15 features an enable function (B2). When the EN voltage is higher than 1.2 V the device is ON, and if it is lower than 0.4 V the device is OFF. In shutdown mode the consumption is lower than 5 µA. The EN pin does not have an internal pull-up, which means that the EN pin cannot be left floating. If the enable function is not used, the EN pin must be connected to V_{IN}.

8 Application information

8.1 Input and output capacitors

Ceramic capacitors with X5R or X7R dielectric and low ESR should be used. The input capacitor filters any disturbance present in the input line so to obtain a stable operation. The output capacitor satisfies the output voltage ripple requirement. The output voltage ripple (V_{OUT_RIPPLE}), in continuous mode, is calculated as follows:

Equation 1

$$V_{OUT_RIPPLE} = \Delta I_L \times \left[ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right] + \frac{V_{IN} \times ESL}{L}$$

where ΔI_L is the ripple current and f_{SW} is the switching frequency. The use of ceramic capacitors with voltage ratings higher than 1.5 times the maximum input or output voltage is recommended.

8.2 Inductor

The inductor is the key passive component for switching converters. The internal compensation is optimized to operate with an output filter of L=0.47 µH and C_{OUT}=4.7 µF. In addition to the inductance value, in order to avoid saturation, the maximum saturation current of the inductor must be higher than I_{PEAK}.

The peak current of the inductor has to be calculated as follows:

Equation 2

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN_MAX} - V_{OUT})}{2 \times V_{IN_MAX} \times f_{SW} \times L}$$

The following inductor part numbers from different suppliers have been tested in the ST1S15 converters.

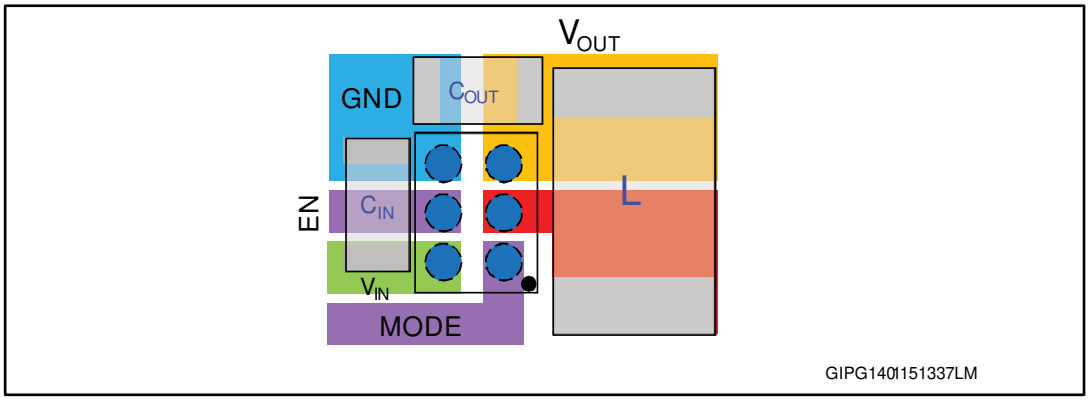
Table 8: Inductors

Manufacturer	Part numbers	Dimension (mm)
Murata	LQM21PNR47MC0D	2.0 x 1.25 x 0.5
	LQM21PNR54MG0D	2.0 x 1.25 x 0.5
	LQH32PNR47NN0L	3.2 x 2.7 x 1.55
TDK	MLP2012SR47T	2.0 x 1.25 x 0.5
	VLS2010ET-1R0N	2.0 x 2.0 x 1.0

8.3 Layout guidelines

Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. If the layout is not fulfilled carefully, important parameters such as: stability, efficiency, line and load regulation and output voltage ripple may be compromised. Short, wide traces must be implemented for main current and for power ground paths. The input capacitor must be placed as close as possible to the device pin as well as the inductor and output capacitor. The feedback pin (FB) is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. A common ground node minimizes ground noise.

Figure 22: Flip Chip layout recommended (not in scale)



9 Different output voltage versions of the ST1S15 available on request

Options available on request:

- 0.8 V
- 1 V
- 1.05 V
- 1.2 V
- 1.25 V
- 1.5 V
- 1.8 V
- 1.85 V
- 1.875 V
- 2.5 V
- 2.8 V
- 3.0 V
- 3.3 V

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

10.1 Flip Chip 6 package information

Figure 23: Flip Chip 6 package outline

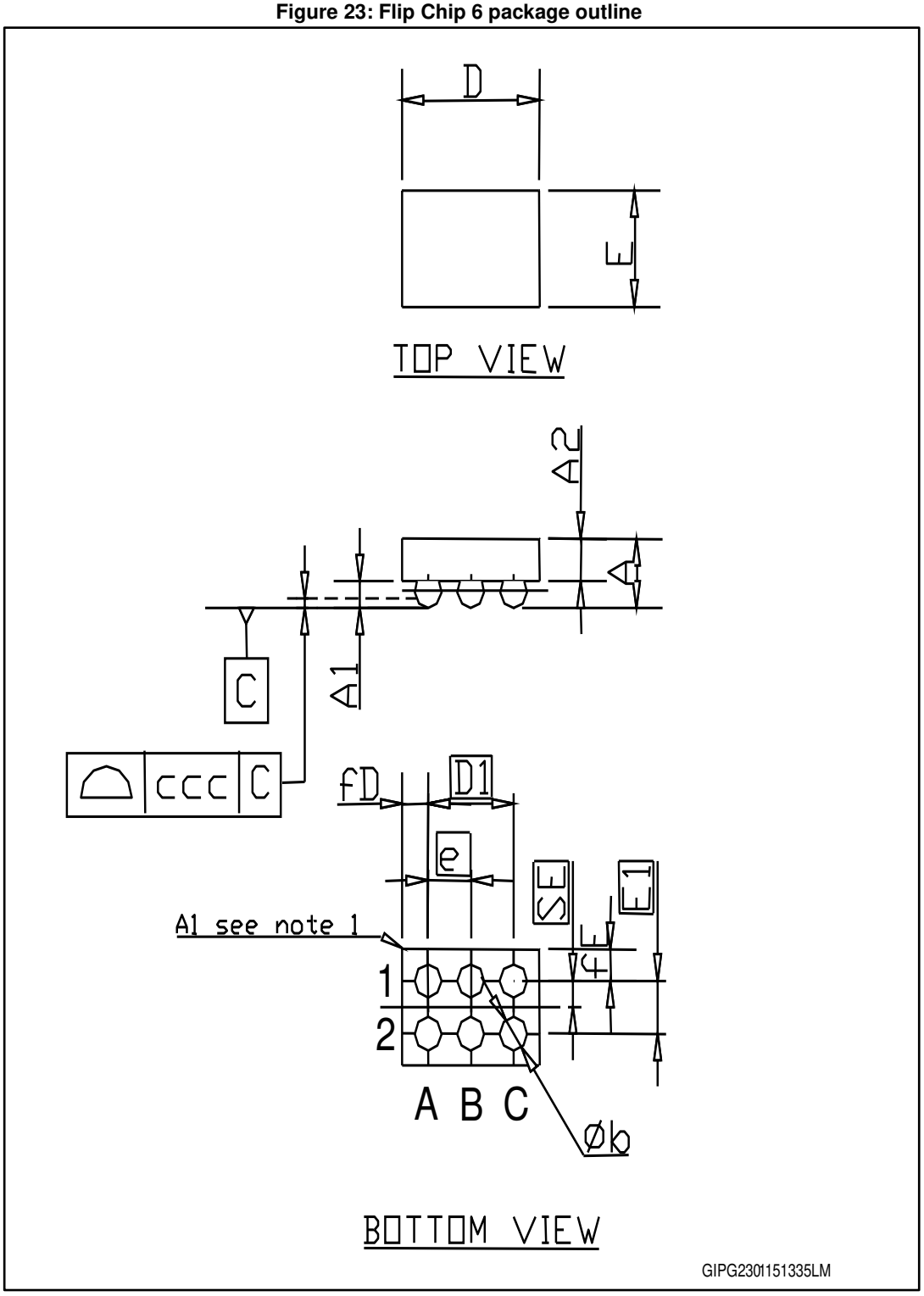
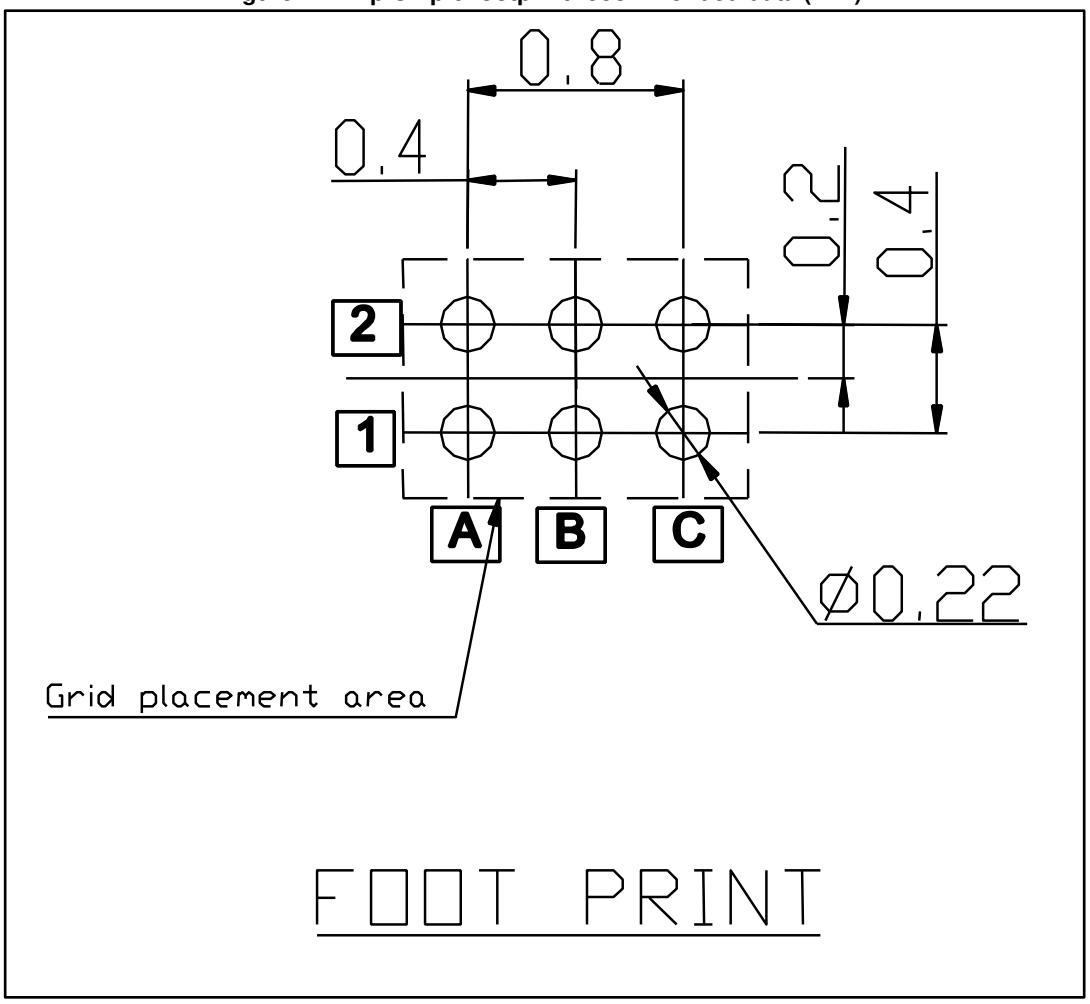


Table 9: Flip Chip 6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.52	0.56	0.6
A1	0.17	0.20	0.23
A2	0.35	0.36	0.37
b	0.23	0.25	0.29
D	1.16	1.19	1.22
D1		0.8	
e		0.4	
E	0.905	0.935	0.965
E1		0.4	
f_D		0.267	
f_E		0.195	
SE		0.2	
ccc		0.075	

The terminal A1 on the bump side is identified by a distinguishing feature (for instance by a circular "clear area" typically 0.1 mm diameter) and/or a missing bump. The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "clear area" typically 0.5 mm diameter).

Figure 24: Flip Chip 6 footprint recommended data (mm)



10.2 Packing information

Figure 25: Tape and reel outline

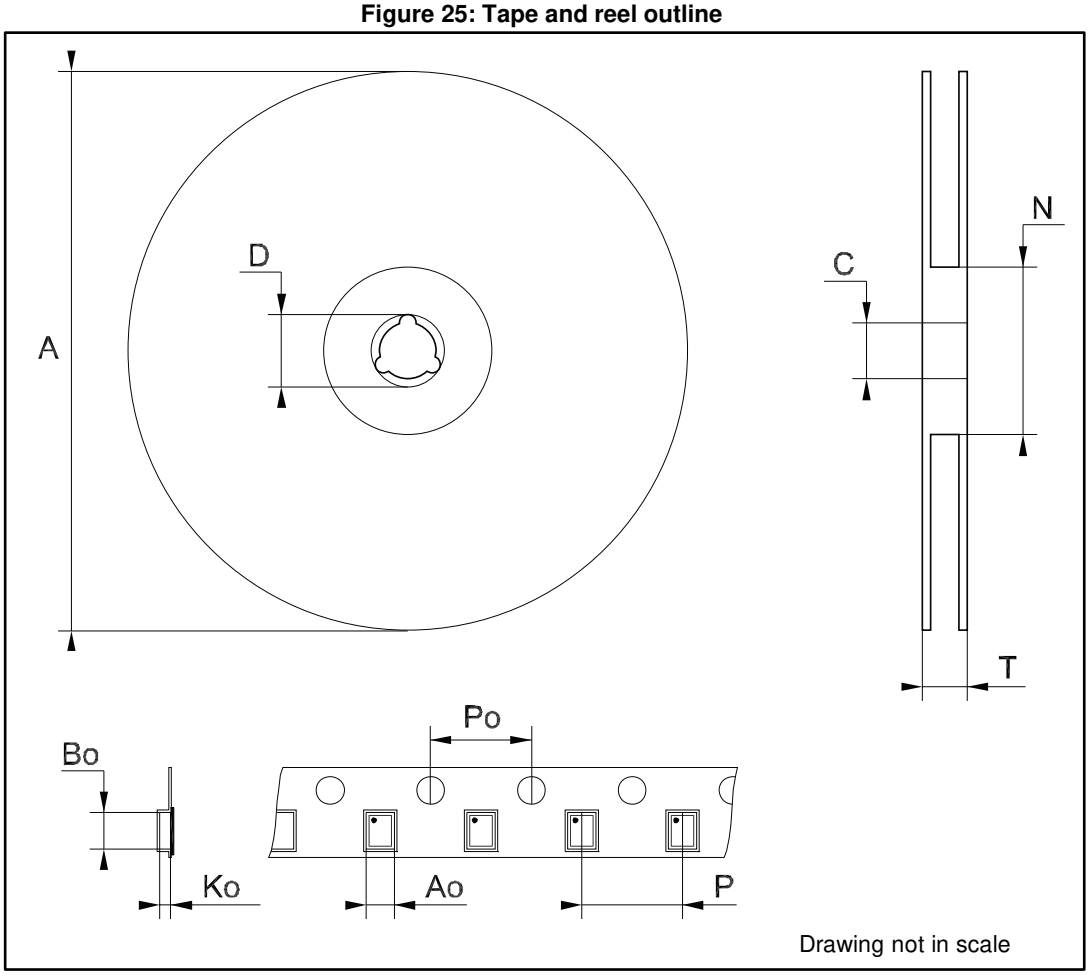


Table 10: Tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8		13.2
D	20.2		
N	60		
T			14.4
Ao	1.01	1.06	1.11
Bo	1.26	1.31	1.36
Ko	0.61	0.66	0.71
Po	3.9		4.1
P	3.9		4.1

11 Revision history

Table 11: Document revision history

Date	Revision	Changes
07-Jun-2012	1	Initial release.
4-Mar-2013	2	Modified: D1 and E1 values in table 9.
27-Aug-2013	3	Updated: table 1, table 7, section 9 and Package mechanical data.
24-Feb-2015	4	Deleted DFN package.

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