Top View

Vishay Siliconix

# Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0267			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0290			
I <sub>D</sub> (A) per leg	23			
Configuration	Dual			

# PowerPAK® SO-8L Dual PowerPAK® SO-8L Dual D1 D2 T S1 S1 G2 G2 G2

**Bottom View** 

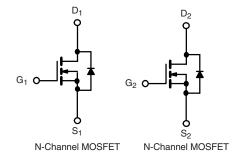
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Material categorization:
   For definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>





ROHS COMPLIANT HALOGEN FREE



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ956EP-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T <sub>C</sub> = 25 °C, unles	s otherwise noted	)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	60	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	V		
Continuous Drain Current	T <sub>C</sub> = 25 °C	1	23		
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	13		
Continuous Source Current (Diode Conduct	I <sub>S</sub>	30	Α		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	92		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	19		
Single Pulse Avalanche Energy	L = 0.1 mn	E <sub>AS</sub>	18	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	34	W	
	T <sub>C</sub> = 125 °C	= 125 °C P <sub>D</sub>		VV	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering Recommendations (Peak Temperature) d, e			260	1	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient PCE	3 Mount <sup>c</sup> R <sub>thJA</sub>	85	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	4.3	C/VV

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square Pcb (Fr4 material).
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.

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PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> :	= 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ
-		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.2 A	-	0.0223	0.0267	
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.2 A, T <sub>J</sub> = 125 °C	-	-	0.0480	Ω
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.2 A, T <sub>J</sub> = 175 °C	-	-	0.0610	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 5 A	-	0.0242	0.0290	
Forward Transconductance b	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 5.2 A	-	19	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	1113	1395	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$	-	100	125	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	44	55	
Total Gate Charge <sup>c</sup>	Qg			-	20	30	
Gate-Source Charge c	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, I_{D} = 9.6 \text{ A}$	-	3.5	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	1		-	3	-	
Gate Resistance	$R_g$		f = 1 MHz	0.8	1.7	2.5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	8	12	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_{L} = 30 \Omega$		-	11	17	ne
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, Y$	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	24	35	ns
Fall Time <sup>c</sup>	t <sub>f</sub>	]		-	6	9	
Source-Drain Diode Ratings and Chara	cteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	92	Α
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 3.6 A, V <sub>GS</sub> = 0 V		_	0.76	1.1	V

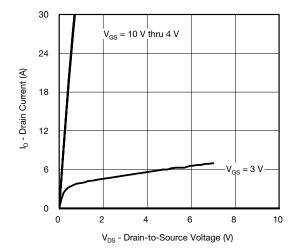
#### **Notes**

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

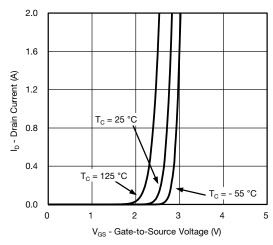
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



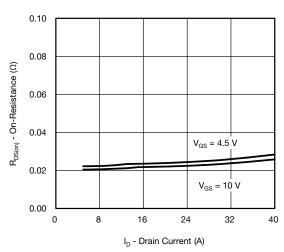
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



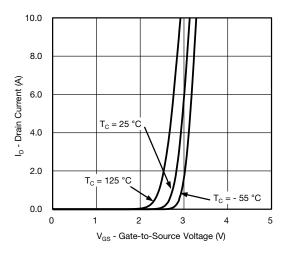
#### **Output Characteristics**



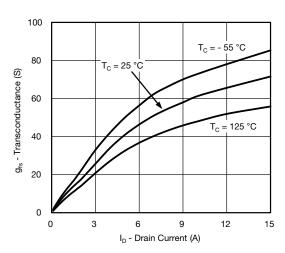
#### **Transfer Characteristics**



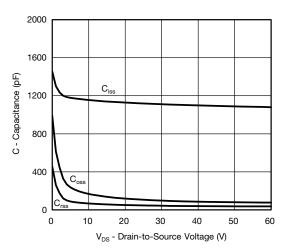
On-Resistance vs. Drain Current



#### **Transfer Characteristics**

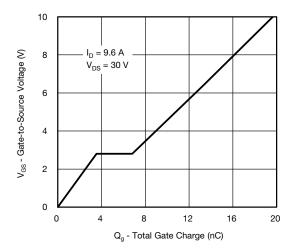


#### Transconductance

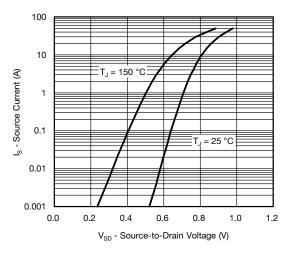




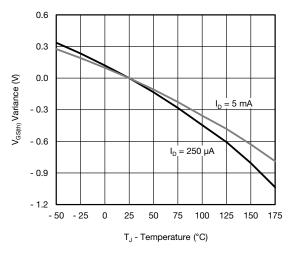
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



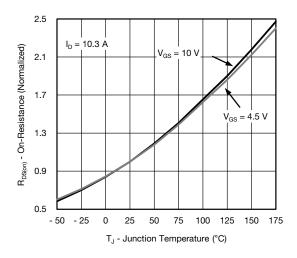
#### **Gate Charge**



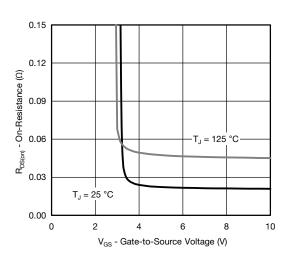
#### Source Drain Diode Forward Voltage



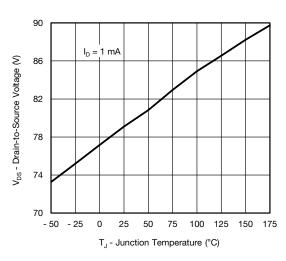
**Threshold Voltage** 



#### On-Resistance vs. Junction Temperature



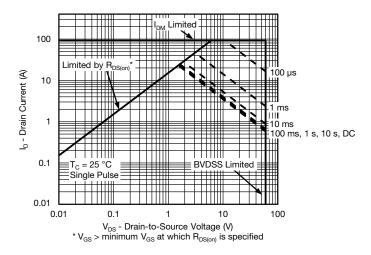
#### On-Resistance vs. Gate-to-Source Voltage



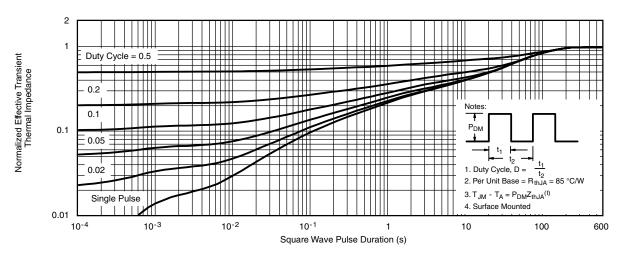
**Drain Source Breakdown vs. Junction Temperature** 



## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



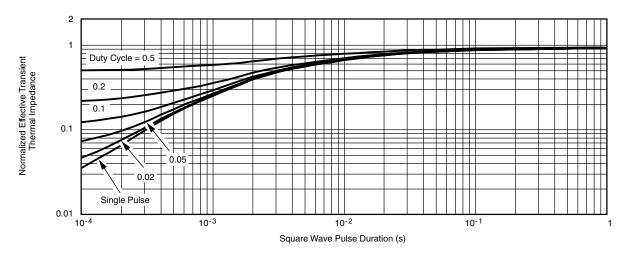
#### **Safe Operating Area**



Normalized Thermal Transient Impedance, Junction-to-Ambient



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

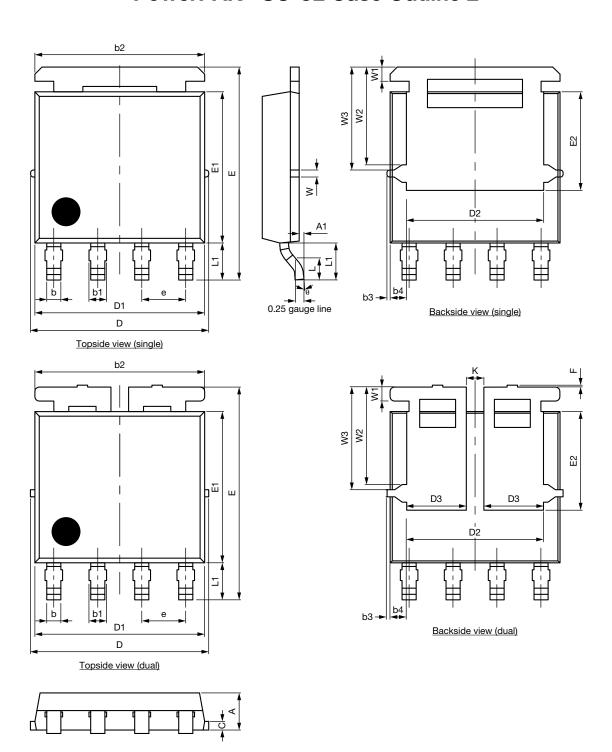
#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppq?64137">www.vishay.com/ppq?64137</a>.



# PowerPAK® SO-8L Case Outline 2



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DIM.		MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094	_		0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC	•	0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51	•	0.020			
W		0.23		0.009			
W1	0.41		0.016				
W2	2.82		0.111				
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

ECN: C21-1498-Rev. C, 01-Nov-2021

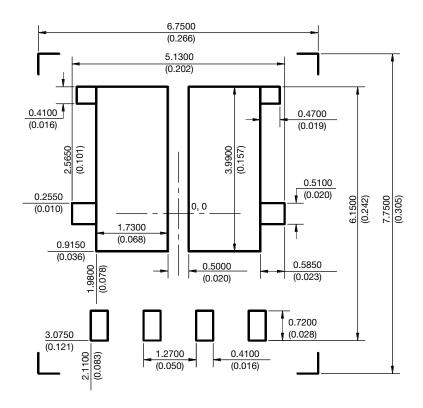
DWG: 6044

#### Note

• Millimeters will govern



#### RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads Dimensions in mm (inches) Keep-out 6.75 (0.266) x 7.75 (0.305)



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