FAN5009

Dual Bootstrapped 12V MOSFET Driver

Features

- Drives N-channel High-Side and Low-Side MOSFETs in a synchronous buck configuration
- 12V High-Side and 12V Low-Side Drive
- Internal Adaptive “Shoot-Through” Protection
- Integrated Bootstrap Diode for High-Side Drive
- Fast rise and fall times
- Switching Frequency Up to 500kHz
- $\overline{OD}$ input for Output Disable – allows for synchronization with PWM controller
- SOIC-8 Package
- Available in low thermal resistance MLP package

Applications

- Multi-phase VRM/VRD regulators for Microprocessor Power
- High Current/High Frequency DC/DC Converters
- High Power Modular Supplies

General Description

The FAN5009 is a dual, high frequency MOSFET driver, specifically designed to drive N-Channel power MOSFETs in a synchronous-rectified buck converter. These drivers, combined with a Fairchild Multi-Phase PWM controller and power MOSFETs, form a complete core voltage regulator solution for advanced microprocessors.

The FAN5009 drives the upper and lower MOSFET gates of a synchronous buck regulator to $12V_{GS}$. The upper gate drive includes an integrated boot diode and requires only an external bootstrap capacitor (C_{BOOT}). The output drivers in the FAN5009 have the capacity to efficiently switch power MOSFETs at frequencies up to 500kHz. The circuit’s adaptive shoot-through protection prevents the MOSFETs from conducting simultaneously.

The FAN5009 is rated for operation from 0°C to +85°C and is available in low-cost SOIC-8 or MLP packages.

Typical Application

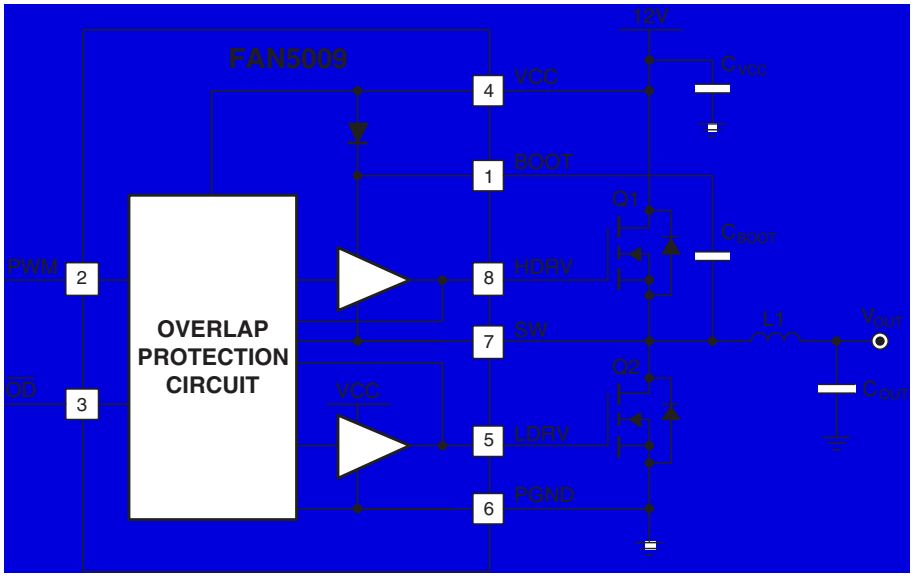
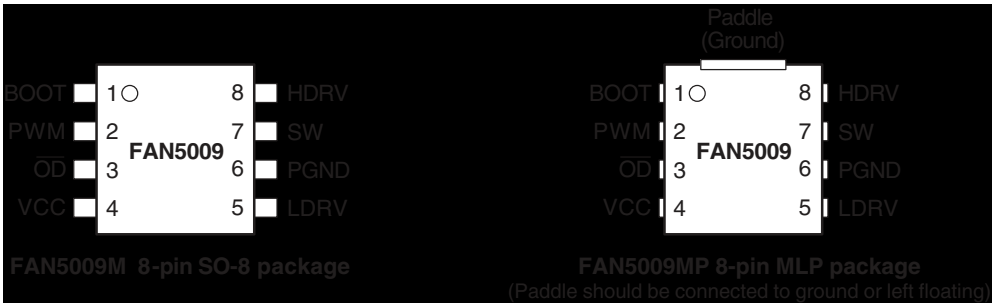


Figure 1. Typical Application.

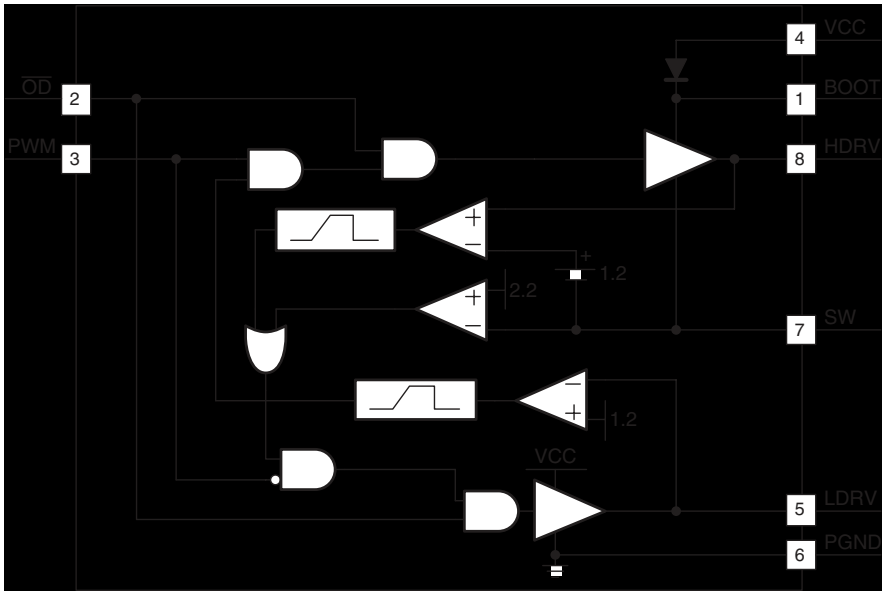
Pin Configuration



Pin Definitions

Pin #	Pin Name	Pin Function Description
1	BOOT	**Bootstrap Supply Input.** Provides voltage supply to high-side MOSFET driver. Connect to bootstrap capacitor. See Applications Section.
2	PWM	**PWM Signal Input.** This pin accepts a logic-level PWM signal from the controller.
3	$\overline{OD}$	**Output Disable.** When low, this pin disables FET switching (HDRV and LDRV are held low).
4	VCC	**Power Input**. +12V chip bias power. Bypass with a 1µF ceramic capacitor.
5	LDRV	**Low Side Gate Drive Output.** Connect to the gate of low-side power MOSFET(s).
6	PGND	**Power ground.** Connect directly to source of low-side MOSFET(s).
7	SW	**Switch Node Input**. Connect as shown in Figure 1. SW provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
8	HDRV	**High Side Gate Drive Output** – Connect to the gate of high-side power MOSFET(s).

Functional Block Diagram



Absolute Maximum Ratings

Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually, not in combination. Unless otherwise specified, voltages are referenced to PGND.

Parameter		Min.	Max.	Units
VCC to PGND		–0.3	15	V
PWM and $\overline{OD}$ pins		–0.3	5.5	V
SW to PGND	Continuous	–1	15	V
	Transient (t=100nsec, F≤500kHz)	–5(1)	25	V
BOOT to SW		–0.3	15	V
BOOT to PGND	Continuous	–0.3	30	V
	Transient (t=100nsec, F≤500kHz)		33(1)	V
HDRV		V_{SW}–1	V_{BOOT}+0.3	V
LDRV	Continuous	–0.5	V_{CC}+0.3	V
	Transient (t=200nsec)	–2(1)		V

Notes:

1. For transient derating beyond the levels indicated, refer to the graphs on page 7.

Thermal Information

Parameter	Min.	Typ.	Max.	Units
Junction Temperature (T_J)	0		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C
Vapor Phase, 60 seconds			215	°C
Infrared, 15 seconds			220	°C
Power Dissipation (P_D) T_A = 25°C			715	mW
Thermal Resistance, SO8 – Junction to Case θ_{JC}		40		°C/W
Thermal Resistance, SO8 – Junction to Ambient θ_{JA}		140		°C/W
Thermal Resistance, MLP – Junction to Paddle θ_{JC}		4		°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC	VCC to PGND	10	12	13.5	V
Ambient Temperature (T_A)		0		85	°C
Junction Temperature (T_J)		0		125	°C

Electrical Specifications

V_{CC} = 12V, and T_A = 25°C using circuit in Figure 2 unless otherwise noted. The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Input Supply							
VCC Voltage Range	V_{CC}		•	6.4	12	13.5	V
VCC Current	I_{CC}	$\overline{OD}$ = 0V	•		3.5	8	mA
Bootstrap Diode							
Continuous Forward Current	$I_{F(AVG)}$		•			25	mA
Reverse Breakdown Voltage	V_R		•	15			V
Reverse Recovery Time[2]	t_{RR}				10		ns
Forward Voltage[2]	V_F	I_F = 10mA			0.8	0.95	V
$\overline{OD}$ Input							
Input High Voltage	$V_{IH\ (\overline{OD})}$		•	2.5			V
Input Low Voltage	$V_{IL\ (\overline{OD})}$		•			0.8	V
Input Current	$I_{\overline{OD}}$	$\overline{OD}$ = 3.0V	•	–300		+300	nA
Propagation Delay[2]	$t_{pdl(\overline{OD})}$	See Figure 3			30	40	ns
	$t_{pdh(\overline{OD})}$				30	45	ns
PWM Input							
Input High Voltage	$V_{IH(PWM)}$		•	3.5			V
Input Low Voltage	$V_{IL(PWM)}$		•			0.8	V
Input Current	$I_{IL(PWM)}$		•	-1		+1	µA
High-Side Driver							
Output Resistance, Sourcing Current	R_{HUP}	V_{BOOT}–V_{SW} = 12V			3.8	4.4	Ω
Output Resistance, Sinking Current	R_{HDN}	V_{BOOT}–V_{SW} = 12V			1.4	1.8	Ω
Transition Times[2,4]	$t_{R(HDRV)}$	See Figure 2			40	55	ns
	$t_{F(HDRV)}$				20	30	ns
Propagation Delay[2,3]	$t_{pdh(HDRV)}$	See Figure 2, and 4			50	65	ns
	$t_{pdl(HDRV)}$				25	40	ns

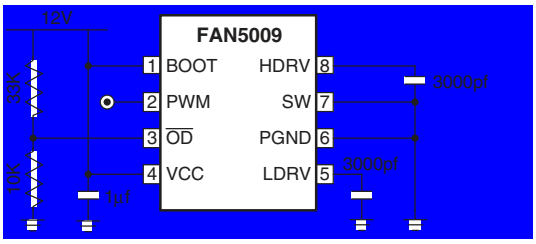


Figure 2. Test Circuit

Electrical Specifications (continued)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Low-Side Driver							
Output Resistance, Sourcing Current	R_{LUP}				3.4	4.0	Ω
Output Resistance, Sinking Current	R_{LDN}				1.4	1.8	Ω
Transition Times[2,4]	$t_{R(LDRV)}$	See Figure 2			40	50	ns
	$t_{F(LDRV)}$				20	30	ns
Propagation Delay[2,3]	$t_{pdh(LDRV)}$	See Figures 2, 4			20	30	ns
	$t_{pdl(LDRV)}$				25	40	ns
	$t_{pdh(ODRV)}$	See Adaptive Gate Drive Circuit description			240		ns

NOTES:

1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control
2. AC Specifications guaranteed by design/characterization (not production tested).
3. For propagation delays, “tpdh” refers to low-to-high signal transition and “tpdl” refers to high-to-low signal transition
4. Transition times are defined for 10% and 90% of DC values

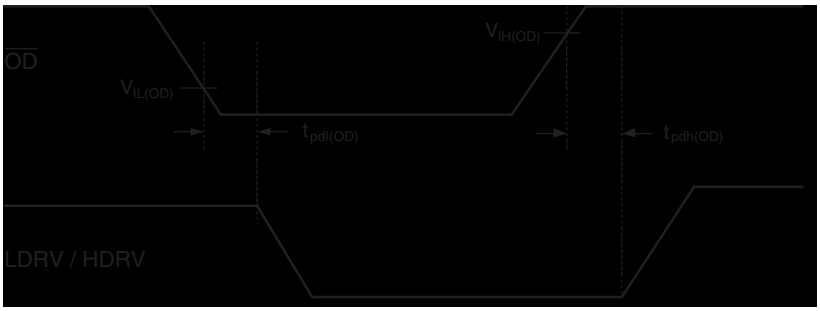
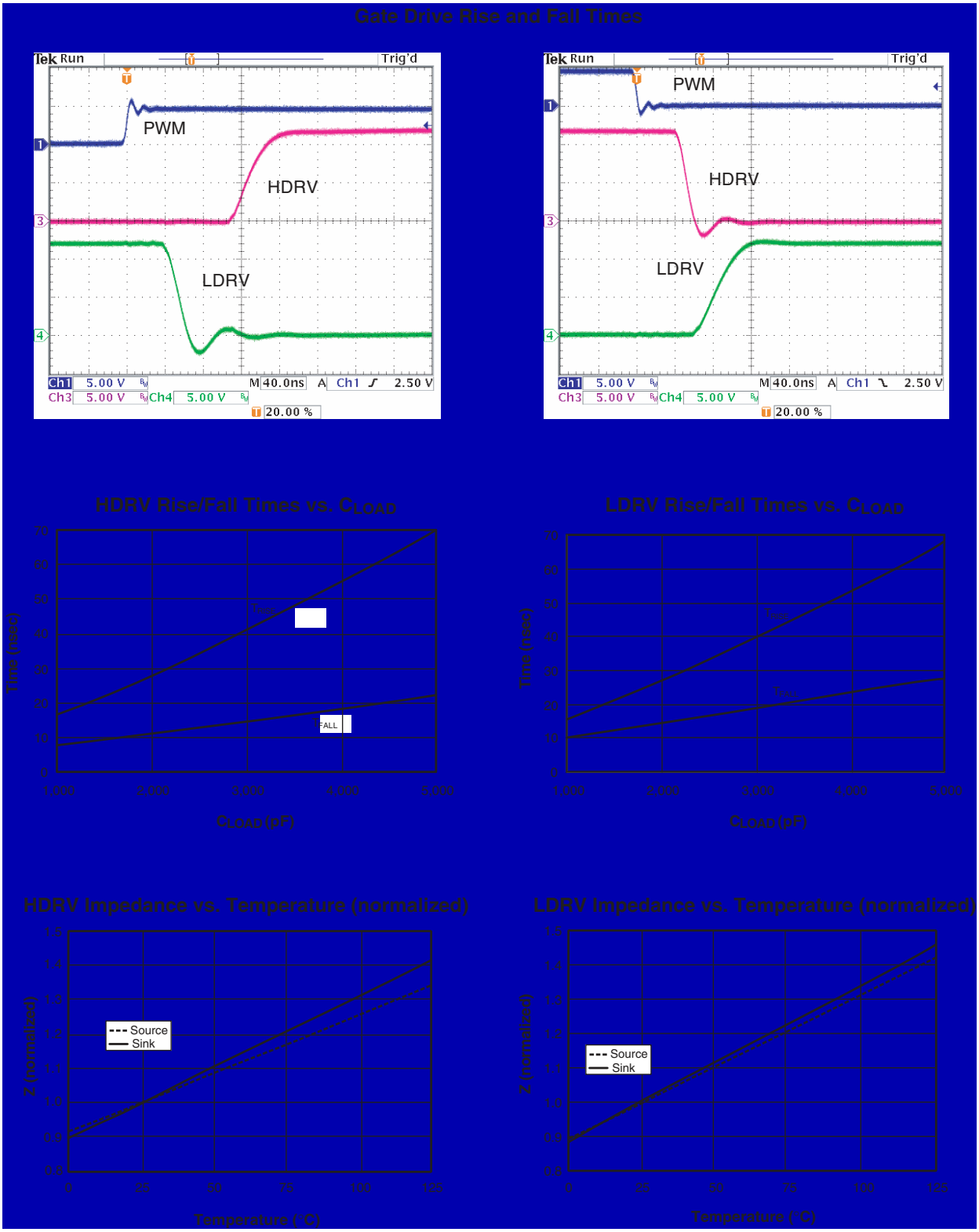


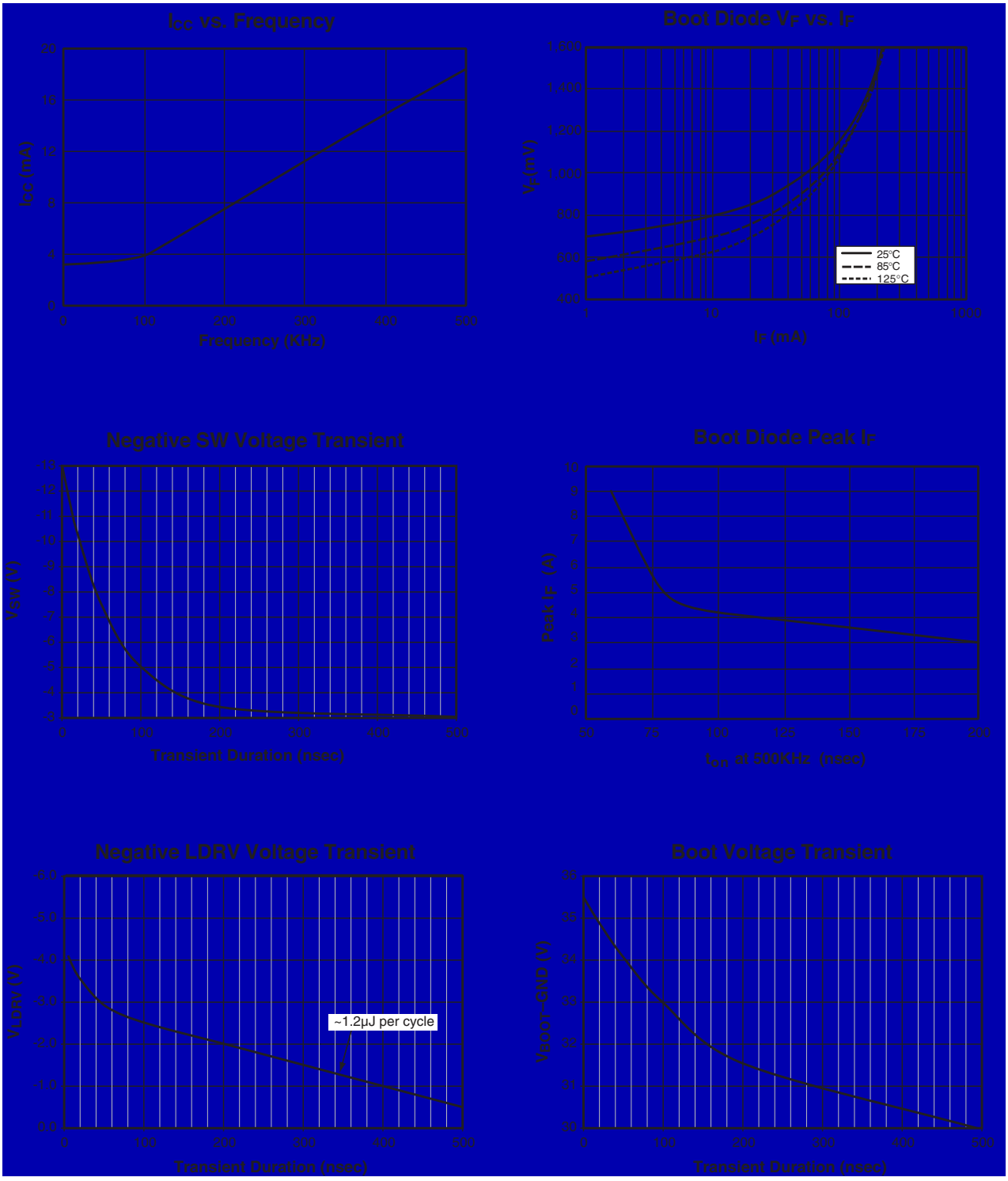
Figure 3. Output Disable Timing

Figure 4. Adaptive Gate Drive Timing

Typical Characteristics



Typical Characteristics (continued)



Circuit Description

The FAN5009 is a dual MOSFET driver optimized for driving N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3nF load at speeds up to 500kHz.

For a more detailed description of the FAN5009 and its features, refer to the Internal Block Diagram and Figure 1.

Low-Side Driver

The low-side driver (LDRV) is designed to drive a ground-referenced low $R_{DS(on)}$ N-channel MOSFETs. The bias for LDRV is internally connected between VCC and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the FAN5009 is disabled ($\overline{OD}$ = 0V), LDRV is held low.

High-Side Driver

The high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the internal diode and external bootstrap capacitor (C_{BOOT}) .

During start-up, SW is held at PGND, allowing C_{BOOT} to charge to VCC through the internal diode. When the PWM input goes high, HDRV will begin to charge the high-side MOSFET's gate (Q1). During this transition, charge is removed from C_{BOOT} and delivered to Q1's gate. As Q1 turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} +$V_{C(BOOT)}$, which provides sufficient V_{GS} enhancement for Q1.

To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. C_{BOOT} is then recharged to VCC when SW falls to PGND.

HDRV output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Adaptive Gate Drive Circuit

The FAN5009 embodies an advanced design that ensures minimum MOSFET dead-time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to Figure 4 for the relevant timing waveforms.

To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, Q2 will begin to turn OFF after some propagation delay ($t_{pdl(LDRV)}$).

Once the LDRV pin is discharged below ~1.2V, Q1 begins to turn ON after adaptive delay $t_{pdh(HDRV)}$.

To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, Q1 will begin to turn OFF after some propagation delay ($t_{pdl(HDRV)}$). Once the SW pin falls below ~2.2V, Q2 begins to turn ON after adaptive delay $t_{pdh(LDRV)}$.

Additionally, V_{GS} of Q1 is monitored. When $V_{GS(Q1)}$ is discharged below ~1.2V, a secondary adaptive delay is initiated, which results in Q2 being driven ON after $t_{pdh(ODRV)}$, regardless of SW state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle, particularly for cases where the power convertor is sinking current and SW voltage does not fall below the 2.2V adaptive threshold. Secondary delay $t_{pdh(ODRV)}$ is longer than $t_{pdh(LDRV)}$.

Application Information

Supply Capacitor Selection

For the supply input (V_{CC}) of the FAN5009, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FAN5009 V_{CC} and PGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and the internal diode, as shown in Figure 1. Selection of these components should be done after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} = \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where Q_G is the total gate charge of the high-side MOSFET, and ΔV_{BOOT} is the voltage droop allowed on the high-side MOSFET drive. For example, the Q_G of the FDD6696 is about 35nC @ 12V_{GS}. For an allowed droop of ~300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor must be used.

The average diode forward current, $I_{F(AVG)}$, can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times F_{SW} \quad (2)$$

where F_{SW} is the switching frequency of the controller.

The peak surge current rating of the internal diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces. For applications requiring higher I_F, an external diode may be used in parallel to the internal diode.

Thermal Considerations

Total device dissipation:

$$P_D = P_Q + P_R + P_{HDRV} + P_{LDRV} \quad (3)$$

where P_Q represents quiescent power dissipation:

$$P_Q = V_{CC} \times [4mA + 0.036\ (F_{SW} - 100)] \quad (4)$$

where F_{SW} is switching frequency (in kHz).

P_R is power dissipated in the bootstrap rectifier:

$$P_R = V_F \times F_{SW} \times Q_{G1} \quad (5)$$

Where Q_{G1} is total gate charge of the upper FET (Q1) for it's applied V_{GS}.

V_F for the applied $I_{F(AVG)}$ can be graphically determined using the datasheet curves, where:

$$I_{F(AVG)} = F_{SW} \times Q_{G1} \quad (6)$$

P_{HDRV} represents internal power dissipation of the upper FET driver.

$$P_{HDRV} = P_{H(R)} + P_{H(F)} \quad (7)$$

Where $P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges, respectively:

$$P_{H(R)} = P_{Q1} \times \frac{R_{HUP}}{R_{HUP} + R_E + R_G} \quad (8)$$

$$P_{H(F)} = P_{Q1} \times \frac{R_{HDN}}{R_{HDN} + R_E + R_G} \quad (9)$$

where:

$$P_{Q1} = \frac{1}{2} \times Q_{G1} \times V_{GS(Q1)} \times F_{SW} \quad (10)$$

As described in eq. 8 and 9 above, the total power consumed in driving the gate is divided in proportion to the resistances in series with the MOSFET's internal gate node as shown below:

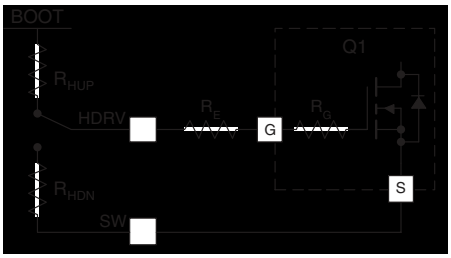


Figure 5. Driver dissipation model

R_G is the polysilicon gate resistance, internal to the FET. R_E is the external gate drive resistor implemented in many designs. Note that the introduction of R_E can reduce driver power dissipation, but excess R_E may cause errors in the "adaptive gate drive" circuitry. For more information please refer to Fairchild app note AN-6003, "Shoot-through" in Synchronous Buck Converters.

P_{LDRV} is dissipation of the lower FET driver.

$$P_{LDRV} = P_{L(R)} + P_{L(F)} \quad (11)$$

Where $P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges, respectively:

$$P_{L(R)} = P_{Q2} \times \frac{R_{LUP}}{R_{LUP} + R_E + R_G} \quad (12)$$

$$P_{L(F)} = P_{Q2} \times \frac{R_{LDN}}{R_{HDN} + R_E + R_G} \quad (13)$$

where:

$$P_{Q2} = \frac{1}{2} \times Q_{G2} \times V_{GS(Q2)} \times F_{SW} \quad (14)$$

Layout Considerations

Use the following general guidelines when designing printed circuit boards (see Figures 6 and 7):

1. Trace out the high-current paths and use short, wide (>25 mil) traces to make these connections.
2. Connect the PGND pin of the FAN5009 as close as possible to the source of the lower MOSFET.
3. The V_{CC} bypass capacitor should be located as close as possible to V_{CC} and PGND pins.
4. Use vias to other layers when possible to maximize thermal conduction away from the IC.

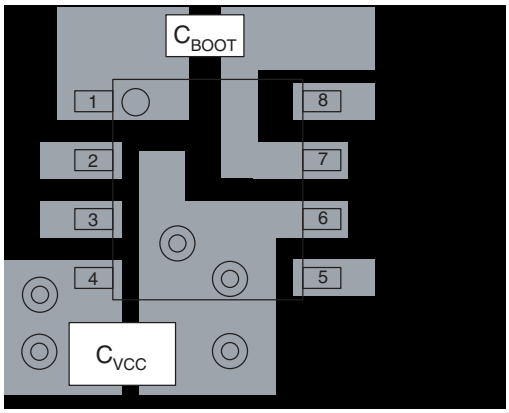


Figure 6. External component placement recommendation for SO8 package (not to scale)

5. The paddle on the MLP package is internally referenced to ground. It can be left floating or connected to ground. For best thermal performance it should be connected to ground as shown in Figure 7.

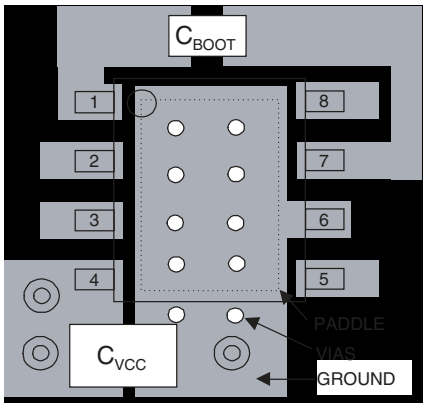


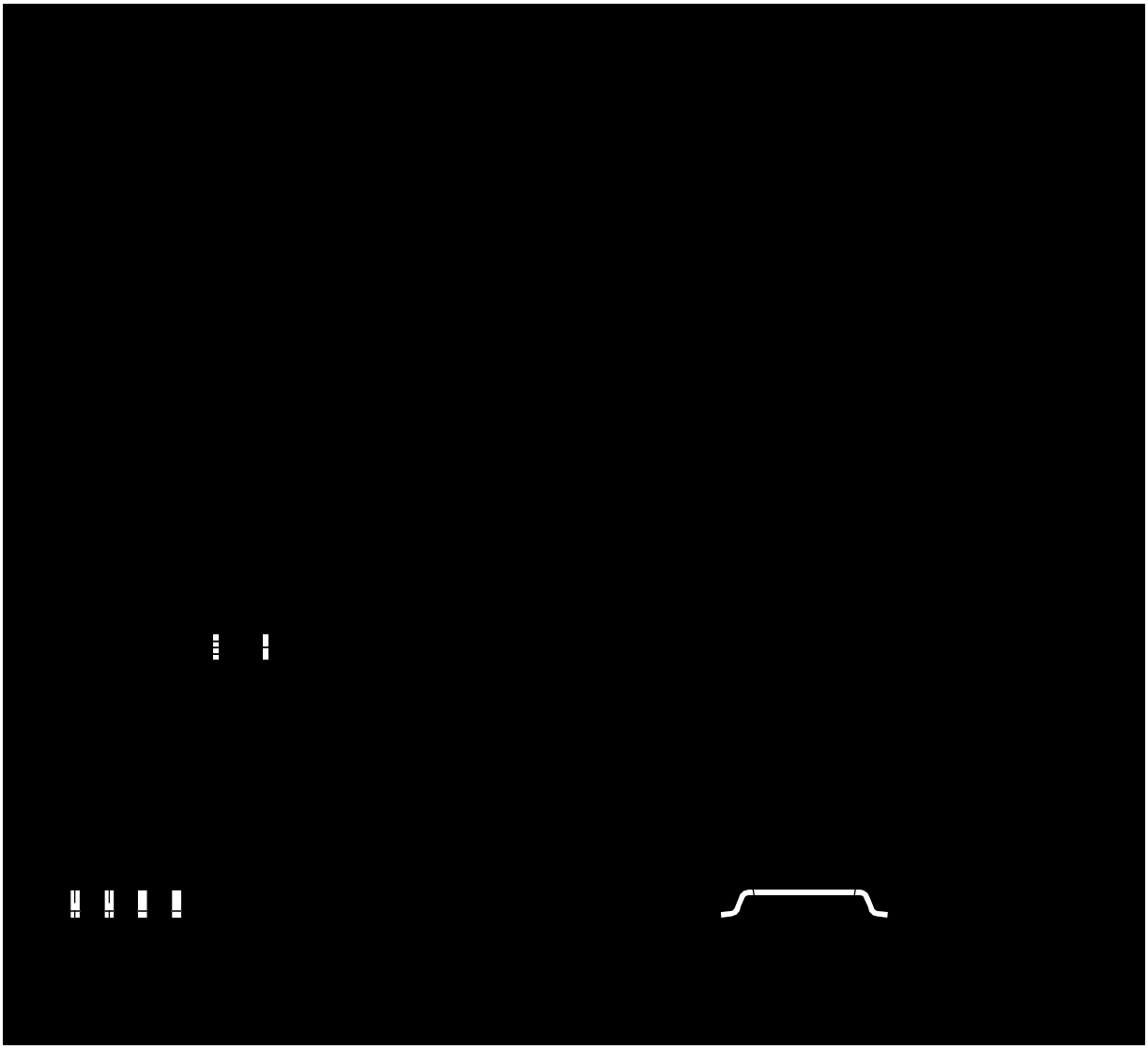
Figure 7. Recommended layout for MLP package. Also accepts SO8 package (not to scale)

6. The recommended land pattern shown in the MLP mechanical dimensions will work with both MLP-8 and SO-8 packages.

The circuit in Figure 1 illustrates a typical implementation of a single phase of a multi-phase buck converter for V_{CORE} applications. For a complete VR10 design example, please refer to the FAN5019 or FAN5018 datasheets.

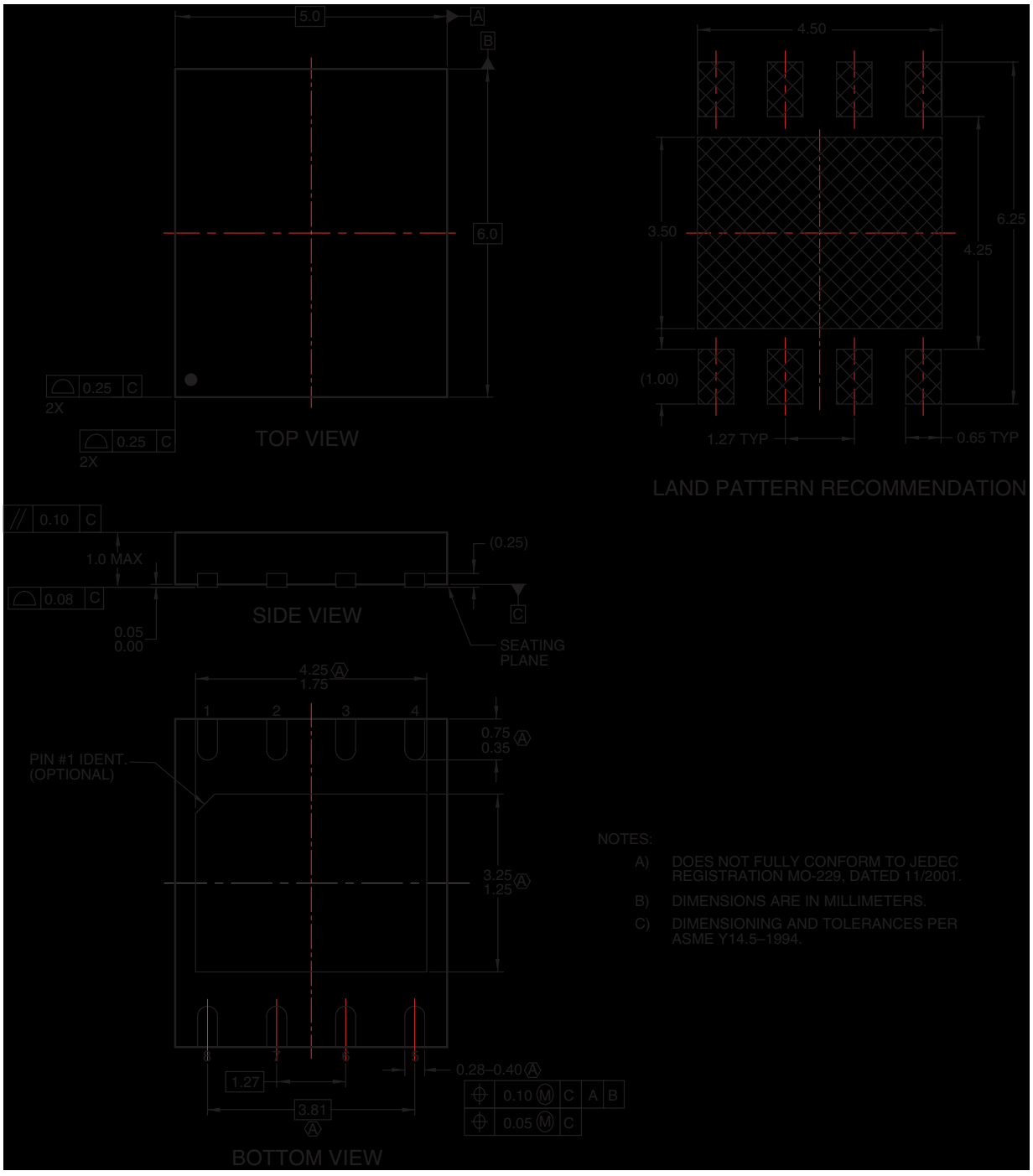
Mechanical Dimensions

0.150, 8 Lead SOIC Package



Mechanical Dimensions

5mm x 6mm, 8 Lead MLP Package



Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5009M	0°C to 85°C	SOIC-8	Rails
FAN5009MX	0°C to 85°C	SOIC-8	Tape and Reel
FAN5009MPX	0°C to 85°C	MLP-8	Tape and Reel