Sound Processor with Built-in 2-band Equalizer

BD37511FS

General Description

BD37511FS is a sound processor with built-in 2-band equalizer for car audio. The functions are 3ch stereo input selector, input-gain control, main volume and 4ch fader volume. Moreover, its “Advanced switch circuit”, which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). “Advanced switch” makes control of microcomputer easier, supporting the construction of a high quality car audio system.

Features

- Reduce switching noise of mute, main volume, fader volume, bass, trebles by using advanced switch circuit
- Built-in 3 single-ended input selectors
- Decrease the number of external components due to built-in 2-band equalizer filter.
- It is possible to adjust the gain of the bass and treble up to ±20dB with 1 dB step gain adjustment.
- Energy-saving design resulting in low current consumption, by utilizing the Bi-CMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Input terminals and output terminals are organized and separately laid out to keep the signal flow in one direction which results in simpler and smaller PCB layout.
- It is possible to control the I^{2}C BUS by 3.3V / 5V.

Applications

It is optimal for use in car audio systems. It can also be used for audio equipment of mini Compo, micro Compo, TV, etc.

Key Specifications

Power Supply Voltage Range:	7.0V to 9.5V
Circuit Current (No Signal):	15mA(Typ)
Total Harmonic Distortion:	0.005%(Typ)
Maximum Input Voltage:	2.3Vrms (Typ)
Cross-talk Between Selectors:	-100dB(Typ)
Volume Control Range:	+0dB to -40dB
Output Noise Voltage:	6µVrms(Typ)
Residual Output Noise Voltage:	2µVrms(Typ)
Operating Temperature Range:	-40°C to +85°C

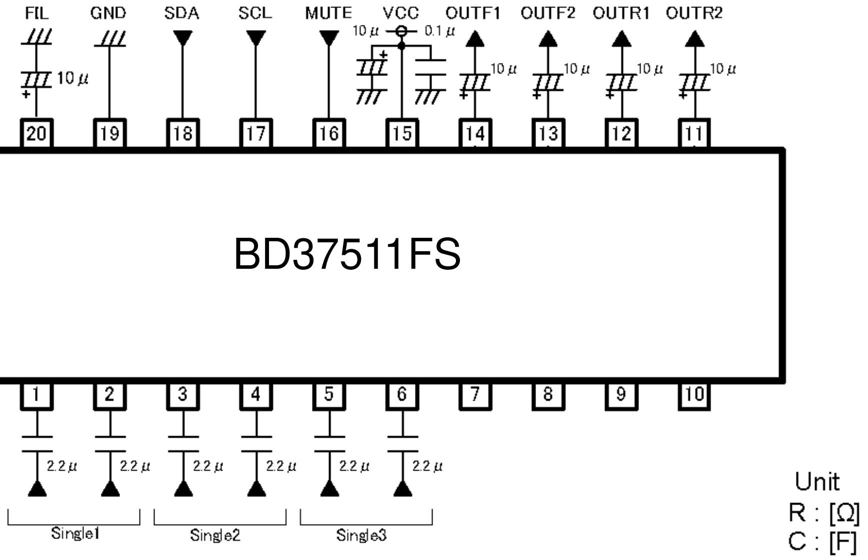
Package

W(Typ) x D(Typ) x H(Max)

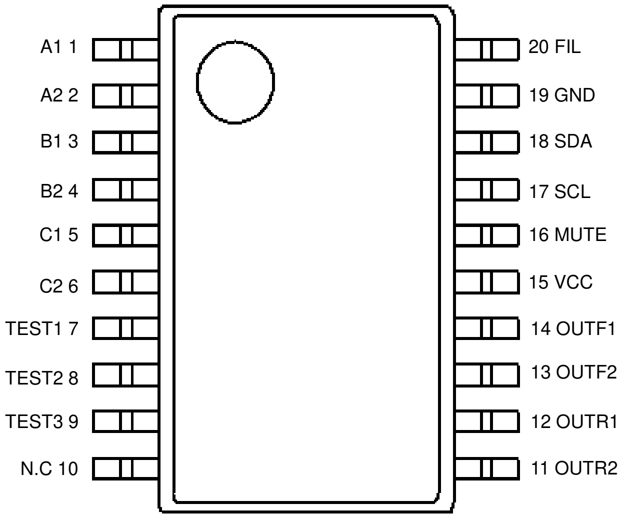
SSOP-A20
8.70mm x 7.80mm x 2.01mm

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit



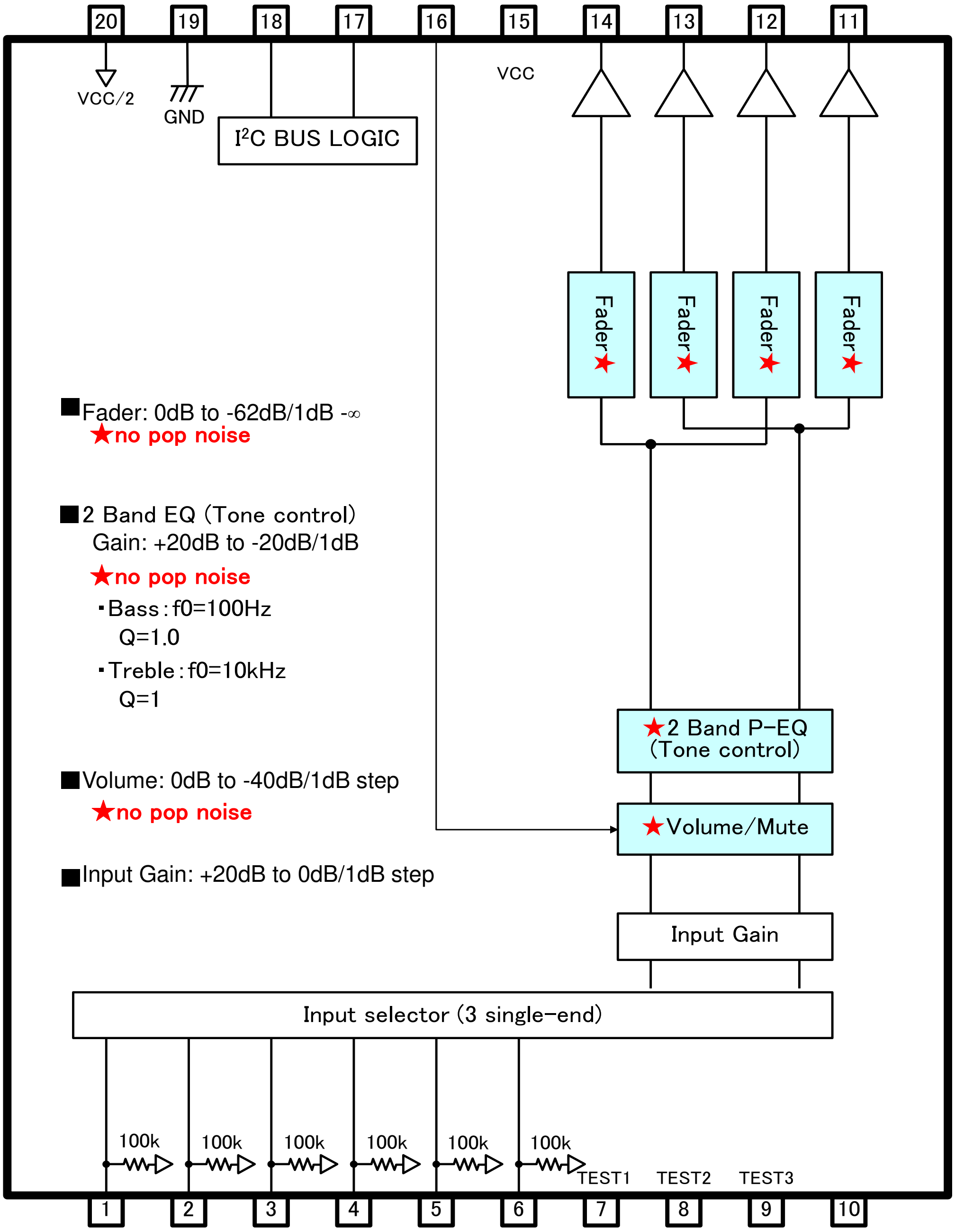
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	11	OUTR2	Rear output terminal of 2ch
2	A2	A input terminal of 2ch	12	OUTR1	Rear output terminal of 1ch
3	B1	B input terminal of 1ch	13	OUTF2	Front output terminal of 2ch
4	B2	B input terminal of 2ch	14	OUTF1	Front output terminal of 1ch
5	C1	C input terminal of 1ch	15	VCC	Power supply terminal
6	C2	C input terminal of 2ch	16	MUTE	External compulsory mute terminal
7	TEST1	Test Pin	17	SCL	I^{2}C Communication clock terminal
8	TEST2	Test Pin	18	SDA	I^{2}C Communication data terminal
9	TEST3	Test Pin	19	GND	GND terminal
10	N.C.	No Connection	20	FIL	VCC/2 terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	10.0	V
Input Voltage	V_{IN}	V_{CC}+0.3 to GND-0.3	V
Power Dissipation	Pd	0.94 (Note 1)	W
Storage Temperature	Tstg	-55 to +150	°C

(Note 1) This value derates by 7.5mW/°C for Ta=25°C or more when ROHM standard board is used.
Thermal resistance θja = 133.3(°C/W)
ROHM Standard board
Size : 70 x 70 x 1.6(mm^3)
Material : A FR4 grass epoxy board(3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	°C

Electrical Characteristics

(Unless specified otherwise, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN} =1Vrms, Rg=600Ω, R_L=10kΩ, A input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, Fader 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current	I_Q	-	15	30	mA	No signal
	Voltage Gain	G_V	-1.5	0	+1.5	dB	G_V=20log(V_{OUT}/V_{IN})
	Channel Balance	CB	-1.5	0	+1.5	dB	CB = G_{V1}-G_{V2}
	Total Harmonic Distortion	THD+N1	-	0.005	0.05	%	V_{OUT}=1Vrms BW=400Hz-30KHz
	Output Noise Voltage *	V_{NO1}	-	6	25	µVrms	Rg = 0Ω BW = IHF-A
	Residual Output Noise Voltage *	V_{NOR}	-	2	10	µVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
	Cross-talk Between Channels *	CTC	-	-100	-90	dB	Rg = 0Ω CTC=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Ripple Rejection	RR	-	-70	-40	dB	f=1KHz V_{RR}=100mVrms RR=20log(V_{CC} IN/V_{OUT})
INPUT SELECTOR	Input Impedance(A, B, C)	R_{IN_S}	70	100	130	kΩ	
	Maximum Input Voltage	V_{IM}	2.1	2.3	-	Vrms	V_{IM} at THD+N(V_{OUT})=1% BW=400Hz-30KHz
	Cross-talk Between Selectors *	CTS	-	-100	-90	dB	Rg = 0Ω CTS=20log(V_{OUT}/V_{IN}) BW = IHF-A
INPUT GAIN	Minimum Input Gain	G_{IN_MIN}	-2	0	+2	dB	Input gain 0dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
	Maximum Input Gain	G_{IN_MAX}	18	20	22	dB	Input gain 20dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
	Gain Set Error	G_{IN_ERR}	-2	0	+2	dB	GAIN=+1dB to +20dB

Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
MUTE	Mute Attenuation *	G_{MUTE}	-	-105	-85	dB	Mute ON G_{MUTE}=20log(V_{OUT}/V_{IN}) BW = IHF-A
VOLUME	Maximum Attenuation	G_{V_MIN}	-43	-40	-37	dB	Volume = -40dB G_{V}=20log(V_{OUT}/V_{IN})
	Attenuation Set Error 1	G_{V_ERR1}	-2	0	+2	dB	GAIN & ATT=0dB to -15dB
	Attenuation Set Error 2	G_{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -40dB
BASS	Maximum Boost Gain	G_{B_BST}	18	20	22	dB	Gain=+20dB f=100Hz V_{IN}=100mVrms G_{B}=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{B_CUT}	-22	-20	-18	dB	Gain=-20dB f=100Hz V_{IN}=2Vrms G_{B}=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{B_ERR}	-2	0	+2	dB	Gain=-20dB to +20dB f=100Hz
TREBLE	Maximum Boost Gain	G_{T_BST}	18	20	22	dB	Gain=+20dB f=10kHz V_{IN}=100mVrms G_{T}=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{T_CUT}	-22	-20	-18	dB	Gain=-20dB f=10kHz V_{IN}=2Vrms G_{T}=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{T_ERR}	-2	0	+2	dB	Gain=-20dB to +20dB f=10kHz
FADER	Maximum Attenuation *	G_{F_MIN}	-	-100	-90	dB	Fader = -∞dB G_{F}=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Attenuation Set Error 1	G_{F_ERR1}	-2	0	+2	dB	ATT=0dB to -15dB
	Attenuation Set Error 2	G_{F_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{F_ERR3}	-4	0	+4	dB	ATT=-48dB to -62dB
	Output Impedance	R_{OUT}	-	-	50	Ω	V_{IN} =100mVrms
	Maximum Output Voltage	V_{OM}	2	2.2	-	Vrms	THD+N=1% BW=400Hz-30KHz

VP-9690A (Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

Typical Performance Curves

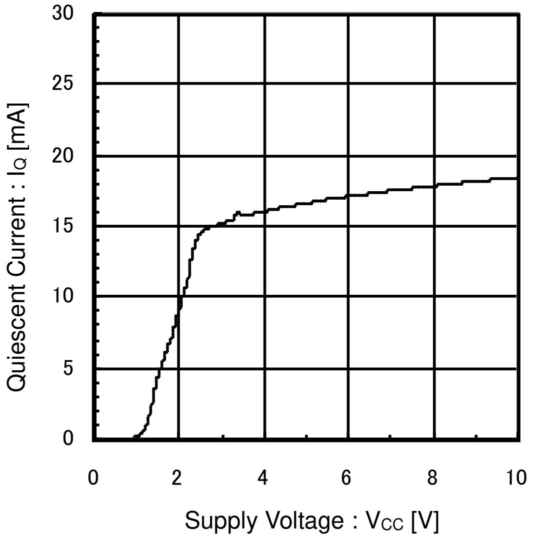


Figure 1. Quiescent Current vs Supply Voltage

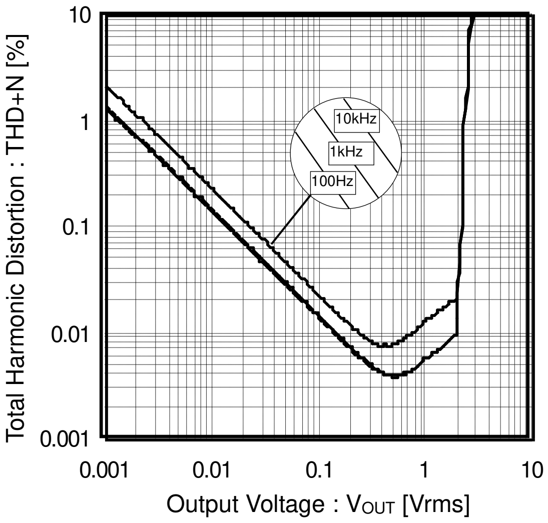


Figure 2. Total Harmonic Distortion vs Output Voltage

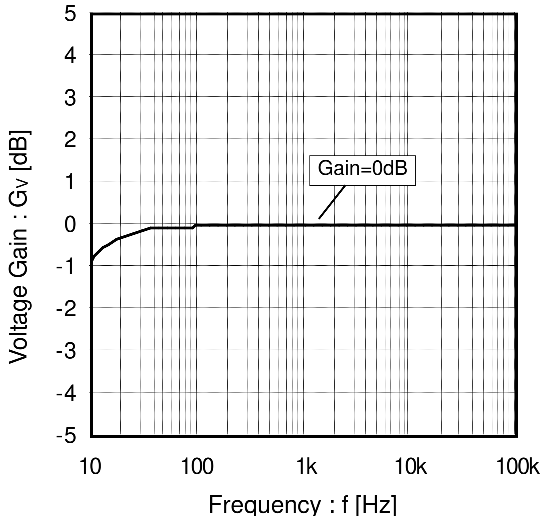


Figure 3. Voltage Gain vs Frequency

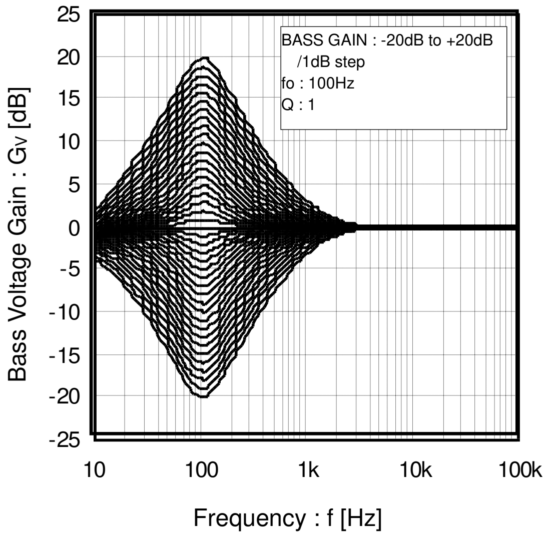


Figure 4. Bass Voltage Gain vs Frequency

Typical Performance Curves - continued

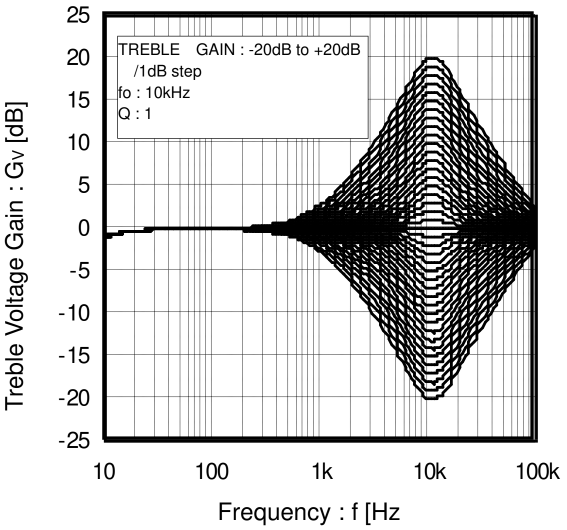


Figure 5. Treble Voltage Gain vs Frequency

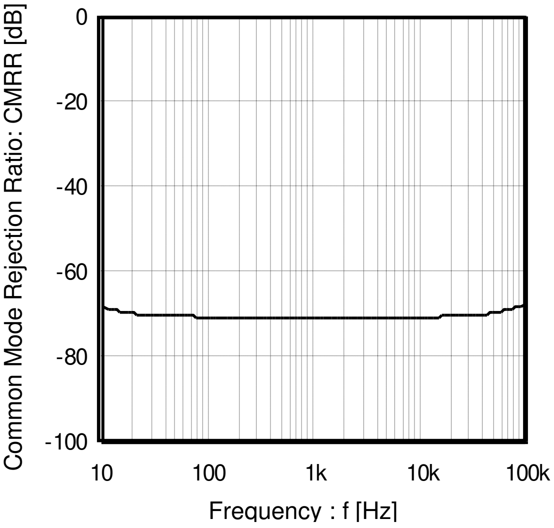


Figure 6. Common Mode Rejection Ratio vs Frequency

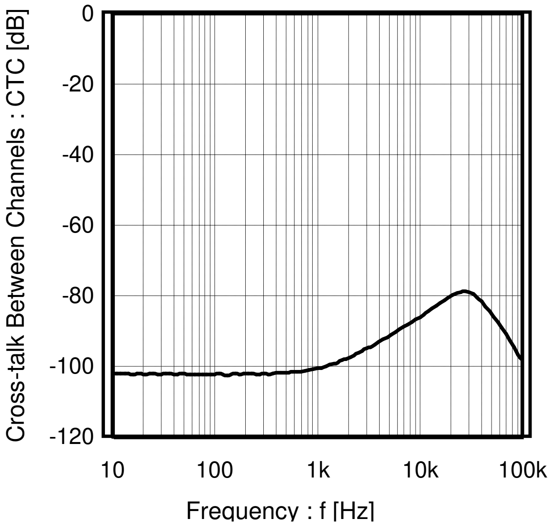


Figure 7. Cross-Talk Between Channels vs Frequency

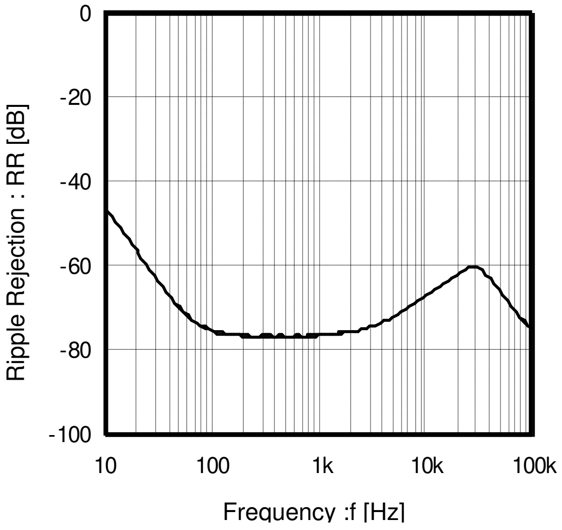


Figure 8. Ripple Rejection Ratio vs Frequency

Typical Performance Curves - continued

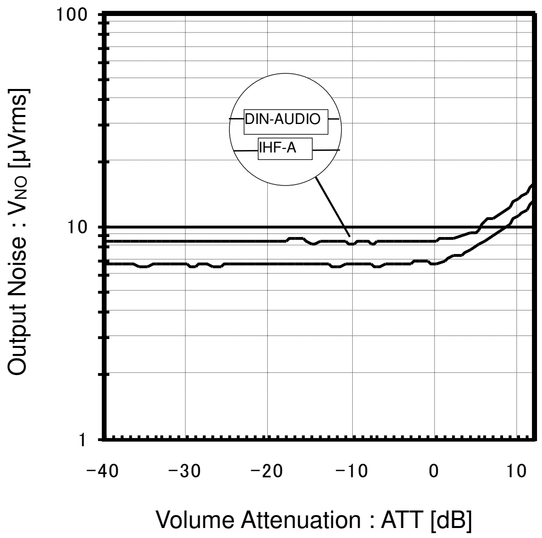


Figure 9. Output Noise vs Volume Attenuation

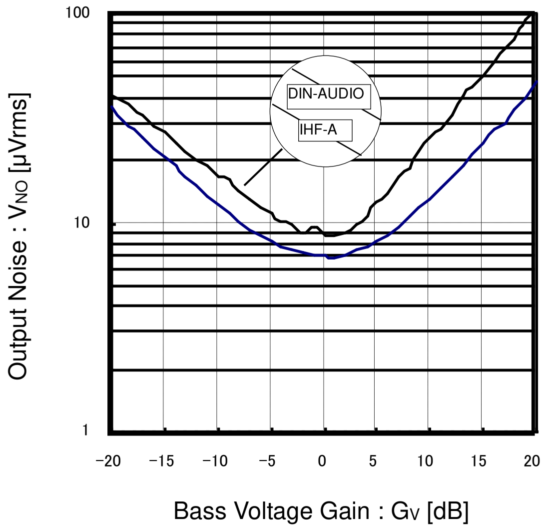


Figure 10. Output Noise vs Bass Voltage Gain

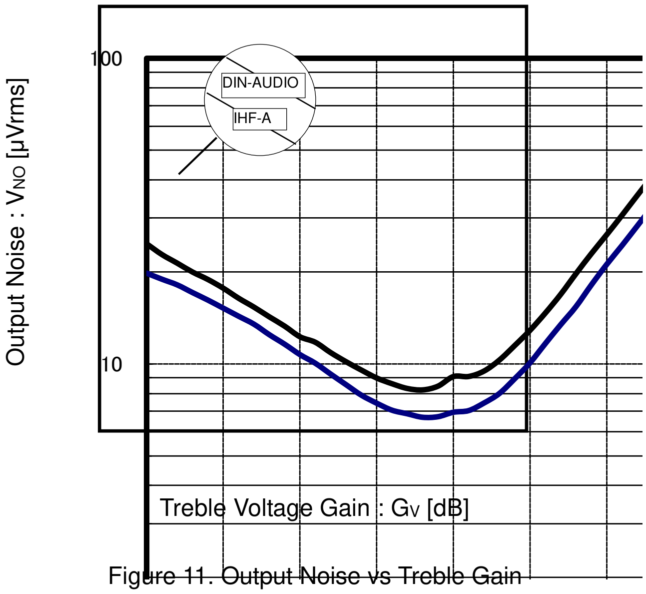


Figure 11. Output Noise vs Treble Gain

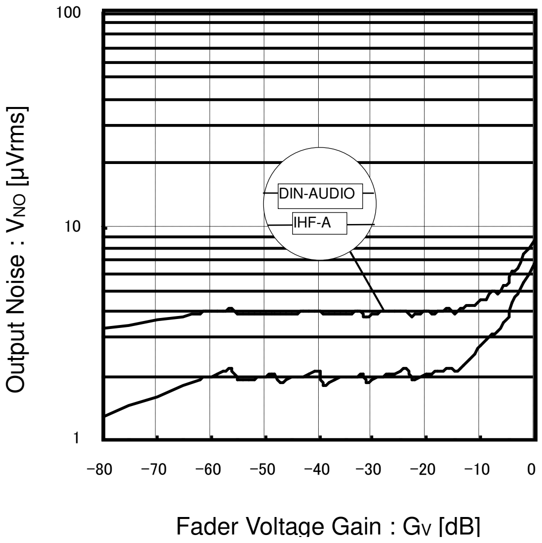


Figure 12. Output Noise vs Fader Gain

Typical Performance Curves - continued

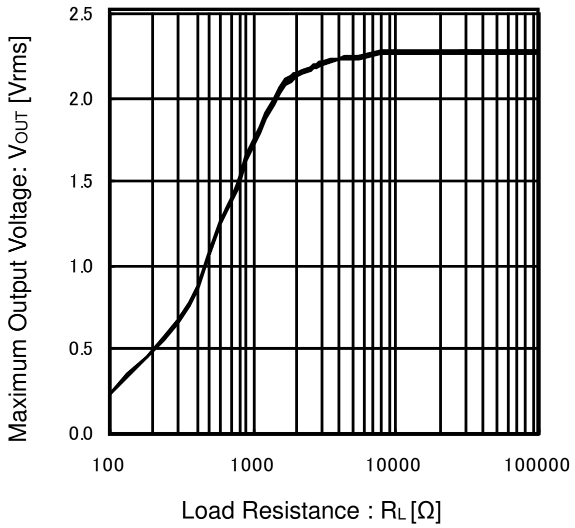


Figure 13. Maximum Output Voltage vs Load Resistance

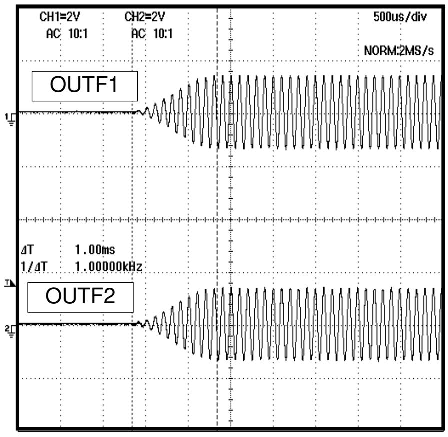


Figure 14. Advanced Switch 1

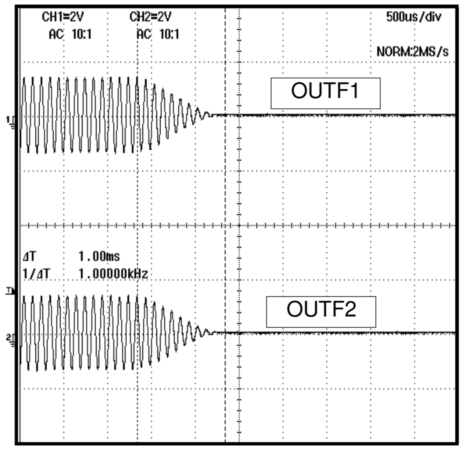


Figure 15. Advanced Switch 2

Timing Chart

Control Signal Specification

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

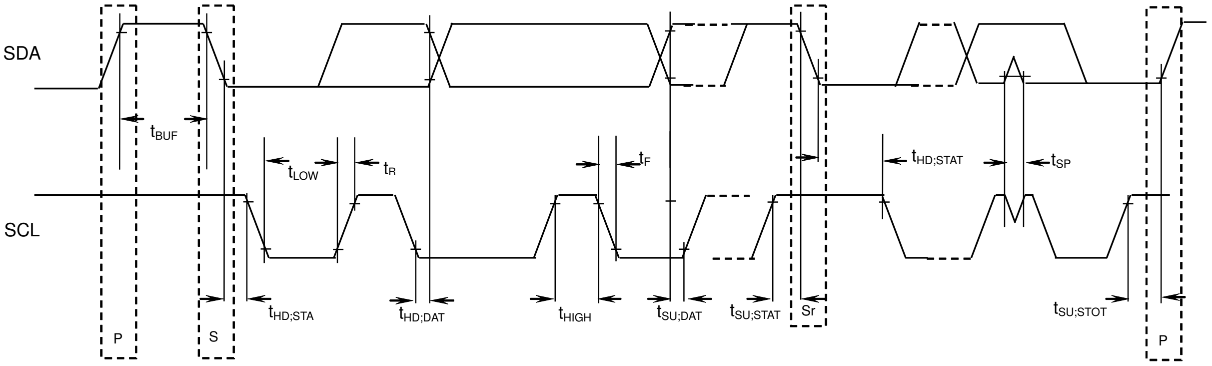


Figure 16. I^{2}C-bus Signal Timing Diagram

Table 1 Characteristics of the SDA and SCL bus lines for I^{2}C-bus devices

Parameter		Symbol	Fast-mode I^{2}C-bus		Unit
			Min	Max	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	μS
4	LOW period of the SCL clock	t_{LOW}	1.3	-	μS
5	HIGH period of the SCL clock	t_{HIGH}	0.6	-	μS
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	μS
7	Data hold time:	$t_{HD;DAT}$	0.7 (Note)	-	μS
8	Data set-up time	$t_{SU;DAT}$	700	-	ns
9	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	μS

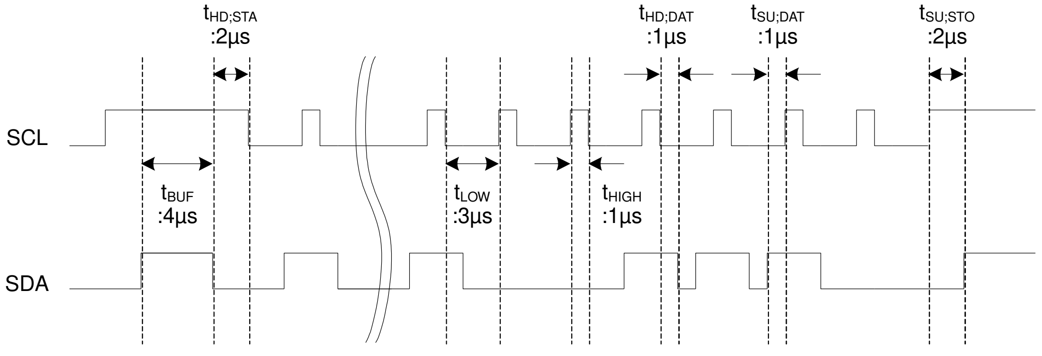
All values referred to VIH Min and VIL Max Levels (see Table 2).

(Note) To avoid sending right after the fall-edge of SCL (VIHmin of the SCL signal), the transmitting device should set a hold time of 300ns or more for the SDA signal.

For 7($t_{HD;DAT}$), 8($t_{SU;DAT}$), make the setup in which the margin is fully in.

Table 2 Characteristics of the SDA and SCL I/O stages for I^{2}C-bus devices

Parameter		Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage:	V_{IL}	-0.3	+1	V
11	HIGH level input voltage:	V_{IH}	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	0	50	ns
13	LOW level output voltage: at 3mA sink current	V_{OL1}	0	0.4	V
14	Input current of each I/O pin with an input voltage between 0.4V and 4.5V.	I_I	-10	+10	μA



SCL clock frequency : 250kHz

Figure 17. I^{2}C Data Transmission Command Timing Diagram

(2) I^2C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start condition (Recognition of start bit)
Slave Address = Recognition of slave address. The first 7 bits correspond to the slave address. The least significant bit is “L” which corresponds to write mode.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select address corresponding to volume, bass or treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

(3) I^2C BUS Interface Protocol

(a) Basic Format

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

(b) Automatic Increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	· · · ·	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

80H

(5) Select Address & Data

Items	Select Address (hex)	**MSB**			**Data**				**LSB**
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Volume/Tone/Fader		0	0	Advanced switch time of Mute	
Input Selector	04	0	0	0	0	0	Input selector		
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	1	0	Volume Attenuation					
Fader 1ch Front	28	1	0	Fader Attenuation					
Fader 2ch Front	29	1	0	Fader Attenuation					
Fader 1ch Rear	2A	1	0	Fader Attenuation					
Fader 2ch Rear	2B	1	0	Fader Attenuation					
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
System Reset	FE	1	0	0	0	0	0	0	1

▨ Advanced switch

Note

1. The Advanced Switch works in the latch part while changing from one function to another.
2. When changing a tone into the cut from the boost, or the cut and the boost, always go via the condition of the tone 0dB.
3. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.

→01→04→06→20→28→29→2A→2B→51→57

4. For the function of Input Selector etc, Advanced Switch is not used. Therefore, please apply mute on the set side when changing these settings.
5. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF while waiting for advanced-mute time.

Select address 01 (hex)

Mode	**MSB**	**Advanced switch time of Mute**						**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Volume/Tone/Fader		0	0	0	0
1.2msec							0	1
2.4msec							1	0
4.8msec							1	1

Mode	**MSB**	**Advanced switch time of Volume/Tone/Fader**						**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
4.6 msec	Advanced Switch ON/OFF	0	0	0	0	0	Advanced switch Time of Mute	
9.3 msec			0	1				
18.6 msec			1	0				
37.2 msec			1	1				

Mode	**MSB**	**Advanced switch ON/OFF**						**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Volume/Tone/Fader		0	0	Advanced switch Time of Mute	
ON	1							

Select address 04(hex)

Mode	**MSB**	**Input Selector**						**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
A	0	0	0	0	0	0	0	0
B						0	0	1
C						0	1	0
SHORT						1	0	1
INPUT MUTE						1	1	0
						1	1	1

▨ :Initial condition

SHORT : The input impedance of each input terminal is lowered from 100kΩ(TYP) to 6 kΩ(TYP).
(For quick charge of coupling capacitor)

INPUT MUTE : Mute is done at the input signal in the part of Input Selector.

Select address 06 (hex)

Gain	MSB				Input Gain			LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

(Note) In case sending prohibited data, 0dB is set.

Mode	MSB				Mute ON/OFF			LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	Input Gain				
ON	1							

▨ :Initial condition

Select address 20 (hex)

Gain & ATT	**MSB**				**Vol Attenuation**			**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	1	0	0	0	0	0	0	0
-1dB			0	0	0	0	0	1
-2dB			0	0	0	0	1	0
· · ·			· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
-38dB			1	0	0	1	1	0
-39dB			1	0	0	1	1	1
-40dB			1	0	1	0	0	0
Prohibition			1	0	1	0	0	1
			:	:	:	:	:	:
			1	1	1	1	1	0
			1	1	1	1	1	1

(Note) In case sending prohibited data, -40dB is set.

Select address 28, 29, 2A, 2B (hex)

Gain & ATT	**MSB**				**Fader Attenuation**			**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	1	0	0	0	0	0	0	0
-1dB			0	0	0	0	0	1
-2dB			0	0	0	0	1	0
· · ·			· · ·	· · ·	· · ·	· · ·	· · ·	· · ·
-61dB			1	1	1	1	0	1
-62dB			1	1	1	1	1	0
-∞dB			1	1	1	1	1	1

▨ : Initial condition

Select address 51, 57 (hex)

Gain	**MSB**			**Bass/Treble Gain**				**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	0
				1	1	1	1	1

(Note) In case sending prohibited data, 0dB is set.

Mode	**MSB**			**Bass/Treble Boost/Cut**				**LSB**
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Treble Gain				
Cut	1							

▨ :Initial condition

(6) About Power ON Reset

Built-in IC initialization is made during power on of the supply voltage. Please send initial data to all addresses at supply voltage on. And please turn ON mute at the set side until this initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t_{RISE}	20	-	-	µsec	V_{CC} rise time from 0V to 3V
VCC Voltage of Release Power ON Reset	V_{POR}	-	4.1	-	V	

(7) About External Compulsory Mute Terminal

It is possible to force mute externally by setting an input voltage to the MUTE terminal.

Mute Voltage Condition	Mode
GND to 1.0V	MUTE ON
2.3V to V_{CC}	MUTE OFF

Establish the voltage of MUTE in the condition to be defined.

Application Information

1. Function and Specifications

Function	Specifications
Input selector	・ Stereo 3 input
Input gain	・ 0dB to 20dB
Mute	・ Possible to use “Advanced switch” for prevention of switching noise.
Volume	・ 0dB to -40dB (1dB step) ・ Possible to use “Advanced switch” for prevention of switching noise.
Bass	・ -20dB to +20dB (1dB step) ・ Q=1 ・ fo=100Hz ・ Possible to use advanced switch at changing gain
Treble	・ -20dB to +20dB (1dB step) ・ Q=1 ・ fo=10kHz ・ Possible to use advanced switch at changing gain
Fader	・ 0dB to -62dB(1dB step), -∞dB ・ Possible to use “Advanced switch” for prevention of switching noise.

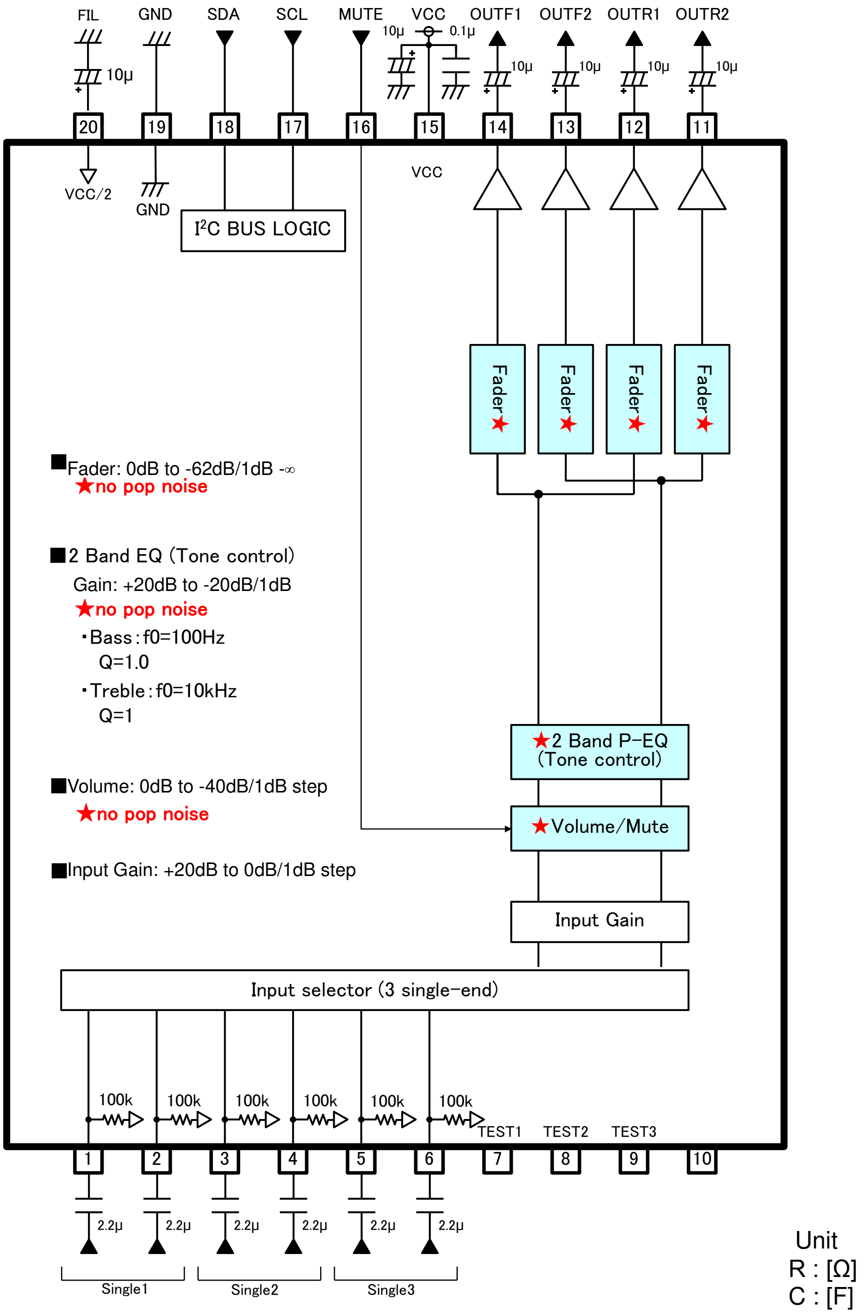
2. Volume / Fader Volume Attenuation Data

(dB)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0
-1			0	0	0	0	0	1
-2			0	0	0	0	1	0
-3			0	0	0	0	1	1
-4			0	0	0	1	0	0
-5			0	0	0	1	0	1
-6			0	0	0	1	1	0
-7			0	0	0	1	1	1
-8			0	0	1	0	0	0
-9			0	0	1	0	0	1
-10			0	0	1	0	1	0
-11			0	0	1	0	1	1
-12			0	0	1	1	0	0
-13			0	0	1	1	0	1
-14			0	0	1	1	1	0
-15			0	0	1	1	1	1
-16			0	1	0	0	0	0
-17			0	1	0	0	0	1
-18			0	1	0	0	1	0
-19			0	1	0	0	1	1
-20			0	1	0	1	0	0
-21			0	1	0	1	0	1
-22			0	1	0	1	1	0
-23			0	1	0	1	1	1
-24			0	1	1	0	0	0
-25			0	1	1	0	0	1
-26			0	1	1	0	1	0
-27			0	1	1	0	1	1
-28			0	1	1	1	0	0
-29			0	1	1	1	0	1
-30			0	1	1	1	1	0
-31			0	1	1	1	1	1
-32	1	0	1	0	0	0	0	0
-33			1	0	0	0	0	1
-34			1	0	0	0	1	0
-35			1	0	0	0	1	1
-36			1	0	0	1	0	0
-37			1	0	0	1	0	1
-38			1	0	0	1	1	0
-39			1	0	0	1	1	1
-40			1	0	1	0	0	0
-41			1	0	1	0	0	1
-42			1	0	1	0	1	0
-43			1	0	1	0	1	1
-44			1	0	1	1	0	0
-45			1	0	1	1	0	1
-46			1	0	1	1	1	0
-47			1	0	1	1	1	1
-48			1	1	0	0	0	0
-49			1	1	0	0	0	1
-50			1	1	0	0	1	0
-51			1	1	0	0	1	1
-52			1	1	0	1	0	0
-53			1	1	0	1	0	1
-54			1	1	0	1	1	0
-55			1	1	0	1	1	1
-56			1	1	1	0	0	0
-57			1	1	1	0	0	1
-58			1	1	1	0	1	0
-59			1	1	1	0	1	1
-60			1	1	1	1	0	0
-61			1	1	1	1	0	1
-62			1	1	1	1	1	0
▨ -∞			▨ 1	▨ 1	▨ 1	▨ 1	▨ 1	▨ 1

For Volume attenuation, only 0dB to -40dB are available.

▨ : Initial condition

3. Application Circuit



Notes on wiring

① Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
② GND lines should be one-point connected.
③ Wiring pattern of Digital should be away from that of Analog unit and cross-talk should not be acceptable.
④ SCL and SDA lines of I²C BUS should not be parallel if possible.
The lines should be shielded, if they are adjacent to each other.
⑤ Analog input lines should not be parallel if possible. The lines should be shielded, if they are adjacent to each other.
⑥ For TEST pins (Pin 7,8,9), please leave them as OPEN.

Power Dissipation

About the thermal design of the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy the device. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

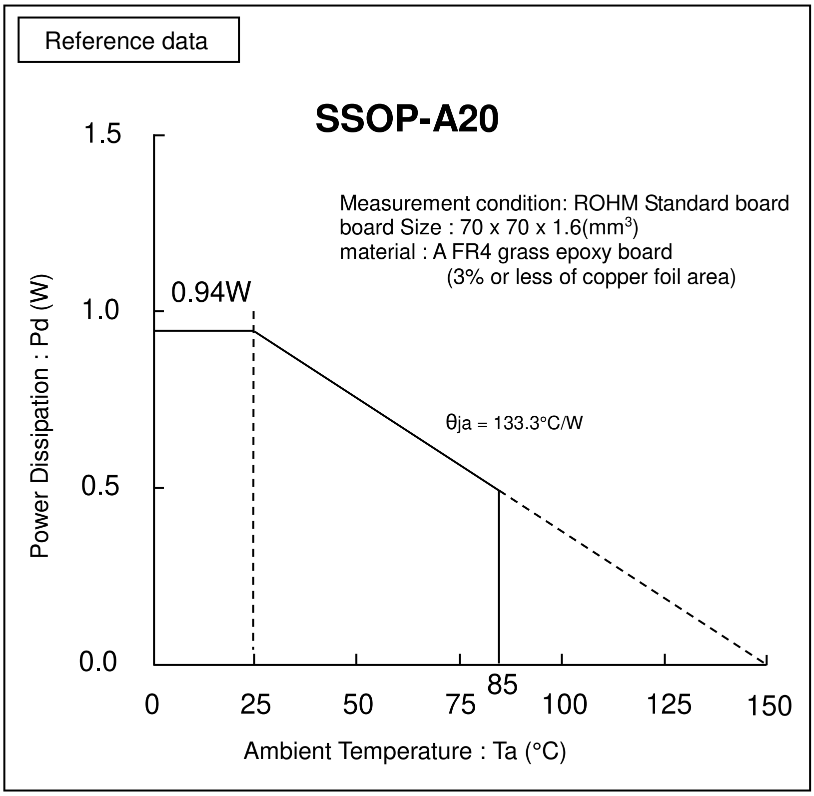
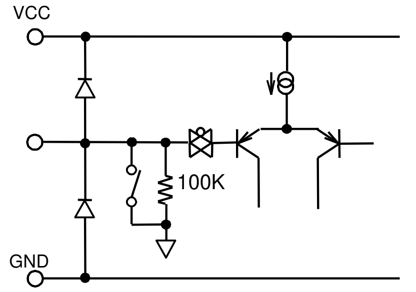
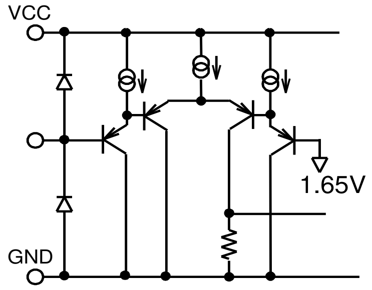
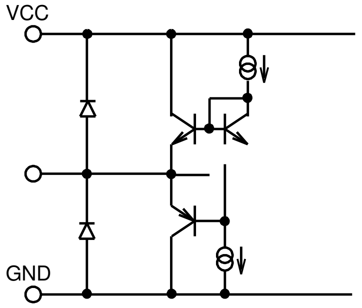
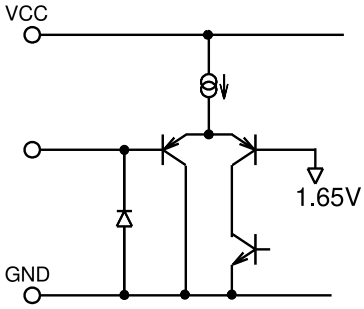


Figure 18. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

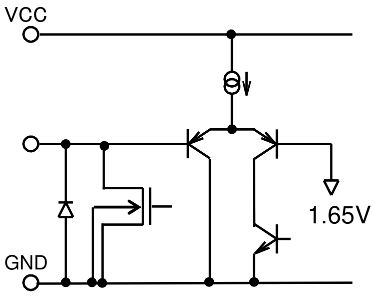
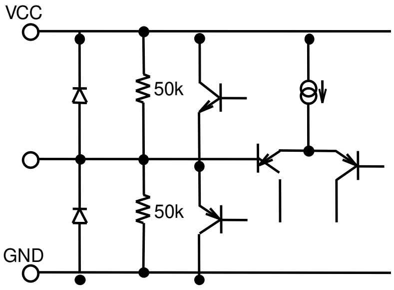
Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ(typ).
16	MUTE	—		A terminal for external compulsory mute. If terminal voltage is High level, the mute is off. And if the terminal voltage is Low level, the mute is on.
11 12 13 14	OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader and Subwoofer output.
15	VCC	8.5		Power supply terminal.
17	SCL	-		A terminal for clock input of I^{2}C BUS communication.

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

I/O Equivalent Circuits - continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
18	SDA	-		A terminal for data input of I^{2}C BUS communication.
19	GND	0		Ground terminal.
20	FIL	4.25		Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
7 8 9	TEST1 TEST2 TEST3	-		TEST terminal.

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

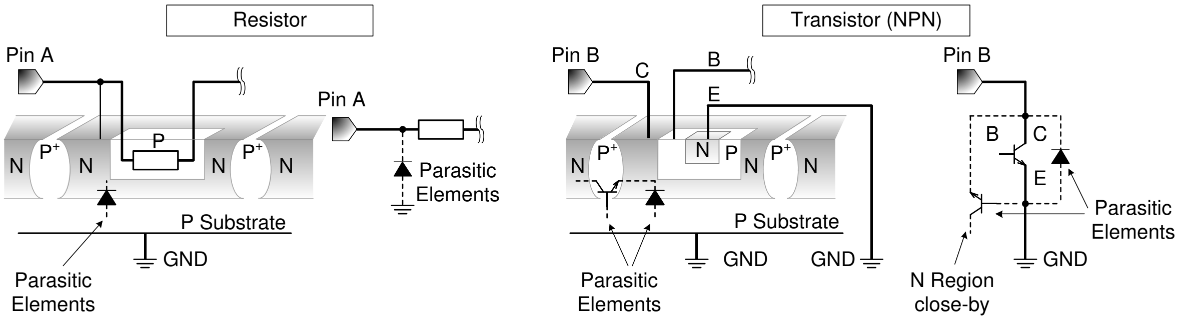
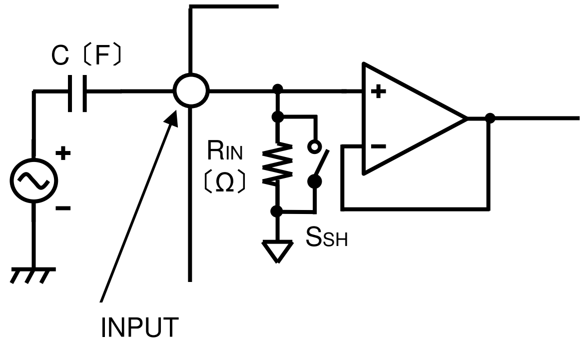


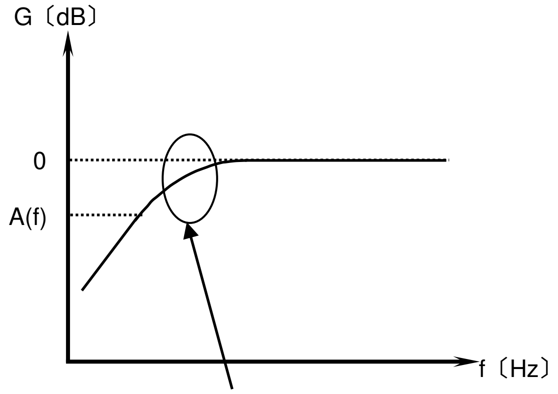
Figure 19. Example of monolithic IC structure

13. About a Signal Input Part

(a) About Input Coupling Capacitor Constant Value

In the input signal terminal, please decide the constant value of the input coupling capacitor C(F) that would be sufficient to form an RC characterized HPF with input impedance R_{IN}(Ω) inside the IC.





$$A(f)=\sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

(b) About the Input Selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON of input selector part so that the input impedance R_{IN} of all terminals becomes small. Switch S_{SH} is OFF when SHORT command is not selected.
The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at no signal condition.

14. About Mute Terminal(Pin 16) when power supply is OFF

There should be no applied voltage across the Mute terminal (Pin 16) when power-supply is OFF.
A resistor (about 2.2kΩ) should be connected in series to Mute terminal in case a voltage is supplied to Mute terminal. (Please refer Application Circuit Diagram.)

15. About TEST Pin

TEST Pin, should be OPEN.
Pin 9, 8, 7 are TEST Pins.

Ordering Information

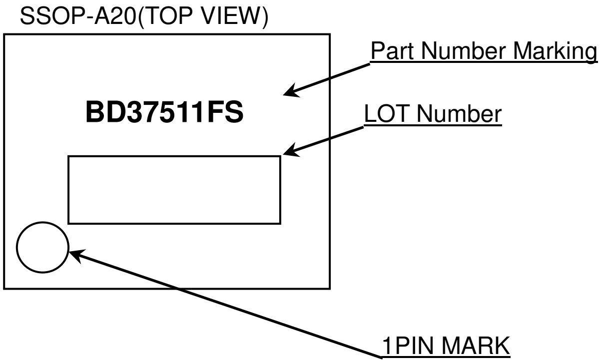
B D 3 7 5 1 1 F S - E 2

Part Number

Package
FS: SSOP-A20

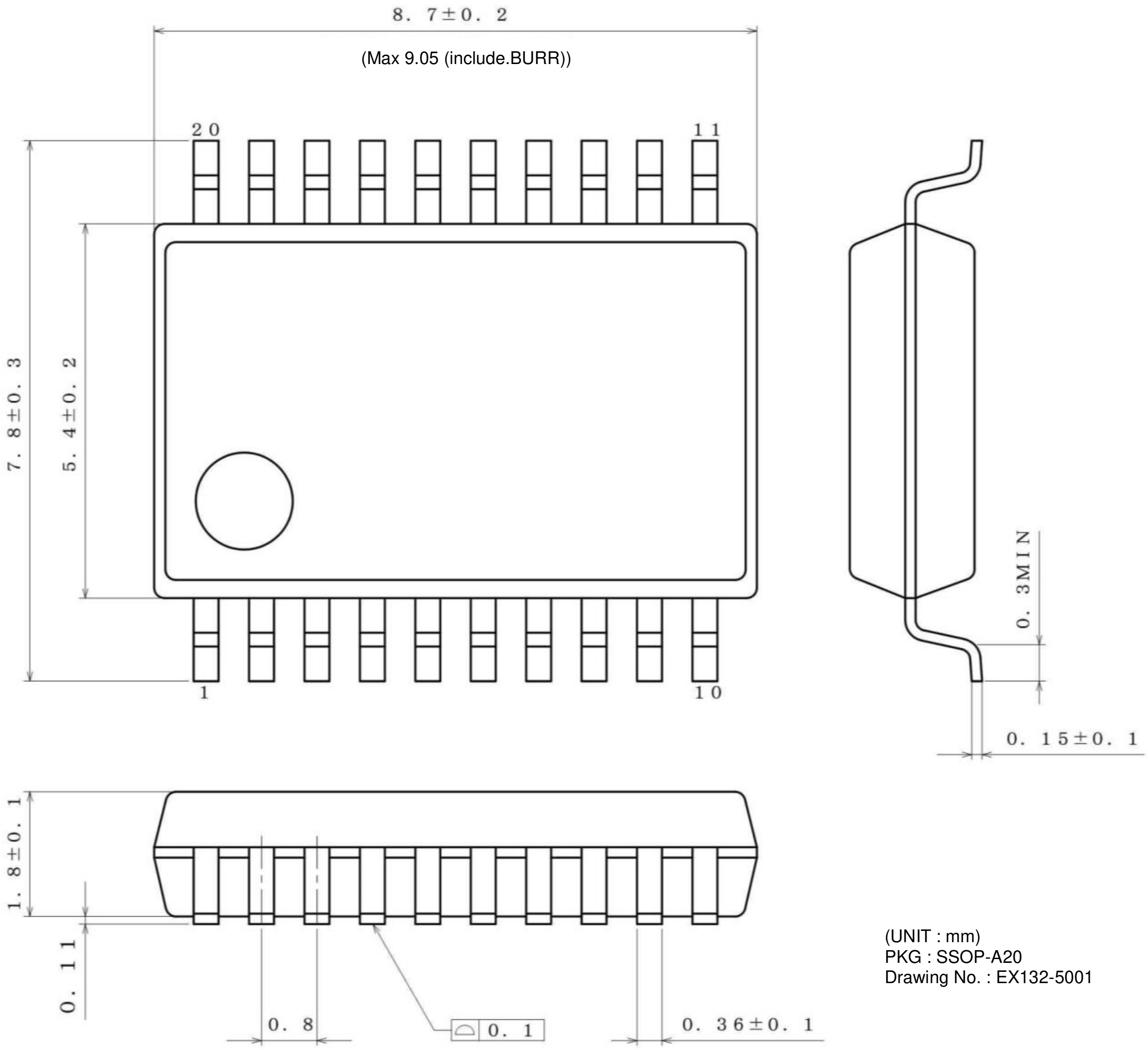
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



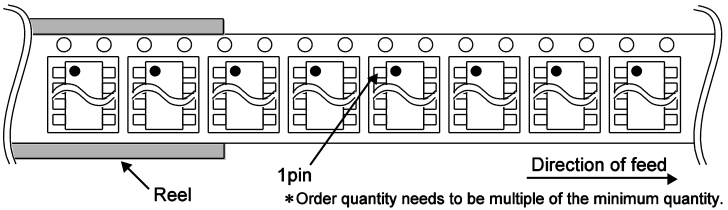
Physical Dimension, Tape and Reel Information

Package Name	SSOP-A20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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