

User's Guide

NHD-0440AZ-FL-GBW

LCM

(Liquid Crystal Display Character Module)

RoHS Compliant

FEATURES

- Display format: 4 Lines x 40 Characters
- **(A)** – Display Series/Model
- **(Z)** – Factory line
- **(F)** – Polarizer = Transflective (+) light method
- **(L)** – Backlight = LED (Yellow-Green)
- **(G)** – LCD Type = STN- Gray
- **(B)** – View Direction = 6:00
- **(W)** – Operating Temp. =Wide (-20 ~ +70c)

LCD driver IC: SPLC780D

For product support, contact

Newhaven Display International, LLC
2511 Technology Drive, #101
Elgin, IL 60124

Tel: (847) 844-8795 Fax: (847) 844-8796

October 16, 2007

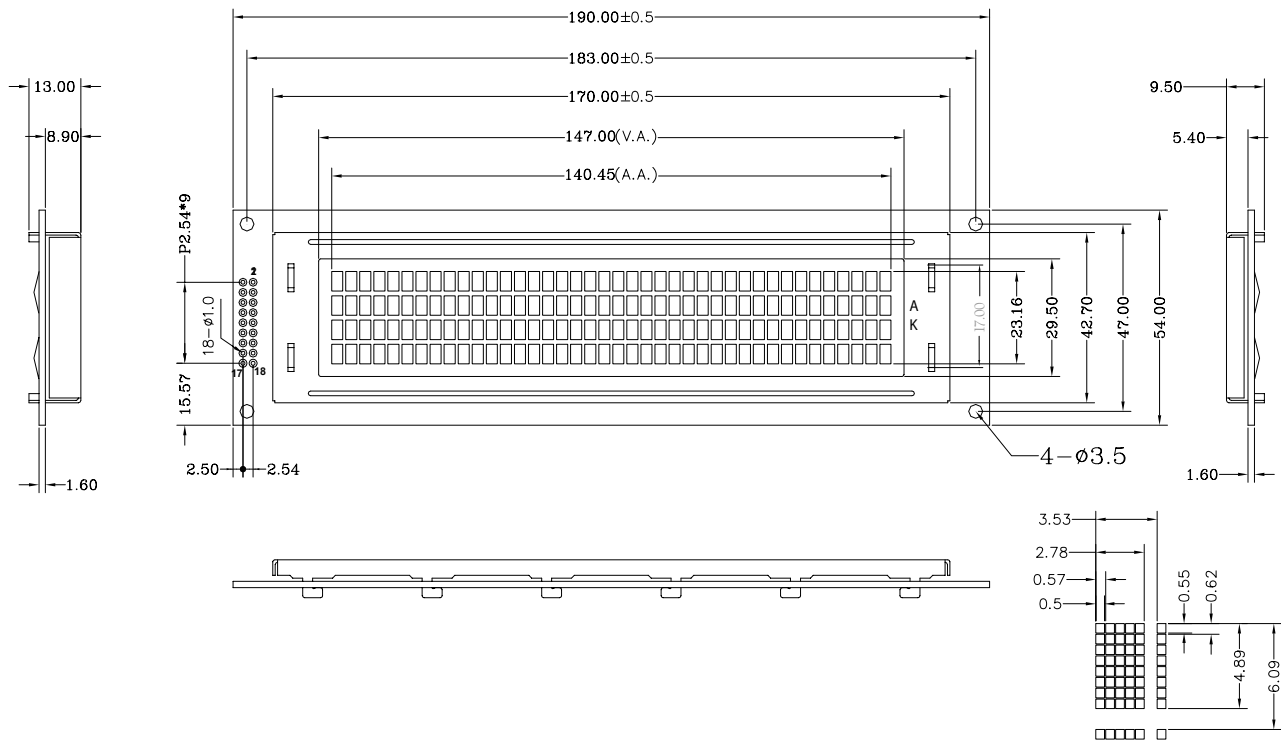
NHD-0440AZ-FL-GBW

SPECIFICATIONS OF LCD MODULE

Features

1. 5x8 dots with cursor
2. Display format: 40characters * 4 lines
3. Built-in controller (SPLC780D)
4. +5V power supply
5. 1/16 duty, 1/5 bias cycle
6. STN- GRAY, Transflective; Positive display
7. Viewing direction: 6:00 o'clock

Outline dimension



Absolute maximum ratings

| Item | Symbol | Standard | Unit |
|-----------------------------|-----------------|----------|----------|
| Power voltage | $V_{DD}-V_{SS}$ | 0 | 7.0 |
| Input voltage | V_{IN} | V_{SS} | V_{DD} |
| Operating temperature range | V_{OP} | -20 | +70 |
| Storage temperature range | V_{ST} | -30 | +80 |

*Wide temperature range is available

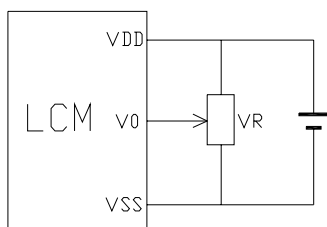
NHD-0440AZ

Interface pin description

| Pin no. | Symbol | External connection | Function |
|---------|-----------------|---------------------|---|
| 1~4 | DB7~DB4 | MPU | Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU |
| 5~8 | DB3~DB0 | MPU | Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation. |
| 9 | E1 | MPU | Operation (data read/write) enable signal |
| 10 | R/W | MPU | Read/write select signal |
| 11 | RS | MPU | Register select signal |
| 12 | V ₀ | Power supply | Contrast adjust |
| 13 | V _{SS} | | Signal ground for LCM (GND) |
| 14 | V _{DD} | | Power supply for logic (+5V) for LCM |
| 15 | E2 | MPU | Enable signal (no pull-up resistor) |
| 16 | NC | | |
| 17 | LED+ | Power supply | Power supply for LED backlight (+5V) |
| 18 | LED- | | Power supply for LED backlight (0V) |

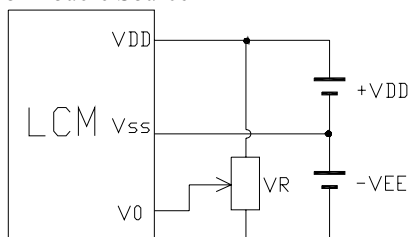
Contrast adjust

A) For Single Source



For Module with Normal Temperature Range Fluid

B) For Double Source



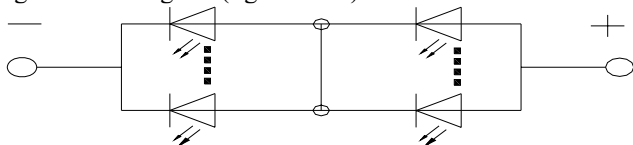
For Module with Extended Temperature Range Fluid or wide viewing cone fluid

V_{DD}-V₀: LCD Driving voltage

VR: 1k~2k

Electrical characteristics

Backlight circuit diagram (light 48 x 2)



led ratings (Yellow/Green)

(UAK = 4.2V, Ta =25°C)

| Item | Symbol | Min | Typ. | Max | Unit |
|------------------|----------------|-----|------|------|-------------------|
| Forward Voltage | VAK | 3.6 | 4.2 | 4.3 | V |
| Forward current | I _f | - | 480 | 500 | mA |
| Power | P | | | 2016 | mW |
| Peak wave length | λ _p | | 570 | | nm |
| Luminance | L _v | | 80 | | Cd/m ² |

NHD-0440AZ

STN type display module (Ta=25°C, VDD=5.0V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------|----------|--------------|------|------|------|------|
| Viewing angle | θ | $C_r \geq 2$ | -60 | - | 35 | deg |
| | Φ | | -40 | - | 40 | |
| Contrast ratio | C_r | | - | 6 | - | - |
| Response time (rise) | T_r | - | - | 150 | 250 | ms |
| Response time (fall) | T_r | - | - | 150 | 250 | |

Electrical characteristics

DC characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|--------------|-----------------------------|------|------|----------|------|
| Supply voltage for LCD | $V_{DD}-V_0$ | Ta=25°C | - | 5.0 | - | V |
| Input voltage | V_{DD} | | 2.7 | - | 5.5 | |
| Supply current | I_{DD} | Ta=25°C, VDD=5.0V | - | 3.5 | 4.0 | mA |
| Input leakage current | I_{LKG} | | - | - | 5.0 | uA |
| “H” level input voltage | V_{IH} | | 2.2 | - | V_{DD} | V |
| “L” level input voltage | V_{IL} | Twice initial value or less | 0 | - | 0.6 | |
| “H” level output voltage | V_{OH} | LOH=-0.25mA | 2.4 | - | - | |
| “L” level output voltage | V_{OL} | LOH=1.6mA | - | - | 0.4 | |
| Backlight supply voltage | V_F | | - | - | 5.0 | |
| Backlight supply current | I_F | $V_F=5.0V$ | - | 480 | - | mA |

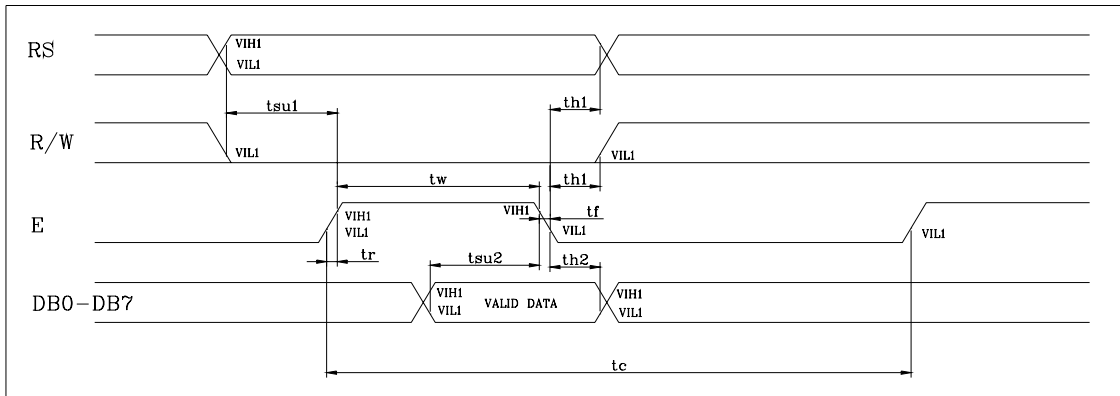
Read cycle (Ta=25°C, VDD=5.0V)

| Parameter | Symbol | Test pin | Min. | Typ. | Max. | Unit |
|---------------------------|------------|----------|------|------|------|------|
| Enable cycle time | t_c | E | 500 | - | - | ns |
| Enable pulse width | t_w | | 300 | - | - | |
| Enable rise/fall time | t_r, t_f | | - | - | 25 | |
| RS; R/W setup time | t_{su} | RS; R/W | 100 | - | - | |
| RS; R/W address hold time | t_h | RS; R/W | 10 | - | - | |
| Read data output delay | t_d | DB0~DB7 | 60 | - | 90 | |
| Read data hold time | t_{dh} | | 20 | - | - | |

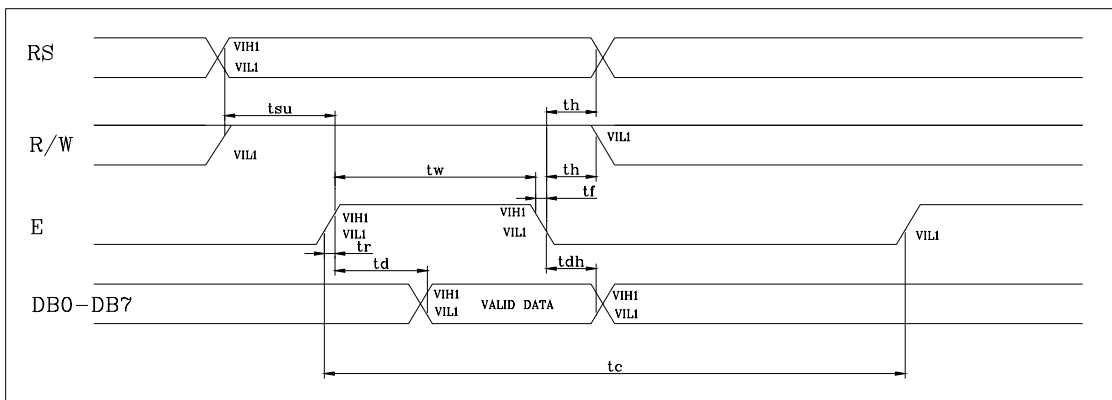
Write cycle (Ta=25°C, VDD=5.0V)

| Parameter | Symbol | Test pin | Min. | Typ. | Max. | Unit |
|---------------------------|------------|----------|------|------|------|------|
| Enable cycle time | t_c | E | 500 | - | - | ns |
| Enable pulse width | t_w | | 300 | - | - | |
| Enable rise/fall time | t_r, t_f | | - | - | 25 | |
| RS; R/W setup time | t_{su1} | RS; R/W | 100 | - | - | |
| RS; R/W address hold time | t_{h1} | RS; R/W | 10 | - | - | |
| Read data output delay | t_{su2} | DB0~DB7 | 60 | - | - | |
| Read data hold time | t_{h2} | | 10 | - | - | |

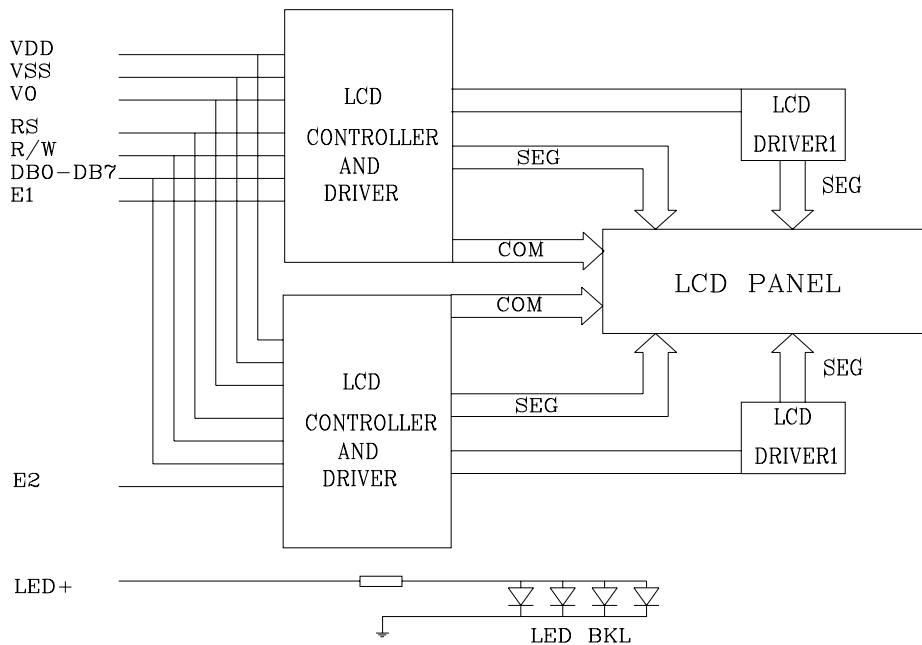
Write mode timing diagram



Read mode timing diagram



Block diagram



Instruction description

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).

Instructions can be divided largely into four groups:

- 1) KS0066U function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read “High”.

Busy flag check must be preceded by the next instruction.

When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2 fuss for executing the next instruction by the falling edge of the “E” signal after the busy flag (DB7) goes to “LOW”.

Contents

- 1) Clear display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, brings the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

- 2) Return home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

- 3) Entry mode set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | I/D | SH |

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D=“high”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D=“Low”, cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

(I/D=“high”. shift left, I/D=“Low”. Shift right).

4) Display ON/OFF control

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D="High", entire display is turned on.

When D="Low", display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D="High", cursor is turned on.

When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor blink ON/OFF control bit

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.

When B="Low", blink is off.

5) Cursor or display shift

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - |

Shifting of right/left cursor position or display without writing or reading of display data.

This instruction is used to correct or search display data. (Refer to Table 6)

During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

When display data is shifted repeatedly, each line is shifted individually.

When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and R/L bits

| S/C | R/L | Operation |
|-----|-----|---|
| 0 | 0 | Shift cursor to the left, AC is decreased by 1 |
| 0 | 1 | Shift cursor to the right, AC is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

6) Function set

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - |

DL: Interface data length control bit

When DL="High", it mans 8-bit bus mode with MPU.

When DL="Low", it mans 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N="Low", 1-line display mode is set.

When N="High", 2-line display mode is set.

NHD-0440AZ

F: Display line number control bit

When F="Low", 5x8 dots format display mode is set.

When F="High", 5x11 dots format display mode.

7) Set CGRAM address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

8) Set DDRAM address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=LOW), DDRAM address is form "00H" to "4FH".

In 2-line display mode (N=High), DDRAM address in the 1st line form "00H" to "27H", and DDRAM address

In the 2nd line is from "40H" to "67H".

9) Read busy flag & address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether KS0066U is in internal operation or not.

If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then if the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).

RAM set instruction can also determine the AC direction to RAM.

After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction,

It also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

Instruction table

| Instruction | Instruction code | | | | | | | | | | Description | Execution Time (fosc= 270 KHZ) | |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------------|--|--------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRA and set DDRAM address to "00H" from AC | 1.53ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - | Set DDRAM address to "00H" From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed. | 1.53ms |
| Entry mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction And blinking of entire display | 39us |
| Display ON/OFF control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit. | |
| Cursor or Display shift | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - | Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data. | 39us |
| Function set | 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - | - | Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8) | 39us |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set CGRAM address in address Counter. | 39us |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set DDRAM address in address Counter. | 39us |
| Read busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read. | 0us |
| Write data to Address | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Write data into internal RAM (DDRAM/CGRAM). | 43us |
| Read data From RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Read data from internal RAM (DDRAM/CGRAM). | 43us |

NOTE: When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

DDRAM address:

| | | | | | | | | | | | | | | | Display position | | | | |
|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------------------|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | - | - | - | - | - | - | - | - | - | - | 36 | 37 | 38 | 39 | 40 |
| 00 | 01 | 02 | 03 | 04 | - | - | - | - | - | - | - | - | - | - | 23 | 24 | 25 | 26 | 27 |
| 40 | 40 | 41 | 42 | 43 | - | - | - | - | - | - | - | - | - | - | 63 | 64 | 65 | 66 | 67 |
| 00 | 01 | 02 | 03 | 04 | - | - | - | - | - | - | - | - | - | - | 23 | 24 | 25 | 26 | 27 |
| 40 | 40 | 41 | 42 | 43 | - | - | - | - | - | - | - | - | - | - | 63 | 64 | 65 | 66 | 67 |

DDRAM address

Standard character pattern

| Lower 4 Bits \ Upper 4 Bits | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|-----------------------------|------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxxx0000 | CG RAM (1) | | 0 | a | P | ` | P | | | | - | 9 | 3 | o | p | |
| xxxx0001 | (2) | | ! | 1 | A | Q | a | 9 | | | o | A | 4 | o | 9 | |
| xxxx0010 | (3) | | " | 2 | B | R | b | r | | | 「 | イ | ツ | × | β | θ |
| xxxx0011 | (4) | | # | 3 | C | S | c | s | | | 」 | ウ | テ | モ | ε | ∞ |
| xxxx0100 | (5) | | \$ | 4 | D | T | d | t | | | 、 | エ | ト | ホ | μ | Ω |
| xxxx0101 | (6) | | % | 5 | E | U | e | u | | | ・ | オ | ナ | 1 | ε | ū |
| xxxx0110 | (7) | | & | 6 | F | V | f | v | | | ヲ | カ | ニ | ヨ | ρ | Σ |
| xxxx0111 | (8) | | ' | 7 | G | W | g | w | | | ア | キ | ヌ | ラ | g | π |
| xxxx1000 | (1) | | (| 8 | H | X | h | x | | | イ | ク | ネ | リ | フ | ⊗ |
| xxxx1001 | (2) | |) | 9 | I | Y | i | y | | | ウ | ケ | ル | ル | 1 | γ |
| xxxx1010 | (3) | | * | : | J | Z | j | z | | | エ | コ | ン | レ | j | ≠ |
| xxxx1011 | (4) | | + | ; | K | [| k | { | | | オ | サ | ヒ | ロ | ° | ⊗ |
| xxxx1100 | (5) | | , | < | L | ¥ | l | | | | ホ | シ | フ | ワ | ⊗ | ⊗ |
| xxxx1101 | (6) | | - | = | M |] | m | } | | | ユ | ヌ | ヘ | ン | モ | ÷ |
| xxxx1110 | (7) | | . | > | N | ^ | n | ‡ | | | ヨ | セ | ホ | ° | ñ | |
| xxxx1111 | (8) | | / | ? | O | _ | o | ‡ | | | ッ | リ | マ | ° | ö | ■ |