TPS3704-Q1 Automotive Quad, Triple, Dual, Single Window or Standard Voltage Supervisor

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B
- Designed for high performance and safety:
- Input current (4 channels): I_{DD} = 15 µA maximum
- High threshold accuracy: ±0.25% typical, ±1% maximum
- Built-in precision hysteresis: V_{HYS} (V_{IT} > 800 mV) = 0.75% typical
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware capability up to ASIL A
  - Self test - manual setup
- Designed for a wide range of applications:
- Input voltage range, V_{DD} = 1.7 V to 6V
- Quad, triple, dual, or single voltage supervisor
- Each channel highly configurable
  - Window (OV, UV), UV-only, OV-only options
  - Window tolerance: ±3% to ±11%
  - High threshold resolution: V_{IT} ≤ 0.8 V: 20-mV steps V_{IT} > 0.8 V: Lower of 0.5% or 20-mV steps
- Push-button monitor on all channels
- Reset time delay (t_D): Fixed time delay options
  - Options: 23 fixed time options ranging from 20 µs minimum to 1200 ms maximum
- Multiple output topologies, package type:
- TPS3704xxxO-Q1:open-drain, active-low ($\overline{\text{RESET}}$)
- TPS3704xxxL-Q1: push-pull, active-low ($\overline{\text{RESET}}$)
- TPS3704xxxH-Q1: push-pull, active-high (RESET)

2 Applications

- Advanced Driver Assistance System (ADAS)
- Automotive infotainment and cluster
- HEV/EV
- Body electronics and lighting

3 Description

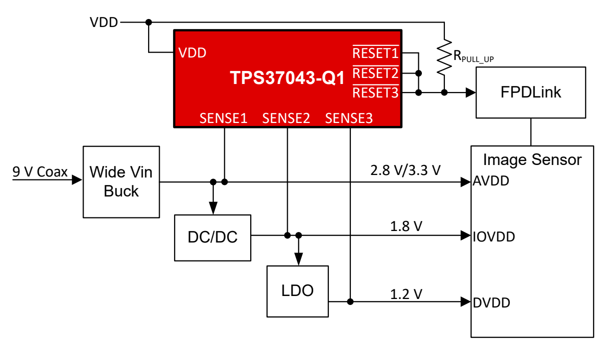
The TPS3704-Q1 is a low-power precision window voltage supervisor that can be configured as a quad, triple, dual, or single channel. Each channel has a threshold accuracy of ±1% in a compact SOT-23 package offering a small solution size. The TPS3704-Q1 includes a very accurate threshold detection, with high resolution, that is ideal for systems that operate on low-voltage supply rails and have narrow margin supply tolerances. Built-in low threshold hysteresis and a fixed reset delay (t_D options from 20 µs to 1200 ms) prevent false reset signals when monitoring multiple voltage rails.

The TPS3704-Q1 does not require any external resistors for setting the over- and undervoltage reset thresholds, which further optimizes overall high accuracy, cost, solution size, and improves reliability for safety systems. The TPS3704-Q1 functional safety compliance elevates automotive design that can meet ISO 26262 requirements and automotive safety integrity levels. Separate VDD and SENSEx pins allow monitoring of rail voltages other than VDD or can be used as a push-button input. Optional use of external resistors are supported by the SENSEx pin(s). Each channel on the TPS3704-Q1 can be customized to its own over- and undervoltage window detection with an upper and lower threshold tolerance that can be symmetric or asymmetric. The TPS3704-Q1 can monitor up to four channels while maintaining an ultra-low I_Q current of 5.5 µA (typical) and operates over a temperature range of –40°C to +125°C (T_A).

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS3704-Q1	DDF (SOT-23 8-pin)	1.6 mm × 2.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (May 2022) — **Page**

- Production Data Release.... 1

5 Device Nomenclature

Figure 5-1 shows the device naming nomenclature to compare the different device variants. See Table 12-1 for a more detailed explanation. See Table 12-2 for the available device variants.

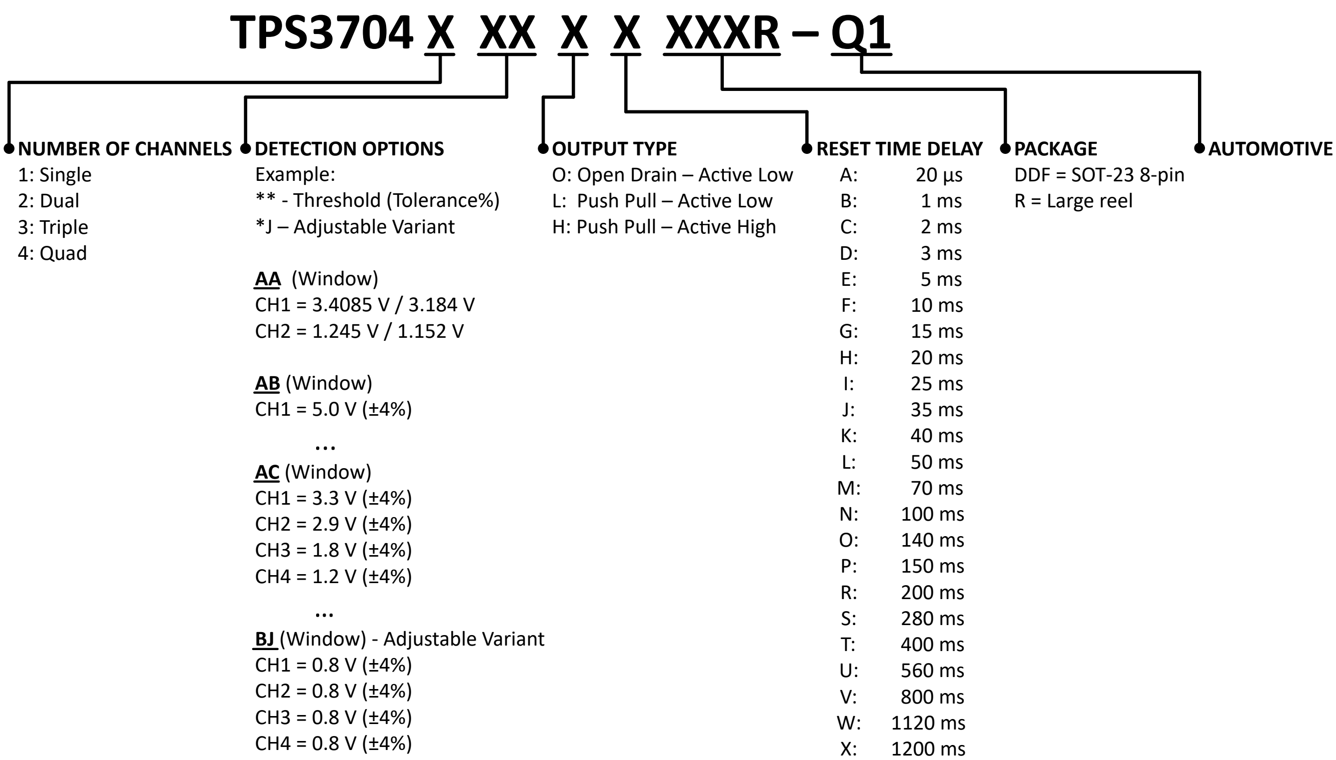


Figure 5-1. Device Naming Convention

6 Pin Configuration and Functions

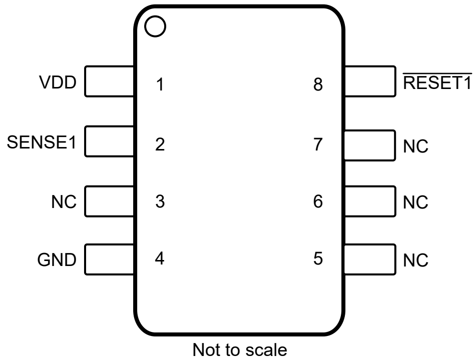


Figure 6-1. DDF Package 8-PIN SOT23 TPS37041-Q1 (Top View)

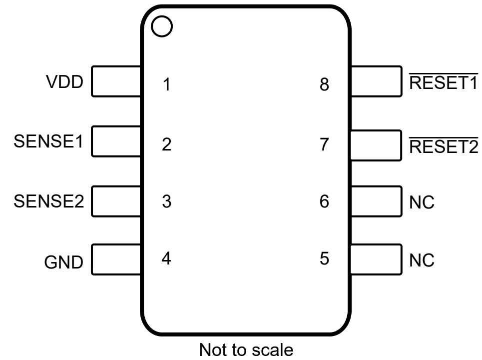


Figure 6-2. DDF Package 8-PIN SOT23 TPS37042-Q1 (Top View)

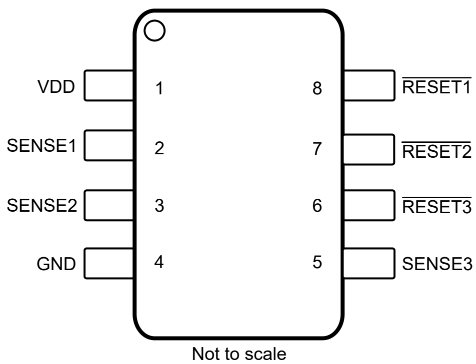


Figure 6-3. DDF Package 8-PIN SOT23 TPS37043-Q1 (Top View)

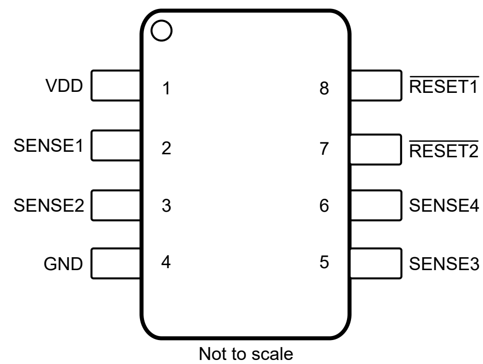


Figure 6-4. DDF Package 8-PIN SOT23 TPS37044-Q1 (Top View)

Table 6-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS37041-Q1	TPS37042-Q1	TPS37043-Q1	TPS37044-Q1		
VDD	1	1	1	1	I	Supply Input. Bypass with a 0.1-µF capacitor to GND.
SENSE1	2	2	2	2	I	Connect directly to a monitored voltage. $\overline{RESET1}$/RESET1 is asserted when SENSE1 falls outside of the window threshold. No external capacitor is required for this SENSE1 pin. For the TPS37044-Q1 (quad version) $\overline{RESET1}$/RESET1 asserts when either SENSE1 or SENSE2 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
SENSE2	—	3	3	3	I	Connect directly to a monitored voltage. $\overline{RESET2}$/RESET2 is asserted when SENSE2 falls outside of window threshold. No external capacitor is required for the SENSE2 pin. For the TPS37044-Q1 (quad version) $\overline{RESET1}$/RESET1 asserts when either SENSE1 or SENSE2 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
SENSE3	—	—	5	5	I	Connect directly to monitored voltage. $\overline{RESET3}$/RESET3 is asserted when SENSE3 falls outside of window threshold. No external capacitor is required for SENSE3 pin. For TPS37044-Q1 (quad version) $\overline{RESET2}$/RESET2 asserts when either SENSE3 or SENSE4 falls outside of window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. If the input pin is not being used, it can be left floating.
SENSE4	—	—	—	6	I	Connect directly to a monitored voltage. For TPS37044-Q1 (quad version) $\overline{RESET2}$/RESET2 asserts when either SENSE3 or SENSE4 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
$\overline{RESET1}$	8	8	8	8	O	$\overline{RESET1}$/RESET1 asserts when SENSE1 falls outside of the overvoltage or undervoltage threshold window. $\overline{RESET1}$/RESET1 stays asserted for the reset timeout period after SENSE1 fall back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. For the TPS37044-Q1, $\overline{RESET1}$/RESET1 asserts when either SENSE1 or SENSE2 falls outside of the window threshold. Leave this pin floating if not used. For the TPS37044F-Q1 option, any SENSEx channels that detect an overvoltage (OV) fault, this pin is asserted.
$\overline{RESET2}$	—	7	7	7	O	$\overline{RESET2}$/RESET2 asserts when SENSE2 falls outside of the overvoltage or undervoltage threshold window. $\overline{RESET2}$/RESET2 stays asserted for the reset timeout period after SENSE2 falls back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. For the TPS37044-Q1, $\overline{RESET2}$/RESET2 asserts when either SENSE3 or SENSE4 fall outside of the window threshold. Leave this pin floating if not used. For the TPS37044F-Q1 option, any SENSEx channels that detect an undervoltage (UV) fault, this pin is asserted.
$\overline{RESET3}$	—	—	6	—	O	$\overline{RESET3}$/RESET3 asserts when SENSE3 falls outside of the overvoltage or undervoltage threshold window. $\overline{RESET3}$/RESET3 stays asserted for the reset timeout period after SENSE3 falls back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. Leave this pin floating if not being used.
GND	4	4	4	4	—	Ground
NC	3,5,6,7	5,6	—	—	—	No connect

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6.5	V
	$V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$, $V_{\overline{RESET3}}$	–0.3	6.5	V
	V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, V_{SENSE4}	–0.3	6.5	V
Current	$I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$,$I_{\overline{RESET3}}$ SINK		±20	mA
Temperature [(2)]	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings (AMR) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to AMR-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011		±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.7		6.0	V
$V_{SENSE1,2,3,4}$	Input pin voltage	0		6.0	V
$V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$, $V_{\overline{RESET3}}$	Output pin voltage	0		6.0	V
$I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$, $I_{\overline{RESET3}}$ SINK	Output pin current sink	0.3		5	mA
T_A	Operating free air temperature	-40		125	℃

7.4 Thermal Information

THERMAL METRIC (1)		TPS3704x-Q1 DDF PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 1.7 V ≤ V_{DD} ≤ 6.0 V, $\overline{RESETx}$ Voltage ($V_{\overline{RESETx}}$) = 10 kΩ to V_{DD}, $\overline{RESETx}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at V_{DD} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.7		6.0	V
UVLO	Under Voltage Lockout (1)	V_{DD} falling below 1.7 V	1.2	1.4	1.6	V
$UVLO_{(HYS)}$	UVLO Hysteresis (2)	V_{DD} rising below 1.7 V		65		mV
V_{POR}	Power on reset voltage (3)	$V_{OL\ (MAX)}$ = 0.3 V, I_{OUT} = 15 µA			0.7	V
V_{IT} Range	Threshold Programming Range		0.4		5.55	V
$V_{IT-\ (UV)}$	UV accuracy (25℃)			0.1		%
$V_{IT+\ (OV)}$	OV accuracy (25℃)			0.1		%
TOL_min	Tolerance Programming minimum			3		%
TOL_max	Tolerance Programming maximum			11		%
THR RES Low	Threshold Programming Resolution Low	V_{IT} ≤ 0.8 V		20		mV / step
THR RES Mid	Threshold Programming Resolution Mid	0.8 V < V_{IT} ≤ 4.0 V		0.5		% / step
THR RES High	Threshold Programming Resolution High	V_{IT} > 4.0 V		20		mV / step
V_{IT}	Accuracy for absolute threshold including tolerance	V_{IT} < 0.8 V	-1.6		1.6	%
V_{IT}	Accuracy for absolute threshold including tolerance	V_{IT} = 0.8 V - 5.55 V	-1		1	%
V_{HYS}	V_{IT} < 0.80V		1.1	1.4	1.7	%
V_{HYS}	V_{IT} ≥ 0.80V		0.40	0.75	1	%
I_{DD}	TPS3704x	V_{DD} ≤ 6.0V		5.5	15	µA
I_{SENSEx}	Input current, SENSEx pin	V_{SENSEx} = 5.5 V		1	2.5	µA
I_{SENSE_ADJ}	Input current, SENSE pin (Bypass internal resistor divider)- Adjustible version	V_{SENSEx} = 5.5 V			350	nA
V_{OL}	Low level output voltage	VDD = 1.7 V, I_{SINK} = 0.4 mA			300	mV
V_{OL}	Low level output voltage	VDD = 2 V, I_{SINK} = 3 mA			300	mV
V_{OL}	Low level output voltage	VDD = 6.0 V, I_{SINK} = 5 mA			300	mV
$I_{(lkg)}$	Open drain output leakage current	V_{DD} = $V_{\overline{RESETx}}$ = 6.0 V			350	nA

(1) $\overline{RESETx}$ pin is driven low when V_{DD} falls below UVLO.
(2) Hysteresis is with respect of the tripoint ($V_{IT-\ (UV)}$, $V_{IT+\ (OV)}$).
(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. Slew rate = 100 mV / µs.

7.6 Timing Requirements

At 1.7 V ≤ V_{DD} ≤ 6.0 V, $\overline{RESETx}$ voltage ($V_{\overline{RESETx}}$) = 10 kΩ to V_{DD}, $\overline{RESETx}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at V_{DD} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_D	Reset release time delay	Fixed delay option t_D < 4 ms, overdrive = 10%	-40	t_D	40	%
t_D	Reset release time delay	Fixed delay option t_D > 5 ms, overdrive = 10%	-30	t_D	30	%
t_{PD}	Propagation detect delay (1)	Fixed time delay t_D > 1 ms, overdrive 10%			10	µs
$t_{GI(VIT-)}$	Glitch Immunity Undervoltage (5% overdrive) (2)			2		µs
$t_{GI(VIT+)}$	Glitch Immunity Overvoltage (5% overdrive) (2)			2		µs
t_R	Ouptut rise (Push-Pull) (2) (3)			25		ns
t_R	Output rise time (Open-Drain) (2) (3)			2.2		µs
t_F	Output fall time (2) (3)			0.2		µs
t_{STRT}	Startup delay (4)			1		ms

(1) t_{PD} measured from threshold trip point ($V_{IT-(UV)}$ or $V_{IT+(OV)}$) to $\overline{RESETx}$ V_{OL} voltage
(2) 5% Overdrive from threshold. Overdrive % = [(V_{SENSEx} - V_{IT}) / V_{IT}]; Where V_{IT} stands for $V_{IT-(UV)}$ or $V_{IT+(OV)}$
(3) Output transitions from V_{OL} to V_{OH} or ($V_{\overline{RESETx}}$) for rise times and V_{OH} or ($V_{\overline{RESETx}}$) to V_{OL} for fall times.
(4) During the power-on sequence, V_{DD} must be at or above $V_{DD(MIN)}$ for at least t_{STRT} + t_D before the output is in the correct state. when VDD is between $V_{DD(MIN)}$ and VPOR the $\overline{RESETx}$ pin will be engaged

7.7 Timing Diagrams

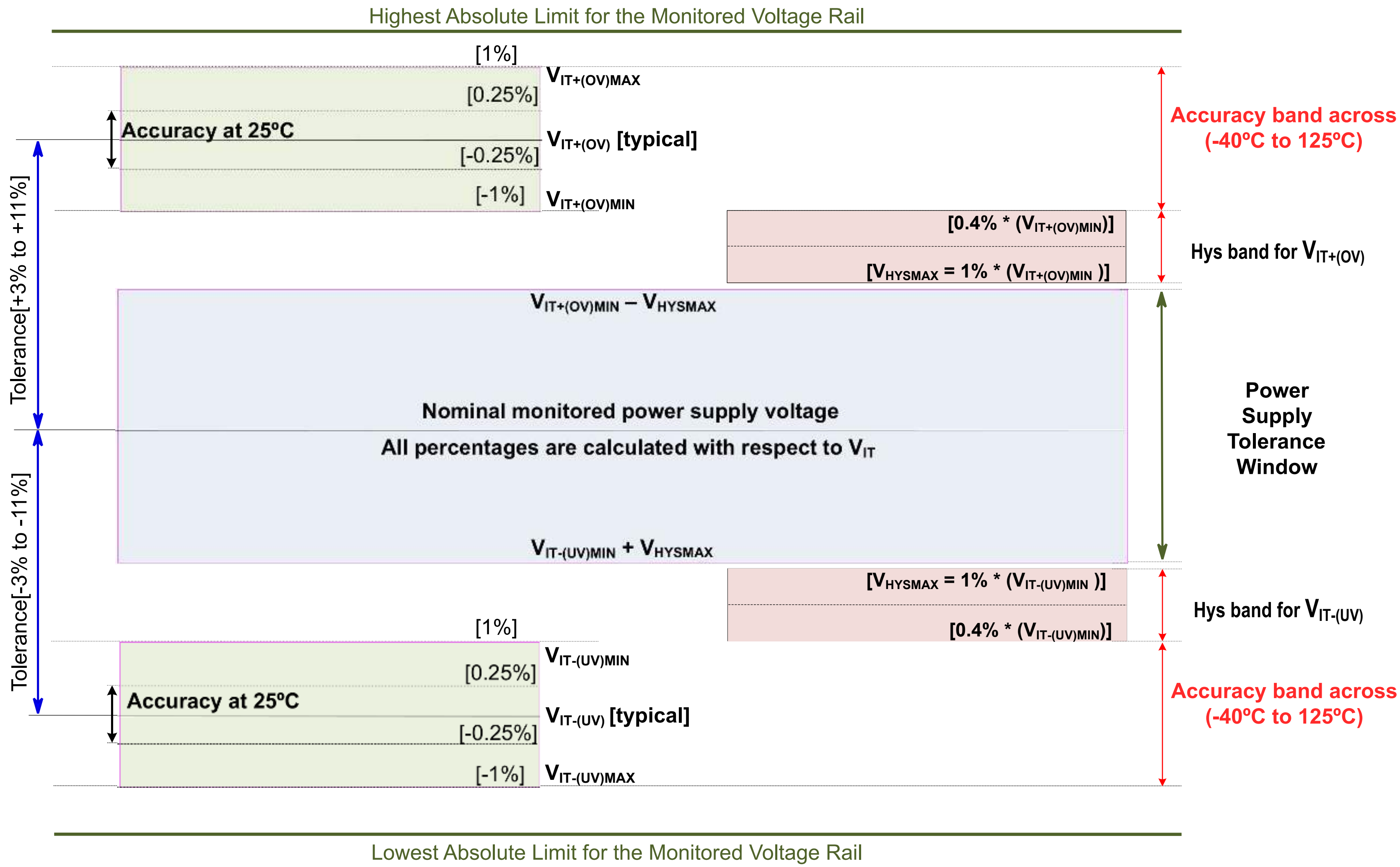
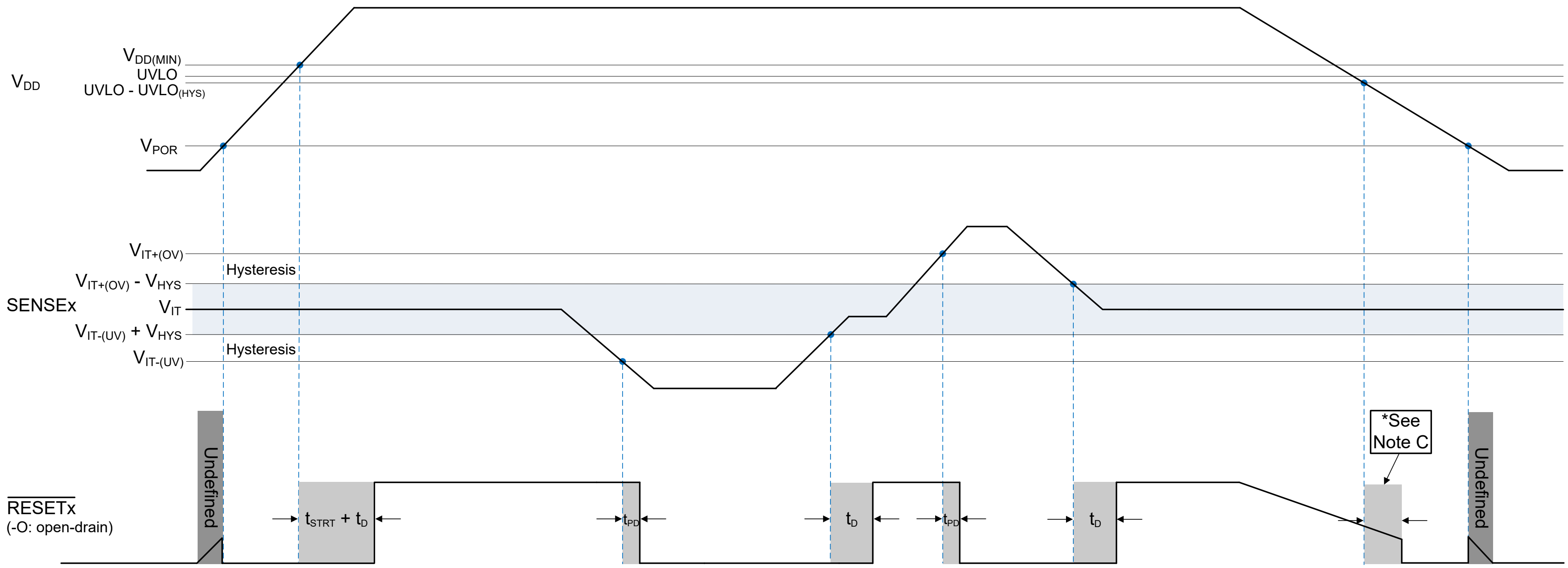


Figure 7-1. Voltage Threshold and Hysteresis Accuracy



A. Open-drain timing diagram assumes the $\overline{\text{RESETx}}$/RESETx pin is connected via an external pullup resistor to VDD.

B. Be advised that Figure 7-2 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{PD}) time.

C. $\overline{\text{RESETx}}$/RESETx is asserted after a time delay, typical value of 100 µs, when VDD goes below the UVLO-UVLO$_{(HYS)}$ threshold.

Figure 7-2. SENSEx Timing Diagram

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.

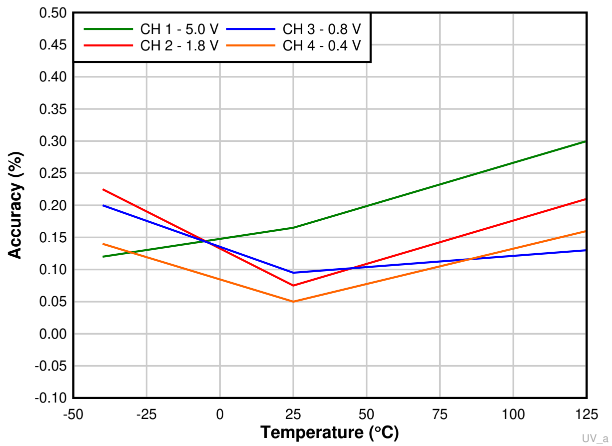


Figure 7-3. Undervoltage Accuracy vs Temperature

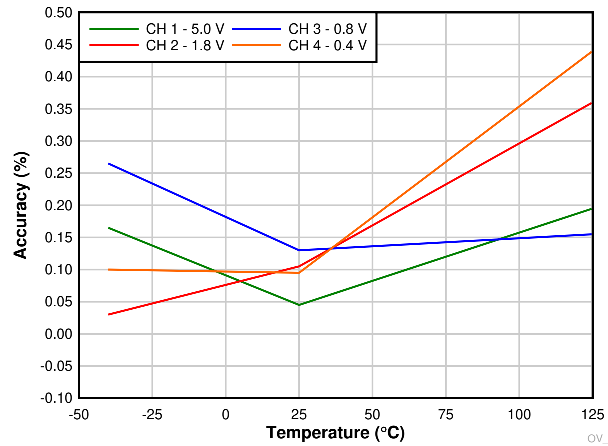


Figure 7-4. Overvoltage Accuracy vs Temperature

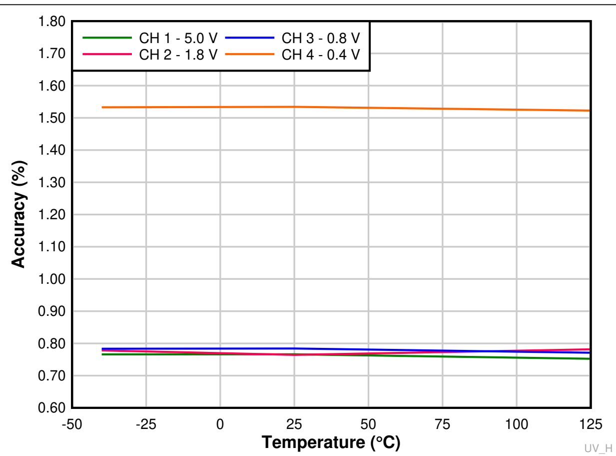


Figure 7-5. Undervoltage Hysteresis Voltage Accuracy vs Temperature

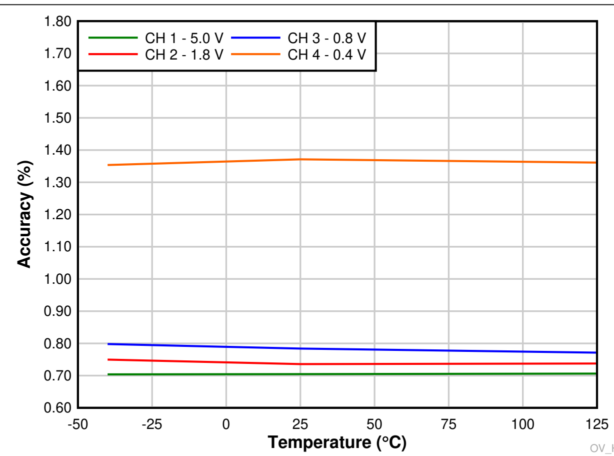
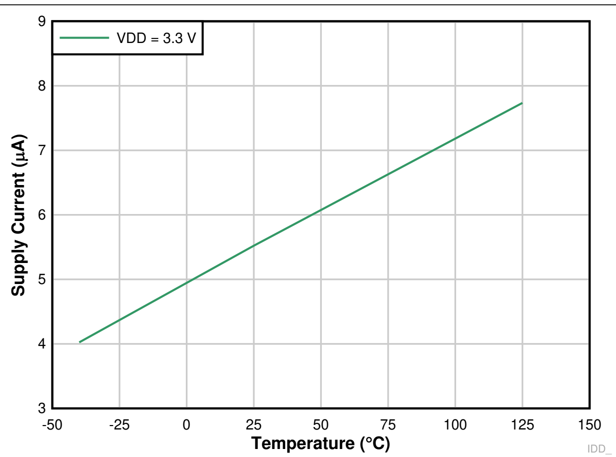
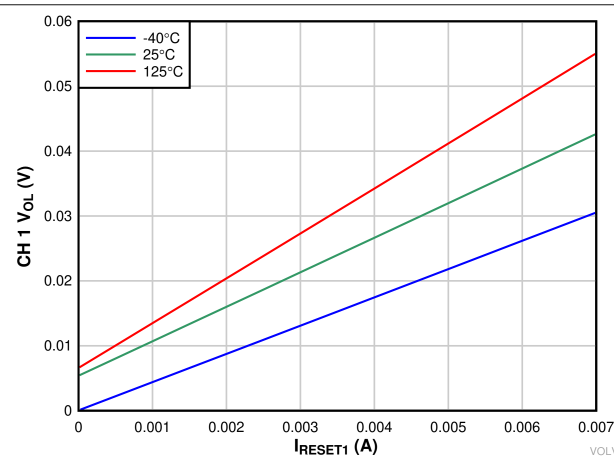


Figure 7-6. Overvoltage Hysteresis Voltage Accuracy vs Temperature



Output ($\overline{\text{RESETx}}$ Pin) = High

Figure 7-7. Supply Current vs Temperature

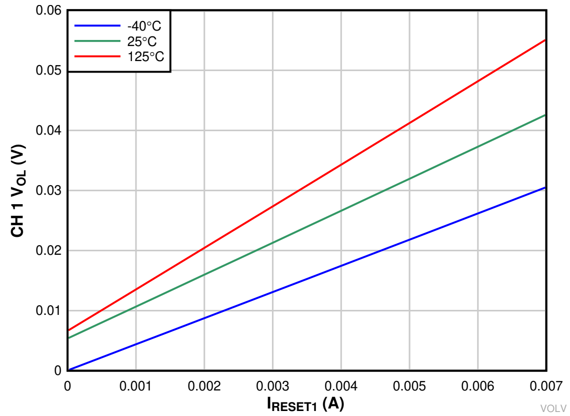


VDD = 1.7 V

Figure 7-8. Low-Level CH 1 Output Voltage vs $\overline{\text{RESET1}}$ Current

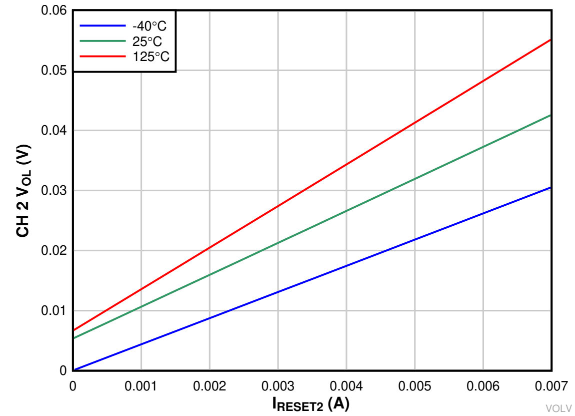
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.



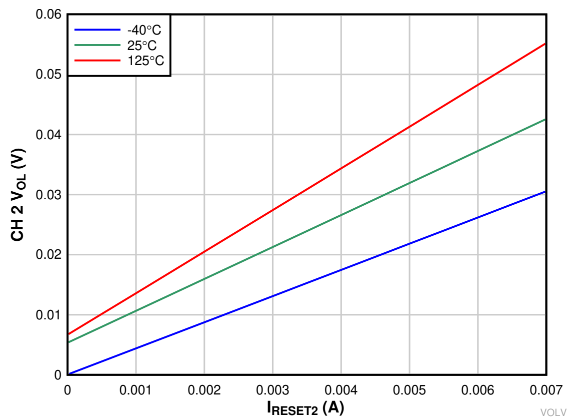
VDD = 5 V

Figure 7-9. Low-Level CH 1 Output Voltage vs $\overline{\text{RESET1}}$ Current



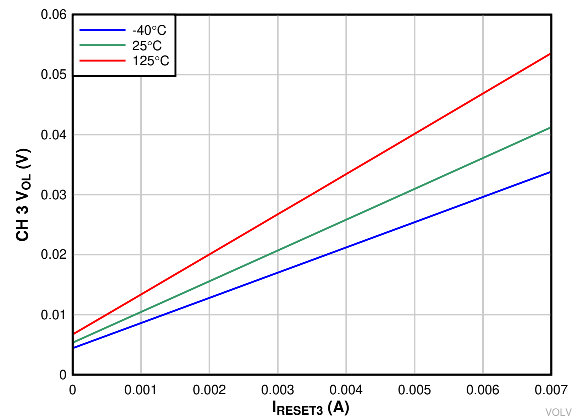
VDD = 1.7 V

Figure 7-10. Low-Level CH 2 Output Voltage vs $\overline{\text{RESET2}}$ Current



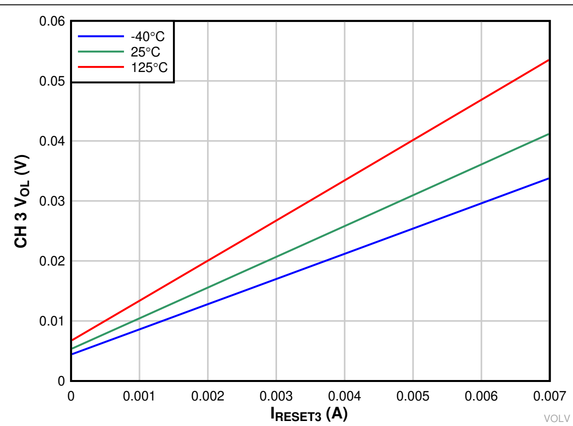
VDD = 5 V

Figure 7-11. Low-Level CH 2 Output Voltage vs $\overline{\text{RESET2}}$ Current



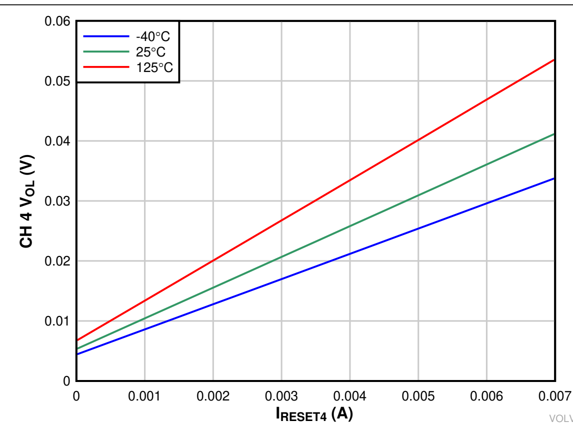
VDD = 1.7 V

Figure 7-12. Low-Level CH 3 Output Voltage vs $\overline{\text{RESET3}}$ Current



VDD = 5 V

Figure 7-13. Low-Level CH 3 Output Voltage vs $\overline{\text{RESET3}}$ Current

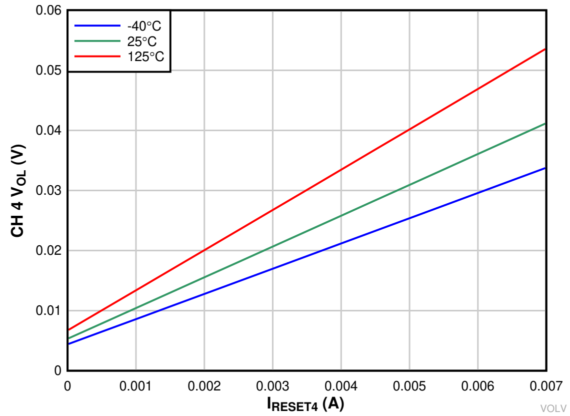


VDD = 1.7 V

Figure 7-14. Low-Level CH 4 Output Voltage vs $\overline{\text{RESET4}}$ Current

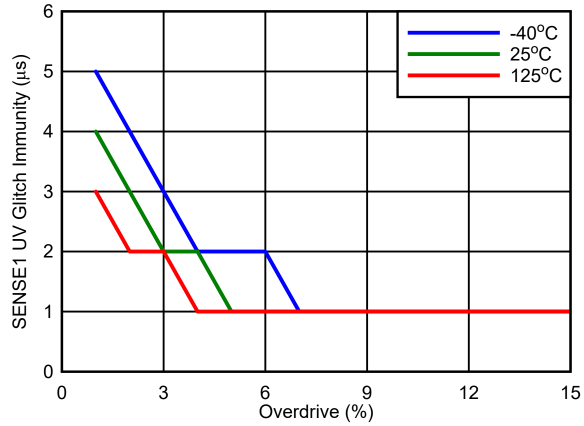
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.



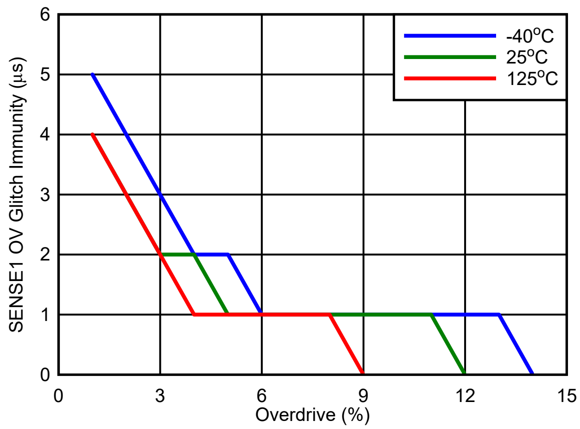
VDD = 5 V

Figure 7-15. Low-Level CH 4 Output Voltage vs $\overline{\text{RESET4}}$ Current



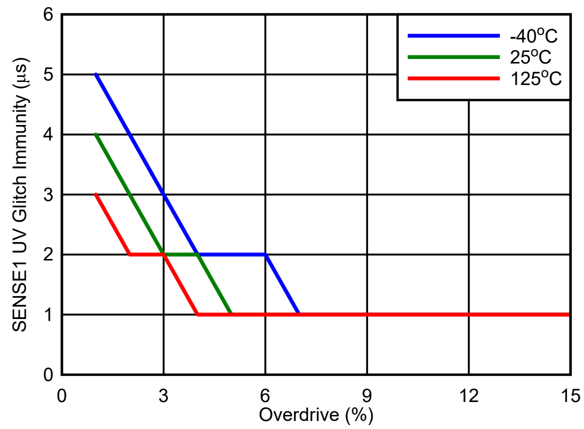
VDD = 1.7 V

Figure 7-16. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive



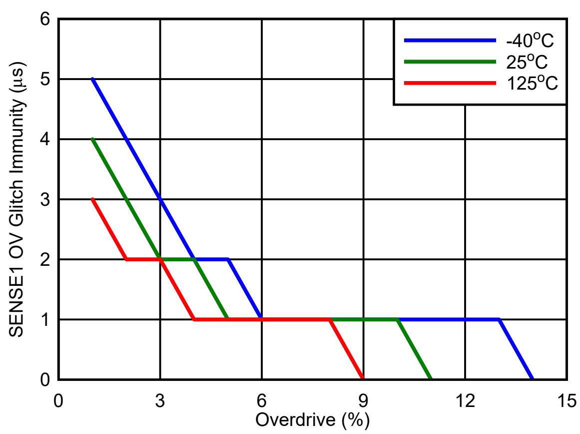
VDD = 1.7 V

Figure 7-17. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive



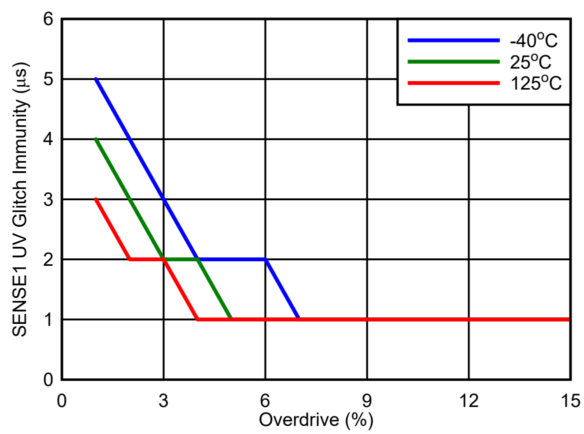
VDD = 3.3 V

Figure 7-18. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive



VDD = 3.3 V

Figure 7-19. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive

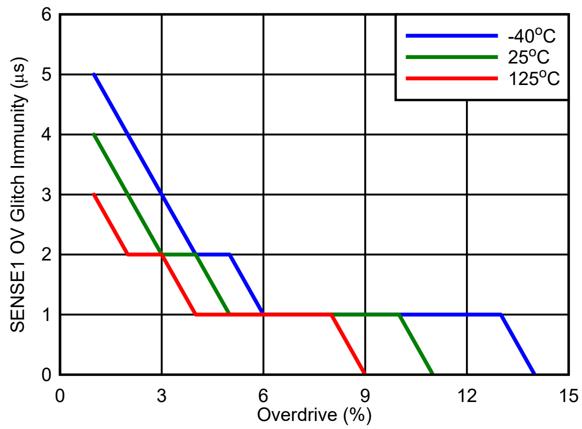


VDD = 5 V

Figure 7-20. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.



VDD = 5 V

Figure 7-21. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive

8 Detailed Description

8.1 Overview

The TPS3704-Q1 (TPS37044-Q1, TPS37043-Q1, TPS37042-Q1, and TPS37041-Q1) is a family of quad, triple, dual, and single precision voltage supervisors where each channel has overvoltage and undervoltage detection capability. The TPS3704-Q1 features a highly accurate window threshold voltage where the upper and lower thresholds can be customized for symmetric or asymmetric tolerances. The reset signal for the TPS3704-Q1 is asserted, with a fault detection time delay (t_{PD} = 10 µs max), when the sense voltage is outside of the overvoltage and undervoltage thresholds.

The TPS3704-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors. The level of integration in the TPS3704-Q1 enables a total small solution size for any application.

The TPS3704-Q1 is able to monitor any voltage rail with high resolution (V_{IT} ≤ 0.8 V: 20-mV steps / V_{IT} > 0.8 V: 0.5% or 20-mV steps whichever is lower). Each channel in the TPS3704x-Q1 can be configured independently as a window, OV or UV supervisor. Also, the VIT threshold voltage for each channel can be asymmetric. For example, a channel that is configured as an overvoltage supervisor can be setup with a +5% tolerance whereas an undervoltage channel supervisor can be programmed with a -4% tolerance. If a window supervisor is configured, the voltage threshold tolerance can either be symmetrical or asymmetrical.

The TPS3704-Q1 device includes fixed reset time delay (t_D) options ranging from 20 µs to 1200 ms and can monitor up to four channels while maintaining an ultra-low I_Q current of 15 µA (maximum).

8.2 Functional Block Diagrams

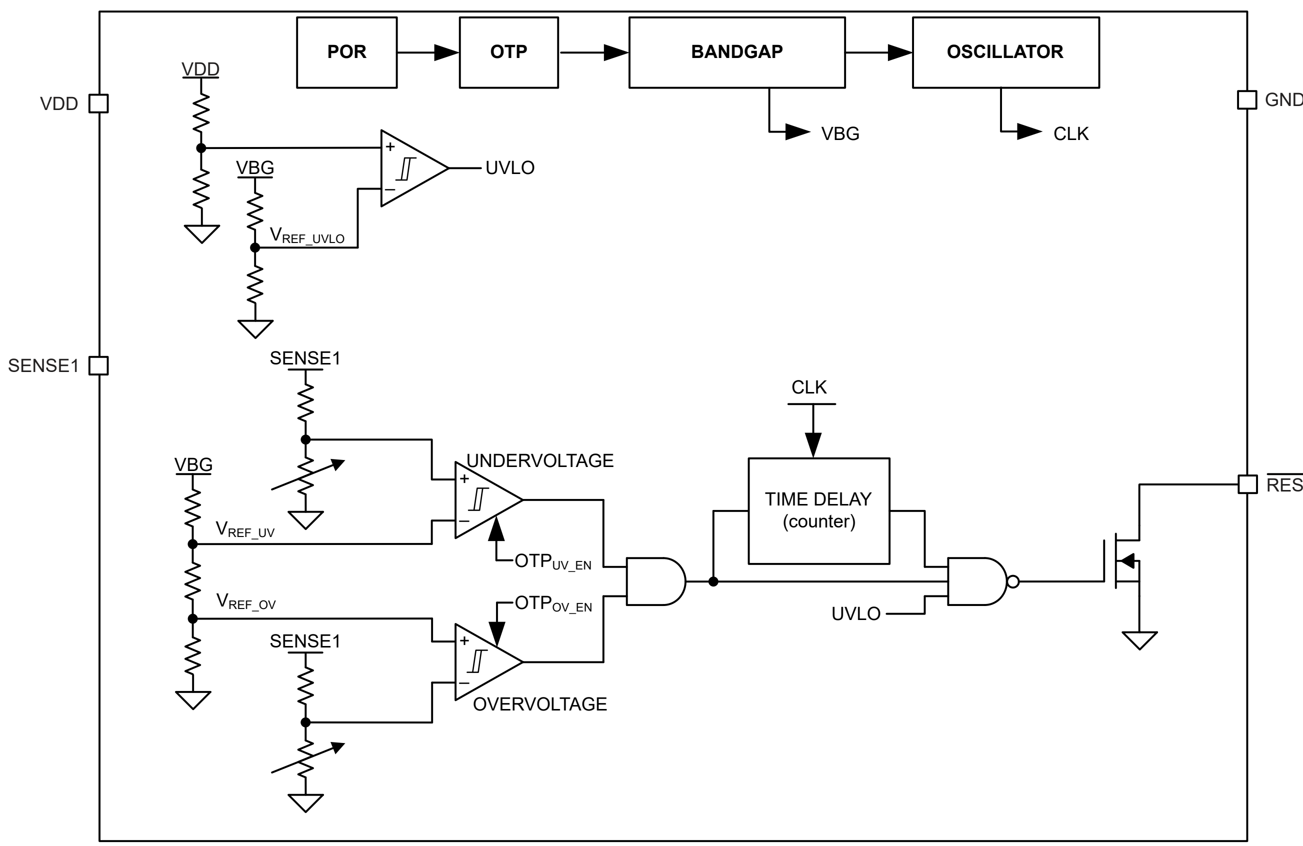


Figure 8-1. TPS37041-Q1 Single-Channel Functional Block Diagram

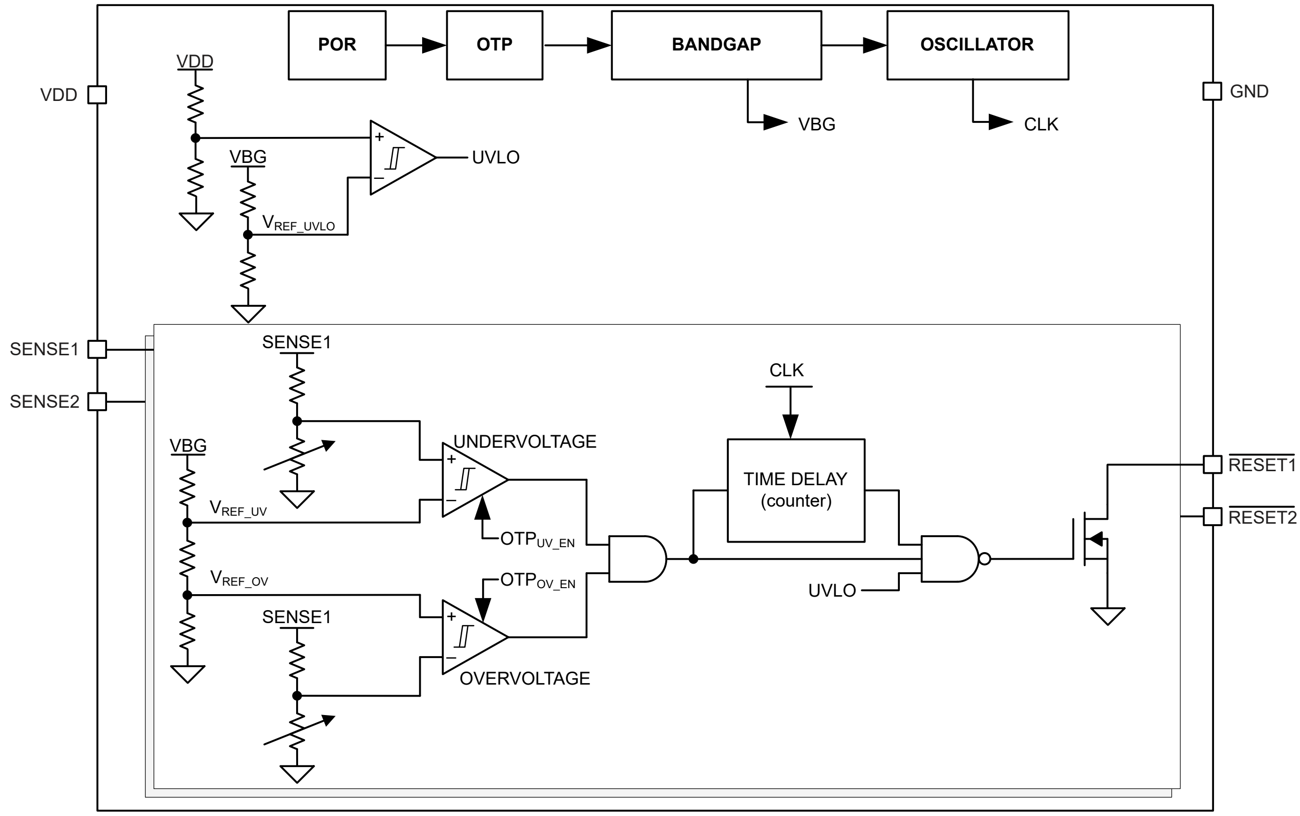


Figure 8-2. TPS37042-Q1 Dual-Channel Functional Block Diagram

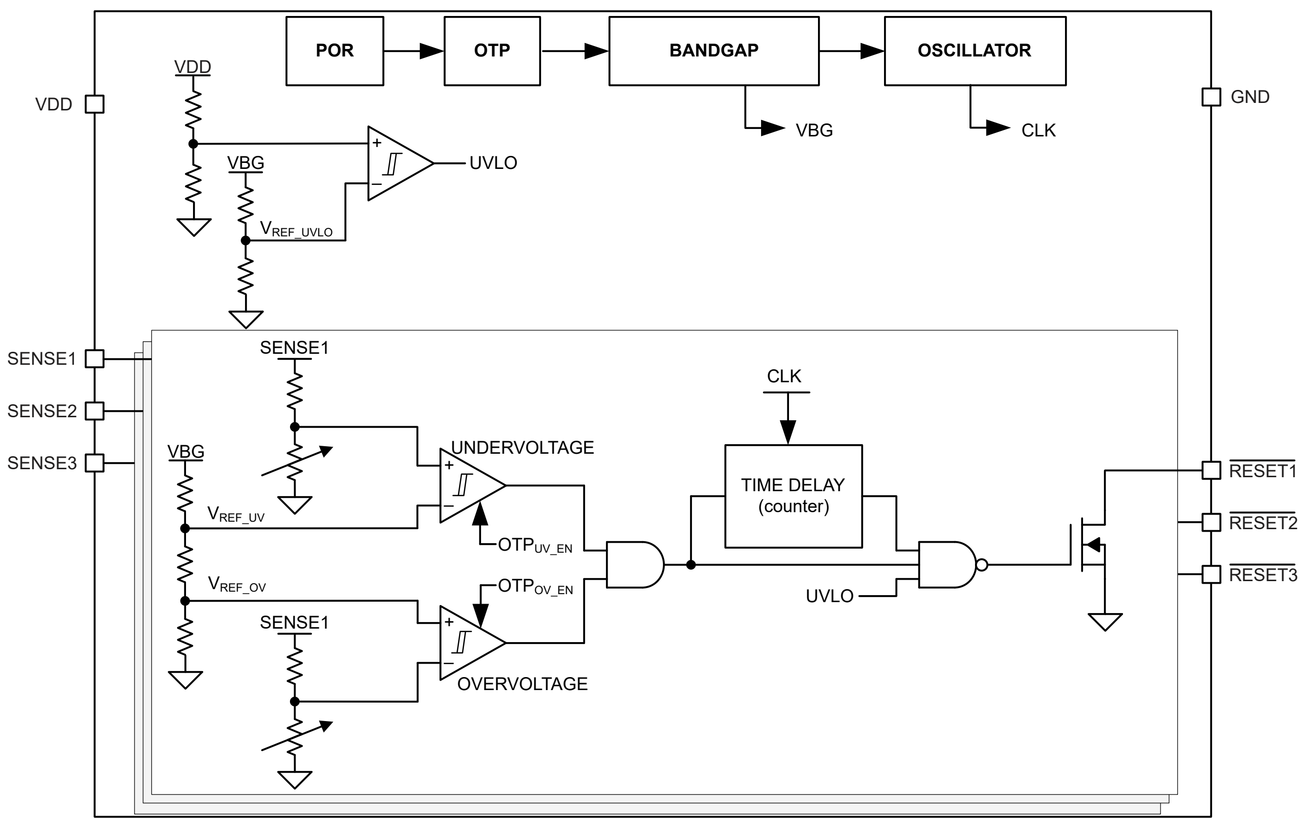


Figure 8-3. TPS37043-Q1 Triple-Channel Functional Block Diagram

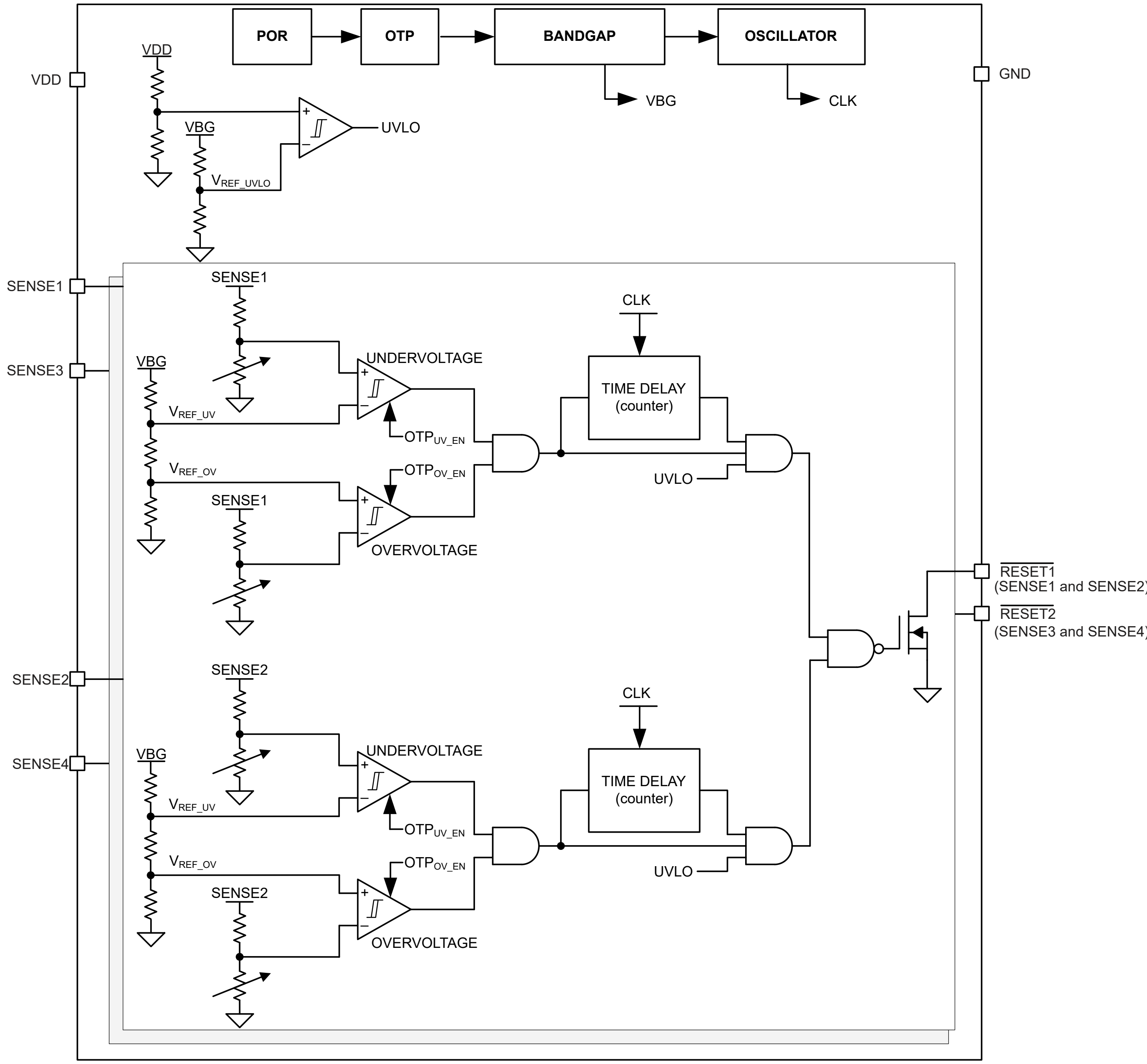


Figure 8-4. TPS37044-Q1 Quadruple-Channel Functional Block Diagram

*For available voltages, window tolerance, time delays, and UV/OV threshold options, see Table 12-2.

8.3 Feature Description

8.3.1 VDD

The TPS3704-Q1 is designed to operate from an input voltage supply range between 1.7 V to 6 V. The SENSEx pins are monitored by the internal comparator. VDD also functions as the supply for the internal band gap, internal regulator, state machine, buffers, and other control blocks. The reset signal is at a known state when VDD > V_{POR}. The undervoltage lockout forces the reset output to be asserted when VDD falls below the minimum VDD voltage.

The VDD capacitor is not required for this device; however, if the input supply is noisy, then good design practice is to place a 0.1-µF to 1-µF bypass capacitor between the VDD pin and the GND pin to ensure enough charge is available for the device to power up correctly. VDD must be at or above $V_{DD(MIN)}$ for start-up delay (t_{STRT} + t_D) to begin and for the device to be fully functional.

8.3.2 SENSEx Input

The SENSEx input can vary from 0 V to 6 V, regardless of the device supply voltage used. The SENSEx pins are used to monitor critical voltage rails or push-button inputs. If the voltage on this pin drops below $V_{IT-(UV)}$ or goes above $V_{IT+(OV)}$, then $\overline{\text{RESETx}}$/RESETx is asserted. When the voltage on the SENSEx pin rises above the positive threshold voltage $V_{IT-(UV)}$ + V_{HYS} or goes below the negative threshold voltage $V_{IT+(OV)}$ - V_{HYS},

$\overline{\text{RESETx}}$/RESETx deasserts after the set $\overline{\text{RESETx}}$/RESETx delay time. The internal comparators have built-in hysteresis to ensure well-defined $\overline{\text{RESETx}}$/RESETx assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3704-Q1 combines comparators with a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. The TPS3704-Q1 is relatively immune to short transients on the SENSEx pin. Although not required in most cases, for noisy applications, good analog design practice is to place a 10-nF to 100-nF bypass capacitor at the SENSEx inputs to reduce sensitivity to transient voltages on the monitored signals.

8.3.2.1 Immunity to SENSEx Pins Voltage Transients

The TPS3704-Q1 is immune to short voltage transient spikes on the input SENSEx pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much V_{SENSEx} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the $\overline{\text{RESETx}}$/RESETx outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1:

$$\text{Overdrive \%} = | (V_{SENSEx} - (V_{IT-(UV)} \text{ or } V_{IT+(OV)})) / V_{IT} \text{ (Nominal)} \times 100\% | \quad (1)$$

where:

- V_{SENSEx} is the voltage at the SENSEx pin
- V_{IT} (Nominal) is the nominal threshold voltage
- $V_{IT-(UV)}$ and $V_{IT+(OV)}$ represent the actual undervoltage or overvoltage tripping voltage

8.3.2.1.1 SENSEx Hysteresis

Overvoltage and undervoltage comparators include built-in hysteresis that provides noise immunity and ensures stable operation. For example, if the voltage on the SENSEx pin falls below $V_{IT-(UV)}$ or above $V_{IT+(OV)}$, then $\overline{\text{RESETx}}$/RESETx is asserted. When the voltage on the SENSEx pin is between the positive and negative threshold voltages, $\overline{\text{RESETx}}$/RESETx deasserts after the set $\overline{\text{RESETx}}$/RESETx delay time. Figure 8-5 shows the relation between $V_{IT-(UV)}$,$V_{IT+(OV)}$ and the hysteresis voltage (V_{HYS}).

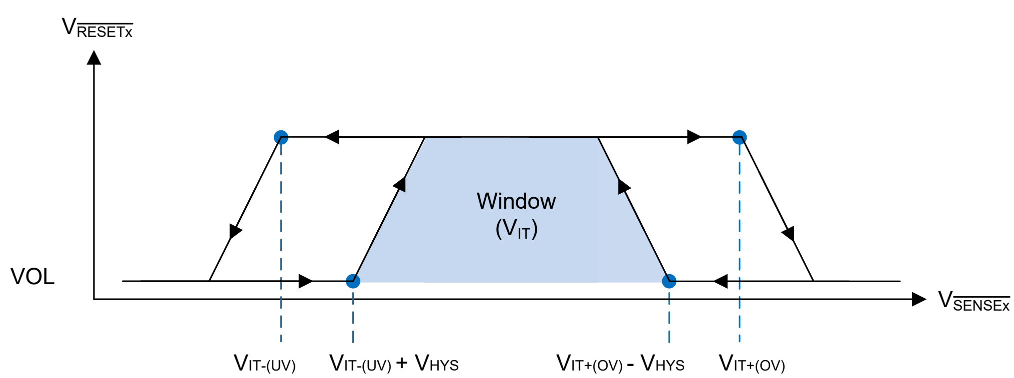


Figure 8-5. SENSEx Pin Hysteresis

8.3.3 $\overline{\text{RESETx}}$/RESETx

In a typical TPS3704-Q1 application, the $\overline{\text{RESETx}}$/RESETx output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC/DC converter or low-dropout regulator (LDO)].

The TPS3704-Q1 has open-drain active low outputs that require an external pullup resistor to hold these lines high to the required voltage logic. Connect the external pullup resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the external pullup resistor values. The external pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in Section 7.5. The open-drain output can be connected as a wired-OR logic with other $\overline{\text{RESETx}}$/RESETx open-drain pins.

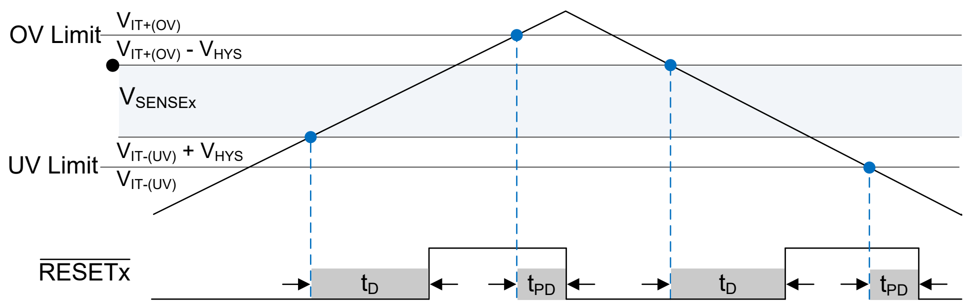


Figure 8-6. $\overline{\text{RESETx}}$ Output

8.4 Device Functional Modes

Table 8-1. Functional Mode Truth Table

DESCRIPTION	CONDITION	VDD PIN	OUTPUT $\overline{\text{RESETx}}$ / (RESETx) PIN
Normal operation	$V_{IT–(UV)}$ < SENSEx < $V_{IT+(OV)}$	$V_{DD} > V_{DD(MIN)}$	High / (Low)
Normal operation (UV only)	SENSEx > $V_{IT-(UV)}$	$V_{DD} > V_{DD(MIN)}$	High / (Low)
Overvoltage detection	SENSEx > $V_{IT+(OV)}$	$V_{DD} > V_{DD(MIN)}$	Low / (High)
Undervoltage detection	SENSEx < $V_{IT-(UV)}$	$V_{DD} > V_{DD(MIN)}$	Low / (High)
UVLO engaged	$V_{IT–(UV)}$ < SENSEx < $V_{IT+(OV)}$	$V_{POR} < V_{DD}$ < UVLO	Low / (High)

8.4.1 Normal Operation ($V_{DD} > V_{DD(MIN)}$)

When the voltage on V_{DD} is greater than $V_{DD(MIN)}$ for approximately (t_{STRT} + t_D), the $\overline{\text{RESETx}}$/RESETx output state corresponds to the SENSEx pin voltage with respect to the threshold limits. When SENSEx voltage is outside of threshold limits the $\overline{\text{RESETx}}$/RESETx voltage is asserted.

8.4.2 Undervoltage Lockout ($V_{POR} < V_{DD}$ < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage but greater than the power-on-reset voltage (V_{POR}), the $\overline{\text{RESETx}}$/RESETx pin is asserted, regardless of the voltage on the SENSEx pin.

8.4.3 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) to internally pull the asserted output to GND, the $\overline{\text{RESETx}}$/RESETx signal is undefined and is not to be relied upon for proper device function.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Voltage Threshold Accuracy

Voltage monitoring requirements vary depending on the voltage supply tolerance of the device being powered. Because of the high precision of the TPS3704-Q1 (±1% max), the device allows for wider supply voltage margins and threshold headroom for tight tolerance applications.

For example, take a DC/DC regulator providing power to a core voltage rail of a microcontroller (MCU). The MCU has a tolerance of ±5% of the nominal output voltage of the DC/DC. The user sets an ideal voltage threshold of ±4%, which allows for ±1% of threshold accuracy. Because the TPS3704-Q1 threshold accuracy is ±1%, the user has more supply voltage margin, which can allow for a relaxed power supply design. This design gives flexibility to the DC/DC to use a smaller output capacitor or inductor because of a larger voltage window for voltage ripple and transients. There is also headroom between the minimum system voltage and voltage tolerance of the MCU to ensure that the voltage supply is never in the region of potential failure of malfunction without the TPS3704-Q1 asserting a reset signal.

Figure 9-1 shows the supply undervoltage margin and accuracy of the TPS3704-Q1 for the example explained in this section. Using a low accuracy supervisor cuts into the available budget for the power-supply ripple and transient response. This gives less flexibility to the user and a more stringent DC/DC converter design.

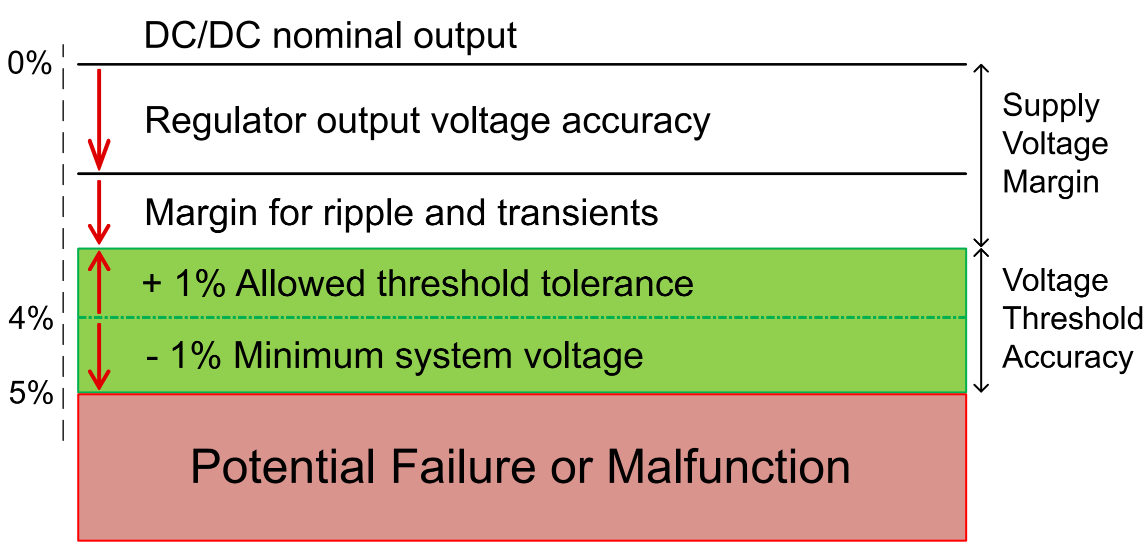


Figure 9-1. TPS3704-Q1 Voltage Threshold Accuracy

9.1.2 Adjustable Voltage Thresholds

The TPS3704-Q1 maximum accuracy (1%) allows for adjustable voltage thresholds using external resistors without adding major inaccuracies to the device. In case the desired monitored voltage is not available, external resistor dividers can be used to set the desired voltage thresholds. Figure 9-2 shows an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using a voltage threshold device variant because of the bypass mode of the internal resistor ladder.

For example, consider a 2.0-V rail being monitored (V_{MON}) using the TPS37042BJOFDDFRQ1 variant. Using Equation 2, R1 = 15 kΩ given that R2 = 10 kΩ, V_{MON} = 2 V, and V_{SENSE1} = 0.8 V. This device is typically meant to monitor a
0.8-V rail with ±4% voltage thresholds. This means that the device undervoltage threshold ($V_{IT-(UV)}$) and overvoltage threshold ($V_{IT+(OV)}$) is 0.768 V and 0.832 V, respectively. Using Equation 2, V_{MON} = 1.92 V when V_{SENSE1} = $V_{IT-(UV)}$. This can be denoted as V_{MON-}, the monitored undervoltage threshold where the device asserts a reset signal. Using Equation 2 again, the monitored overvoltage threshold (V_{MON+}) = 2.08 V when V_{SENSE1} = $V_{IT+(OV)}$. If a wider tolerance or UV only threshold is desired, use a device variant listed in
Table 12-2 to determine which device part number matches which application.

$$V_{SENSE1} = V_{MON} \times (R_2 / (R_1 + R_2)) \tag{2}$$

There are inaccuracies that must be taken into consideration when adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE1 pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for design specifications. The internal sense resistance R_{SENSE1} can be calculated by the sense voltage V_{SENSE1} divided by the sense current I_{SENSE1} as shown in Equation 4. V_{SENSE1} can be calculated using
Equation 2 depending on the resistor divider and monitored voltage. I_{SENSE1} can be calculated using Equation 3.

$$I_{SENSE1} = [(V_{MON} - V_{SENSE1}) / R_1] - (V_{SENSE1} / R_2) \tag{3}$$

$$R_{SENSE1} = V_{SENSE1} / I_{SENSE1} \tag{4}$$

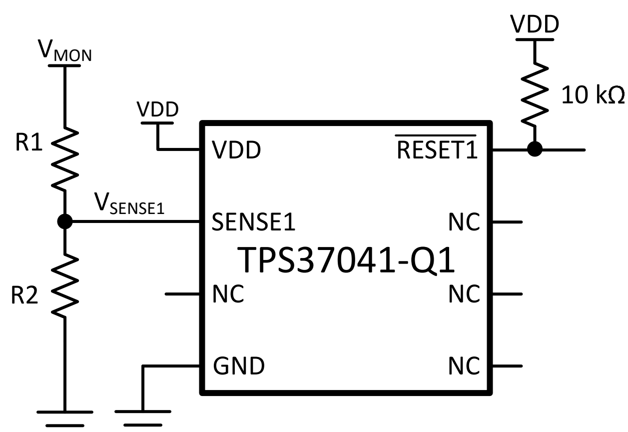


Figure 9-2. Adjustable Voltage Threshold With External Resistor Dividers

9.2 Typical Applications

9.2.1 Design 1: Multi-Rail Window Monitoring for Microcontroller Power Rails

Figure 9-3 show a typical application for the TPS37042-Q1. The TPS37042-Q1 is used to monitor two PMIC (Power Management IC) voltage rails that power the core and I/O voltage of the microcontroller that requires accurate reset delay and voltage supervision. The PMIC leverages the TPS37042-Q1 to monitor the core voltage rail of a MCU similar to the circuit below.

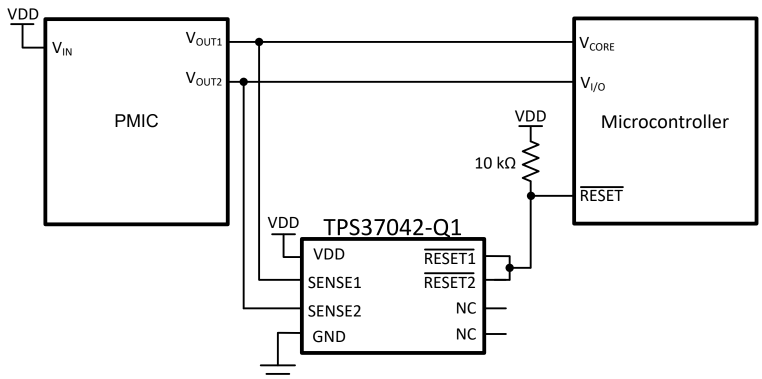


Figure 9-3. TPS37042-Q1 Dual-Channel Monitoring Two Microcontroller Power Rails

9.2.1.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-$V_{I/O}$ nominal, with alerts if outside of ±8% of 3.3 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 3.533 V (7.06%) Worst case $V_{IT–(UV)}$ = 3.071 V (–6.94%)
	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.2484 V (4.03%) Worst case $V_{IT–(UV)}$ = 1.1524 V (–3.97%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum system supervision current consumption	25 µA	5.5 µA (20 µA max)

9.2.1.2 Detailed Design Procedure

Determine which version of the TPS3704-Q1 best suits the monitored rail (V_{MON}) and window tolerances found on Table 12-2. The TPS3704-Q1 allows overvoltage and undervoltage monitoring for precise voltage supervision of common rails between 0.4 V and 5.5 V. This application calls for very tight monitoring of the rail with only ±5% of variation allowed on the 1.2-V_{CORE} rail. To ensure this requirement is met, the TPS37042-Q1 was chosen for its ±3% thresholds. The 3.3-$V_{I/O}$ is more flexible and can operate up to 8% variance. Because the TPS3704-Q1 comes in various tolerance options, the ±6% thresholds can be chosen for this voltage rail. To calculate the worst case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$, the accuracy must also be taken into account. The worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$ can be calculated shown in Equation 5 and Equation 6 respectively:

$$V_{IT+(OV\text{-}Worst\ Case)} = V_{MON} \times (1 + \%Threshold) \times (1 + \%Accuracy) = 1.2 \times (1.03) \times (1.01) = 1.2484\ V \quad (5)$$

$$V_{IT-(UV\text{-}Worst\ Case)} = V_{MON} \times (1 - \%Threshold) \times (1 - \%Accuracy) = 1.2 \times (0.97) \times (0.99) = 1.1524V \quad (6)$$

Hysteresis must also be taken into account when determining the OV and UV thresholds such that the release point after the fault is higher than the power-supply tolerance limits. See Figure 7-1 for more details.

When the outputs switch to a high impedance state, the rise time of the $\overline{RESETx}$/RESETx pin depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 10-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

9.2.2 Design 2: Manual Self-Test Option for Enhanced Functional Safety Use Cases

Figure 9-4 displays a self-test scheme where a manual self-test function can be implemented. Any SENSEx pin can be reserved and used to trigger a fault to be observed at the output, thus pre-checking the TPS3704-Q1 for fault detection. Because the TPS3704-Q1 is functional safety compliant, it helps elevate applications like the automotive ADAS camera achieve ISO 26262 requirements and automotive safety integrity levels. This example uses a TPS37044F-Q1, configured for separate undervoltage and overvoltage (UV/OV) outputs where the SENSE4 thresholds are set at 5.5 V for OV and 2 V for UV.

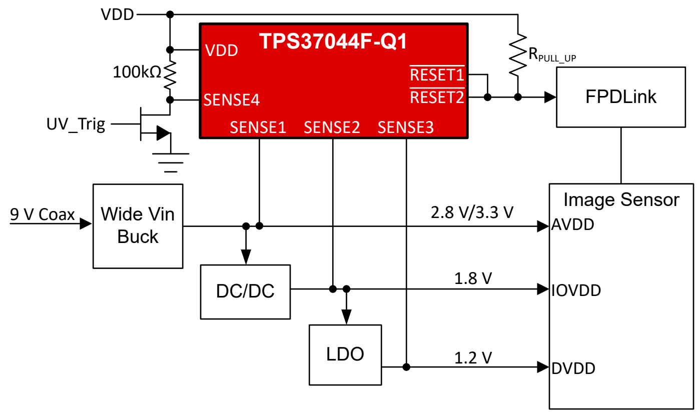


Figure 9-4. TPS37044F-Q1 Quad-Channel Monitoring With Manual Self-Test Option for Functional Safety

9.2.2.1 Design Requirements

Table 9-2. Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-V AVDD nominal, with alerts if outside of ±4% of 3.3 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 3.432 V (+4%) Worst case $V_{IT-(UV)}$ = 3.168 V (–4%)
	1.8-V IOVDD nominal, with alerts if outside of ±4% of 1.8 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.872 V (+4%) Worst case $V_{IT-(UV)}$ = 1.728 V (–4%)
	1.2-V DVDD nominal, with alerts if outside of ±4% of 1.2 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.248 V (+4%) Worst case $V_{IT-(UV)}$ = 1.152 V (–4%)
SENSE4 (Self-test Option)	100-kΩ pullup resistor to VDD with NFET pulldown transistor to GND	UV_Trig = High - causing SENSE4 pin going low UV_Trig = Low - in normal operation
Output logic voltage	5-V CMOS	5-V CMOS
Max system IDD current	25 µA	5.5 µA (20 µA maximum)

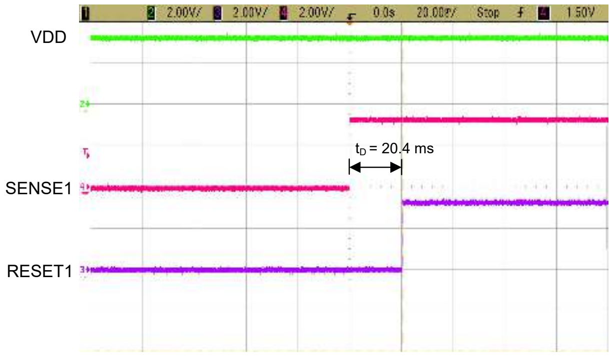
9.2.2.2 Detailed Design Procedure

Figure 9-4 shows a self-test scheme where a manual self-test function can be implemented. SENSE4 has an overvoltage (OV) threshold that is set at 5.5 V and the undervoltage (UV) threshold set at 2 V. SENSE4 can be connected via a 100-kΩ resistor to VDD. The self-test setup gives the added benefit of a built-in overvoltage detector for the rail powering the TPS37044F-Q1. From a functional safety perspective, a voltage supervisor cannot be considered reliable if the supervisor is operating outside its recommended operated limits.

To trigger a manual self-test, pull UV_Trig high to cause SENSE4 to be logic low, therefore triggering an undervoltage (UV) fault. The UV fault appears at RESET2 as an asserted low signal. By tying both reset outputs to an NMI or interrupt input of the processor, this self-test option scheme serves as a purpose to ensure that RESET2, of the TPS37044F-Q1 is operating properly. For more information on functional safety, see the Functional Safety Manual.

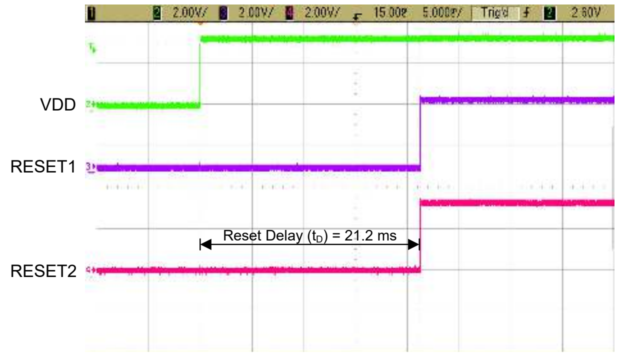
9.2.3 Application Curves

These application curves were taken with the TPS37044A7OHDDFRQ1 device on the TPS3704Q1EVM. Please see the TPS3704Q1EVM User Guide for more information.



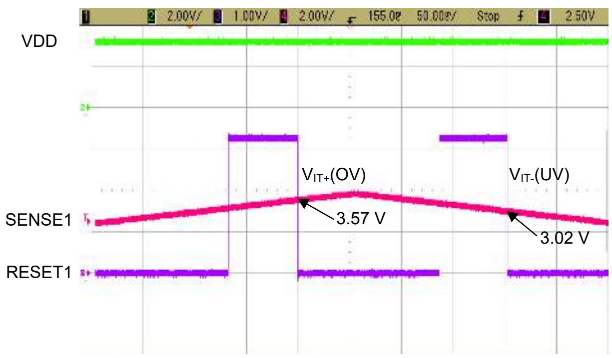
V_{SENSE1} start up 0 V to 3.3 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-5. TPS37044-Q1 SENSE1 Start-Up Function



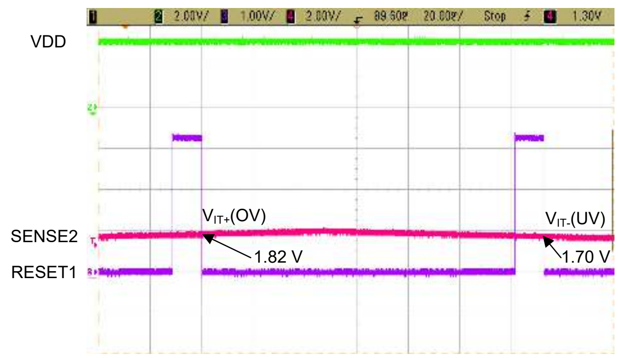
V_{DD} start up 0 V to 3.3 V, V_{SENSE1} = 3.3 V, V_{SENSE2} = 1.8 V, V_{SENSE3_4} = 1.15 V, $V_{\overline{RESET1\_2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-6. TPS37044-Q1 VDD Start-Up Function



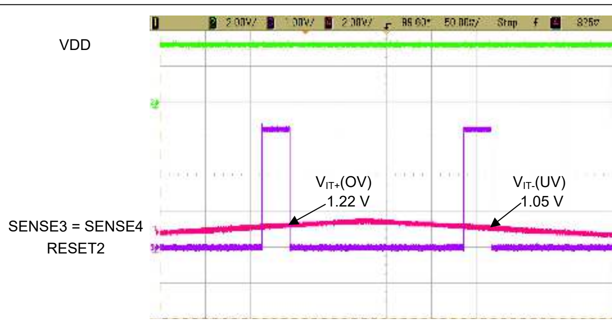
V_{SENSE1} ramp 0 V to 3.75 V, OV/UV Threshold = 3.3 V (±8%), V_{SENSE2} = 1.8 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-7. TPS37044-Q1 Overvoltage and Undervoltage Function



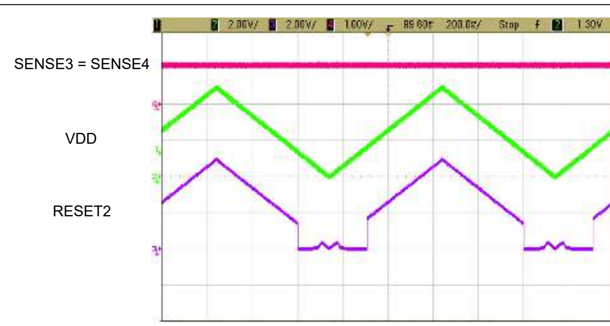
V_{SENSE2} ramp 0 V to 2 V, OV/UV Threshold = 1.8 V (+4%, -3.5%), V_{SENSE1} = 3.3 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-8. TPS37044-Q1 Overvoltage and Undervoltage Function



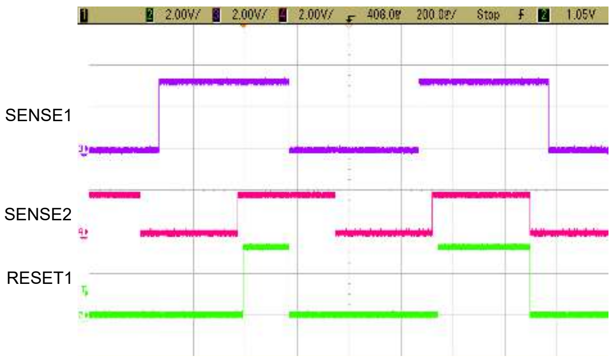
V_{SENSE3_4} ramp 0 V to 1.5 V, OV/UV Threshold = 1.15 V (+7.5%, -5.5%), V_{DD} = 3.3 V, $V_{\overline{RESET2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-9. TPS37044-Q1 Overvoltage and Undervoltage Function



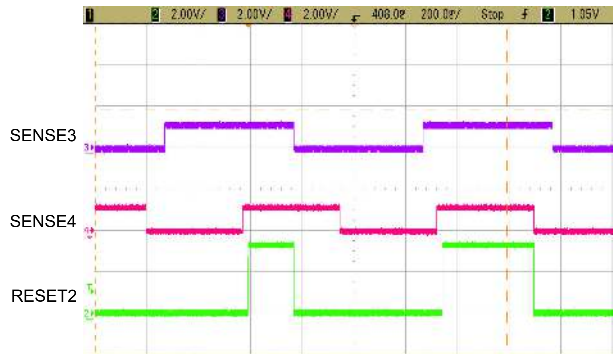
V_{DD} ramp 0 V to 5 V, V_{SENSE3_4} = 1.2 V, $V_{\overline{RESET2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-10. TPS37044-Q1 VDD Ramp-Up Function



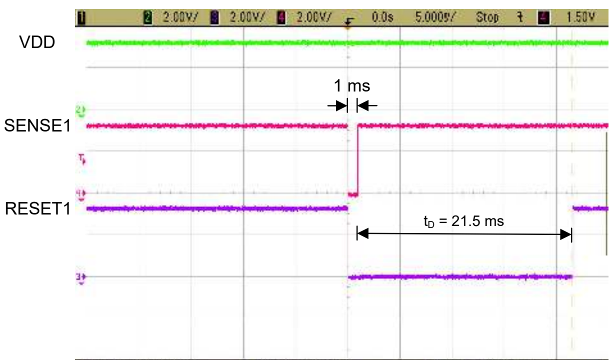
V_{SENSE1} toggling 0 V to 3.3 V [OV/UV Threshold = 3.3 V (±8%)], V_{SENSE2} toggling from 0 V to 1.8 V [OV/UV Threshold = 1.8 V (+4%, -3.5%)], V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-11. TPS37044-Q1 SENSE 1 and SENSE 2 Toggling



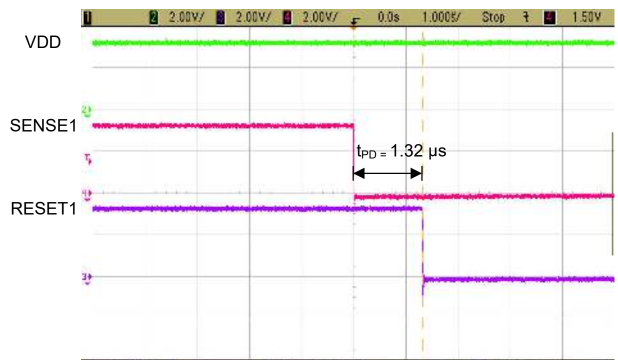
V_{SENSE3} toggling 0 V to 1.15 V [OV/UV Threshold = 1.15 V (+7.5%, -5.5%)], V_{SENSE4} toggling from 0 V to 1.15 V [OV/UV Threshold = 1.15 V (+7.5%, -5.5%)], V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-12. TPS37044-Q1 SENSE 3 and SENSE 4 Toggling



V_{SENSE1} = 3.3 V, V_{SENSE1} = 0 V via push-button for 1 ms, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

Figure 9-13. TPS37044-Q1 SENSE1 Push-Button Monitoring Function With Reset Time Delay



V_{SENSE1} toggling from 3.3 V to 0 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ toggling from 3.3 V to 0 V, TPS37044A7OHDDFRQ1

Figure 9-14. TPS37044-Q1 SENSE1 Propagation Delay Function

10 Power Supply Recommendations

10.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 1.7 V to 5.5 V. This devise has a 6-V absolute maximum rating on the VDD pin. Good analog practice is to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transients that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

11 Layout

11.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long voltage traces to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If SENSEx capacitors (C_{SENSEx}) are used, place capacitors as close as possible to the SENSEx pins to further improve noise immunity on the SENSEx pins. Placing a 10-nF to 100-nF capacitor(s) between the SENSEx pin(s) and GND can reduce the sensitivity to transient voltages on the monitored signal.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

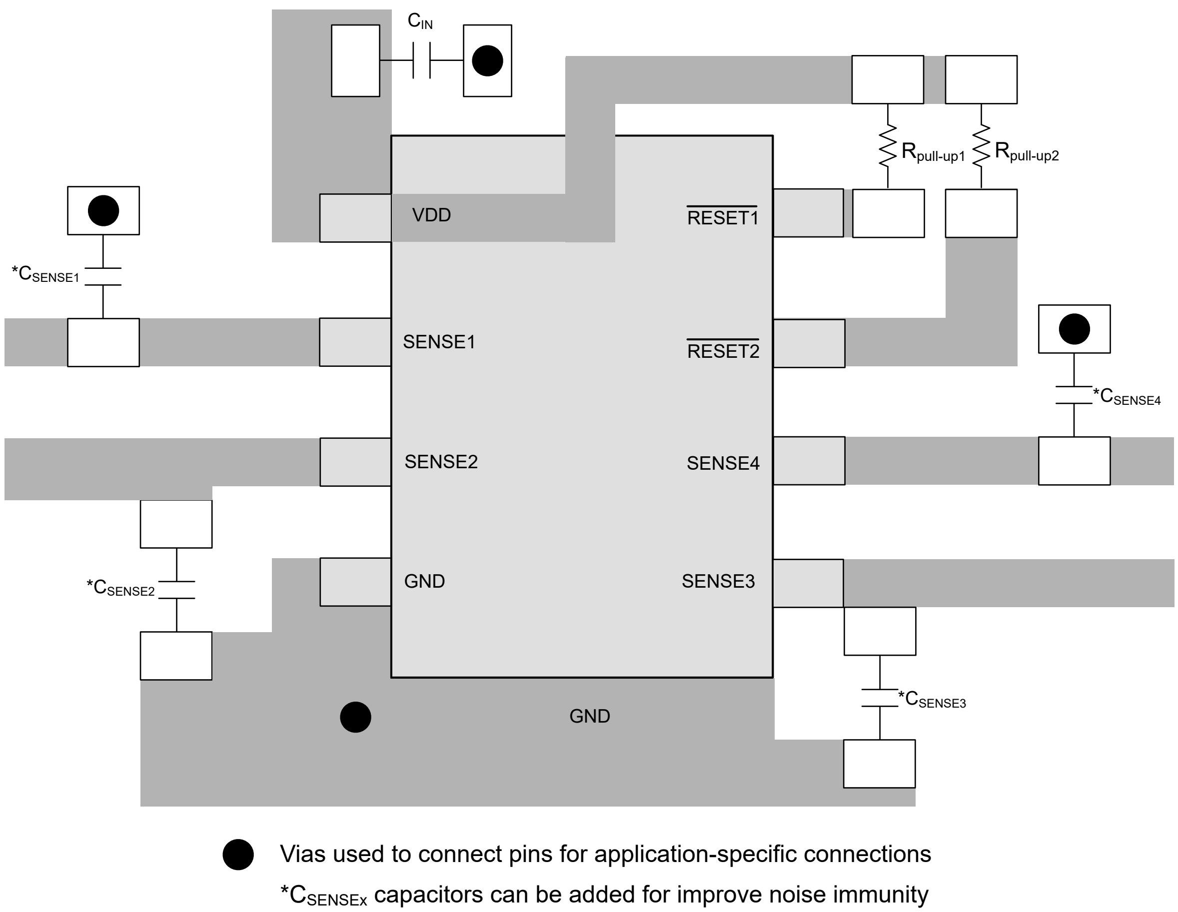


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

Figure 5-1 in Section 5 and Table 12-1 describe how to decode the function of the device based on its part number listed in Table 12-2.

Table 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic part number	TPS3704x-Q1	TPS3704x-Q1
Channel options	1	One-channel option
	2	Dual-channel option
	3	Triple-channel option
	4	Quad-channel option
Detection options	Ax, Bx, Cx,...	See Table 12-2
Variant code (output topology)	O	Open-drain, active-low
	L	Push-pull, active-low
	H	Push-pull, active-high
Reset time delay option	A	20-µs reset time delay
	B	1-ms reset time delay
	C	2-ms reset time delay
	D	3-ms reset time delay
	E	5-ms reset time delay
	F	10-ms reset time delay
	G	15-ms reset time delay
	H	20-ms reset time delay
	I	25-ms reset time delay
	J	35-ms reset time delay
	K	40-ms reset time delay
	L	50-ms reset time delay
	M	70-ms reset time delay
	N	100-ms reset time delay
	O	140-ms reset time delay
	P	150-ms reset time delay
	R	200-ms reset time delay
	S	280-ms reset time delay
	T	400-ms reset time delay
	U	560-ms reset time delay
	V	800-ms reset time delay
	W	1120-ms reset time delay
	X	1200-ms reset time delay
Package	DDF	SOT-23 8-pin (1.6 mm × 2.9 mm)
Reel	R	Large reel
Automotive version	Q1	Q100 AEC

Table 12-2. Device Threshold Table

ORDERABLE PART NAME	VARIANT	NUM CHAN	RESET TIME	SENSE1	SENSE2	SENSE3	SENSE4
TPS37042BJOFDDFRQ1	TPS37042	2	10ms	0.8V (±4%)	0.8V (±4%)	-	-
TPS37042A3OFDDFRQ1	TPS37042	2	10ms	3.3V (±5%)	1.2V (±5%)	-	-
TPS37043BJOFDDFRQ1	TPS37043	3	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	-
TPS37043A4OFDDFRQ1	TPS37043	3	10ms	2.8V (±5%)	1.8V (±5%)	1.2V (±5%)	-
TPS37043A8OFDDFRQ1	TPS37043	3	10ms	3.3V (±5%)	1.8V (±5%)	1.0V (±5%)	-
TPS37044BJOFDDFRQ1	TPS37044	4	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)
TPS37044A4OGDDFRQ1	TPS37044	4	10ms	3.3V (±8%)	1.8V (±4%)	1.15V (±6%)	1.15V (±6%)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS37042A3OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2A3FQ	Samples
TPS37043A4OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3A4FQ	Samples
TPS37043A8OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3A8FQ	Samples
TPS37043BJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BJFQ	Samples
TPS37044A4OGDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4A4GQ	Samples
TPS37044BJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4BJFQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3704-Q1 :

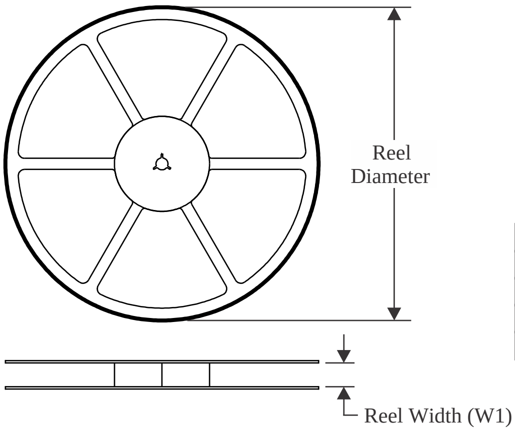
- Catalog : TPS3704

NOTE: Qualified Version Definitions:

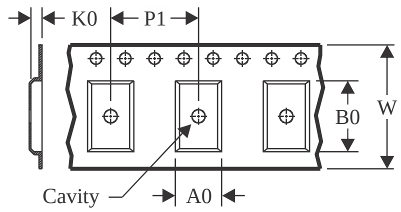
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

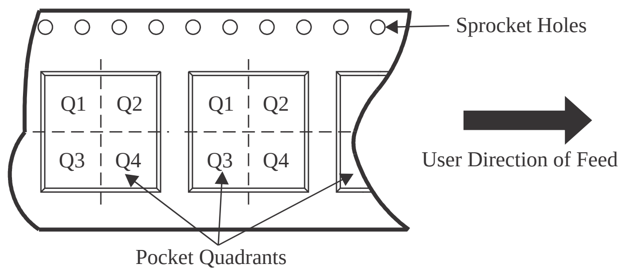


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

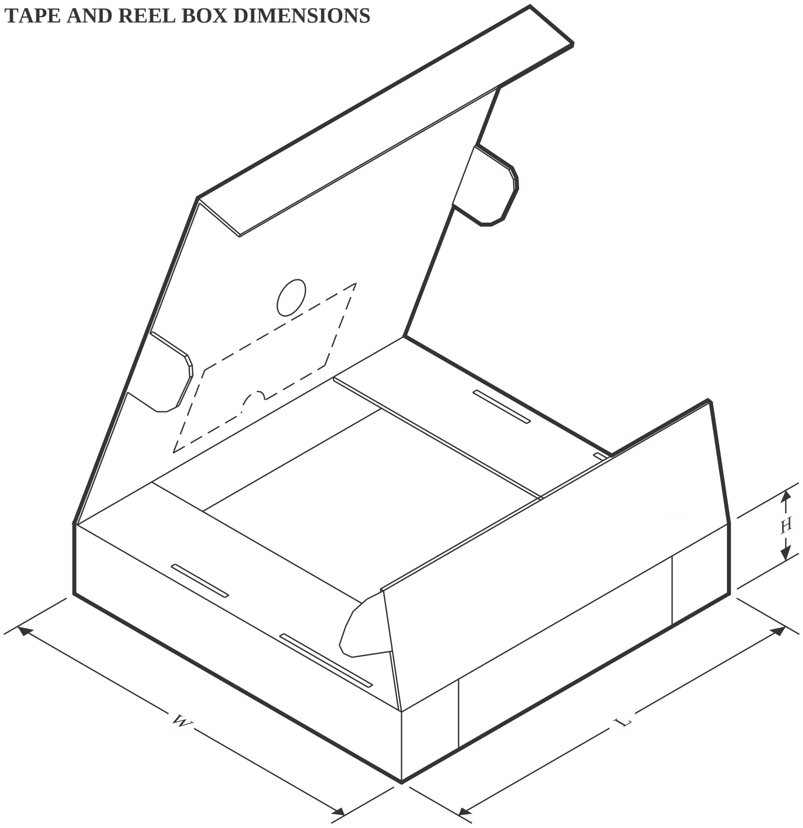
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

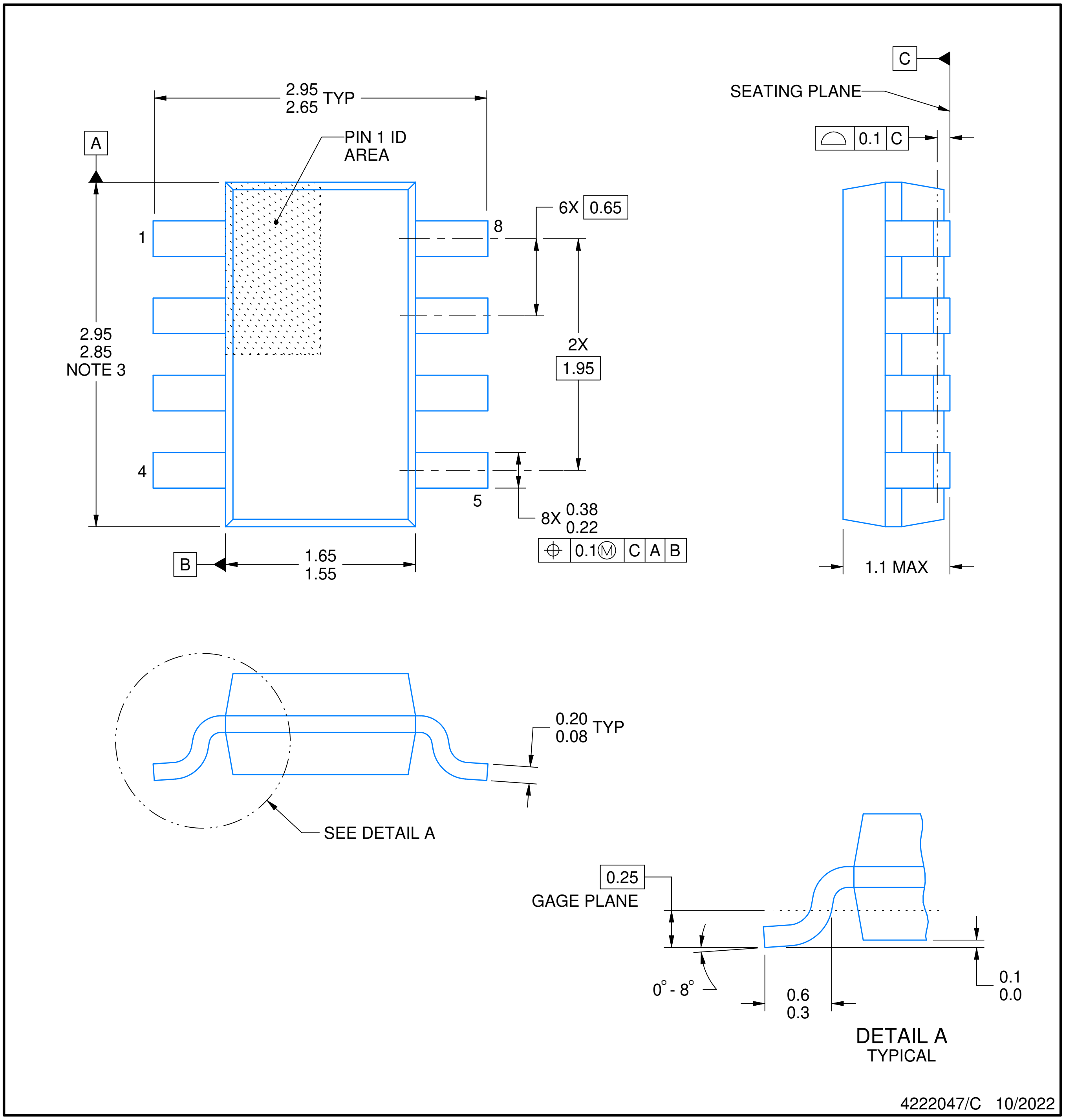
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS37042A3OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043A4OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043A8OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044A4OGDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS37042A3OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043A4OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043A8OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044A4OGDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0



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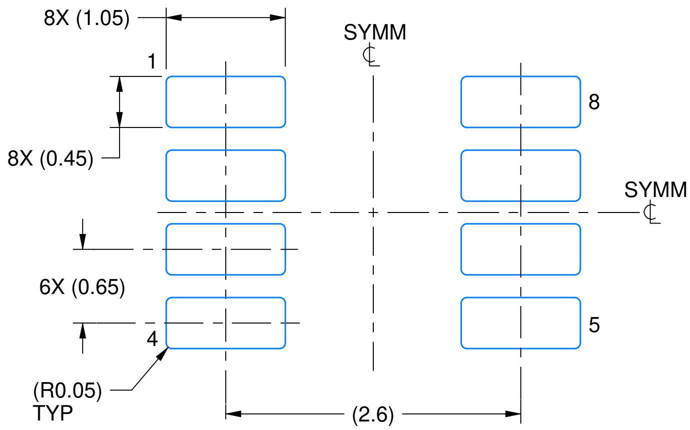
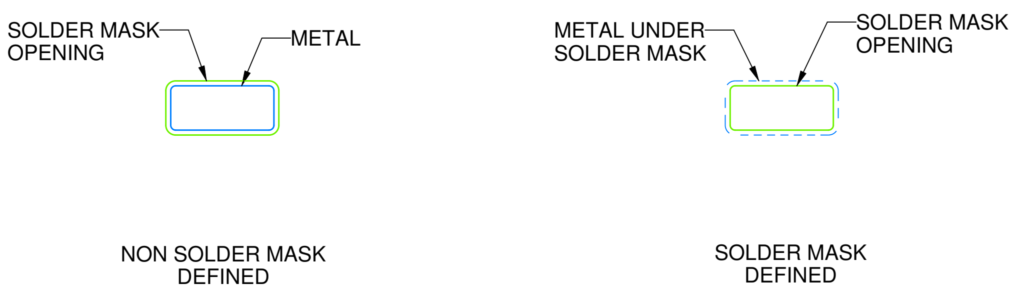
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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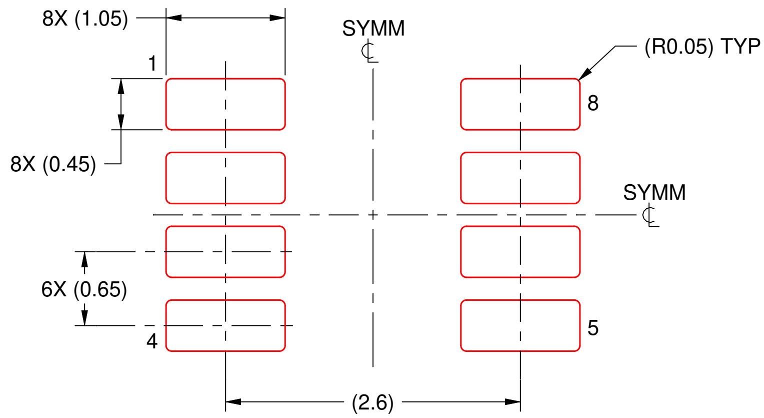
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.