To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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DATA SHEET

RENESAS

MOS FIELD EFFECT TRANSISTOR
2SK3482

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3482 is N-channel MOS Field Effect Transistor designed for high current switching applications.

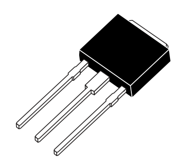
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 33 mΩ MAX. (V_{GS} = 10 V, I_D = 18 A)
  $R_{DS(on)2}$ = 39 mΩ MAX. (V_{GS} = 4.5 V, I_D = 18 A)
- Low C_{iss}: C_{iss} = 3600 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package

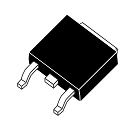
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3482	TO-251 (MP-3)
2SK3482-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±36	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±100	A
Total Power Dissipation (T_C = 25°C)	P_T	50	W
Total Power Dissipation (T_A = 25°C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	30	A
Single Avalanche Energy Note2	E_{AS}	90	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V

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Date Published June 2006 NS CP(K)
Printed in Japan

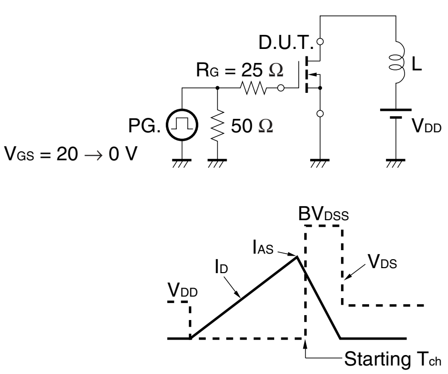
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

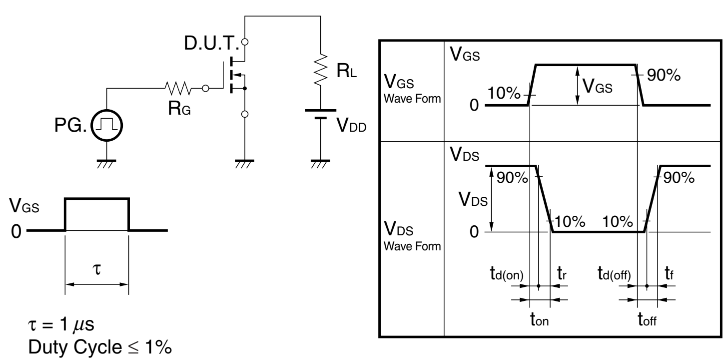
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 18 A	12	23		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 18 A		27	33	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 18 A		29	39	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		3600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		360		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		190		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 18 A		15		ns
Rise Time	t_r	V_{GS} = 10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		68		ns
Fall Time	t_f			6		ns
Total Gate Charge	Q_G	V_{DD} = 80 V		72		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		10		nC
Gate to Drain Charge	Q_{GD}	I_D = 36 A		19		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 36 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 36 A, V_{GS} = 0 V		70		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		180		nC

Note Pulsed

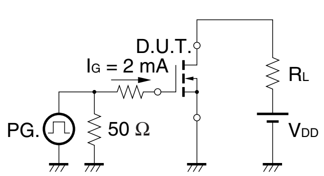
TEST CIRCUIT 1 AVALANCHE CAPABILITY



<R> **TEST CIRCUIT 2 SWITCHING TIME**

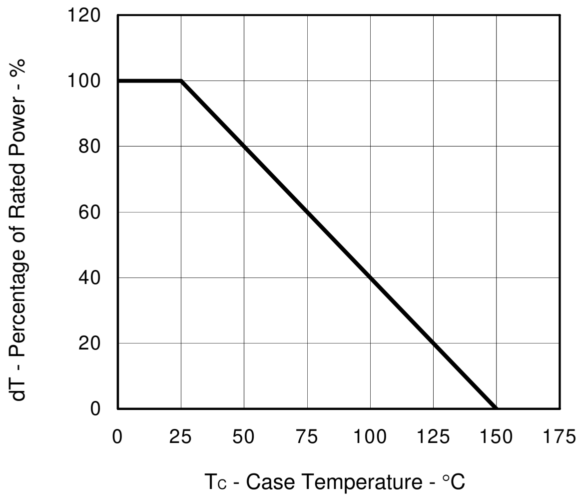


TEST CIRCUIT 3 GATE CHARGE

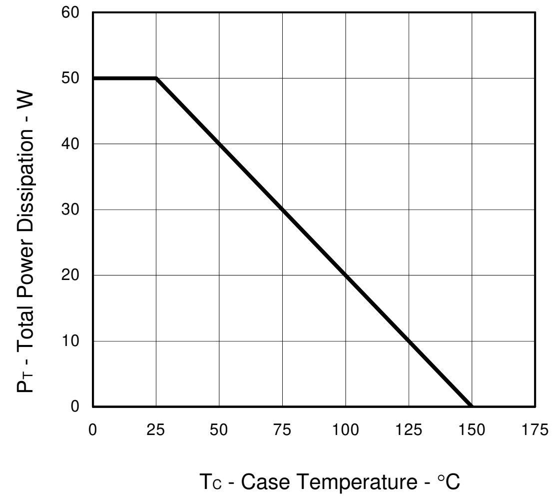


TYPICAL CHARACTERISTICS (TA = 25°C)

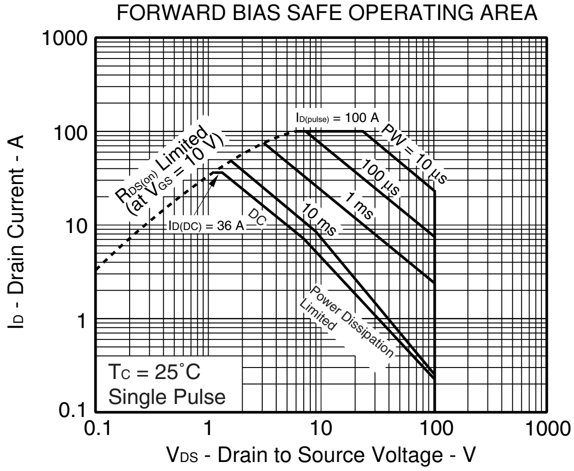
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



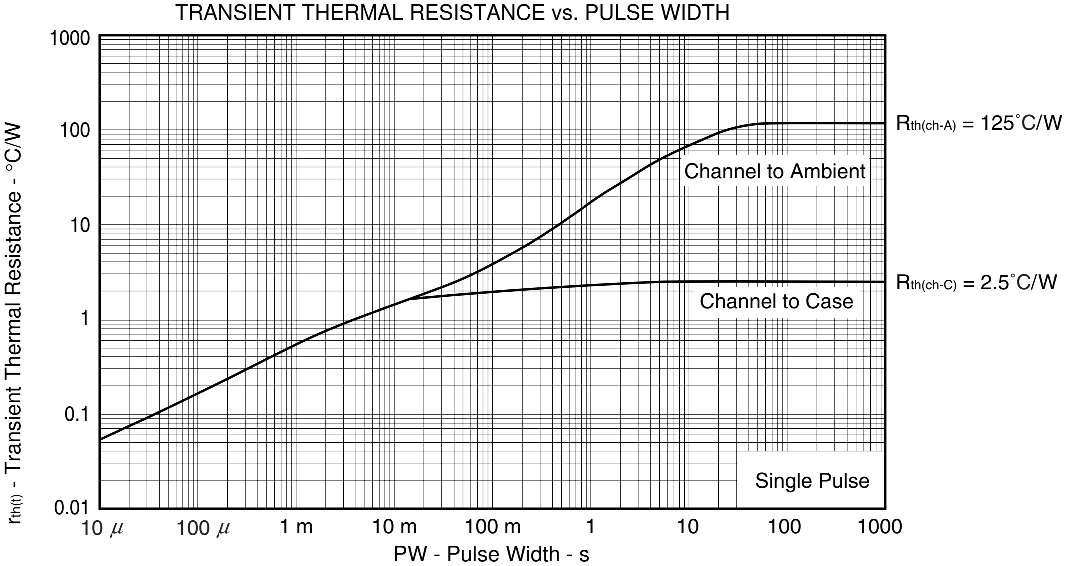
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



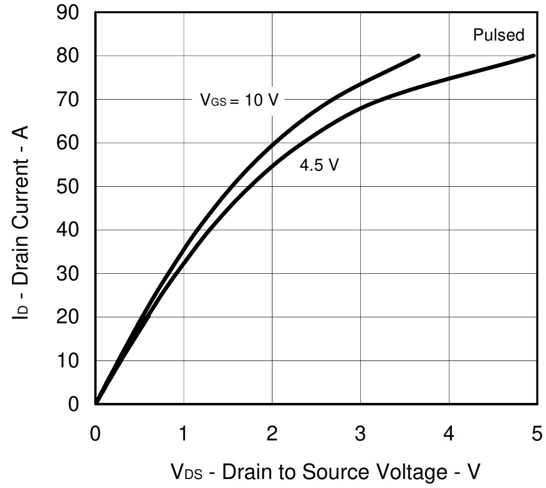
FORWARD BIAS SAFE OPERATING AREA



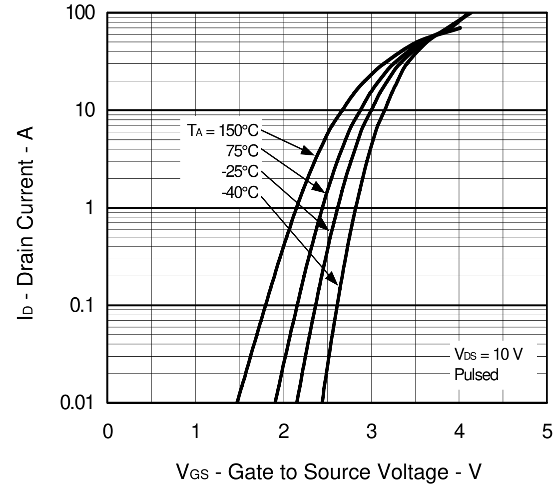
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



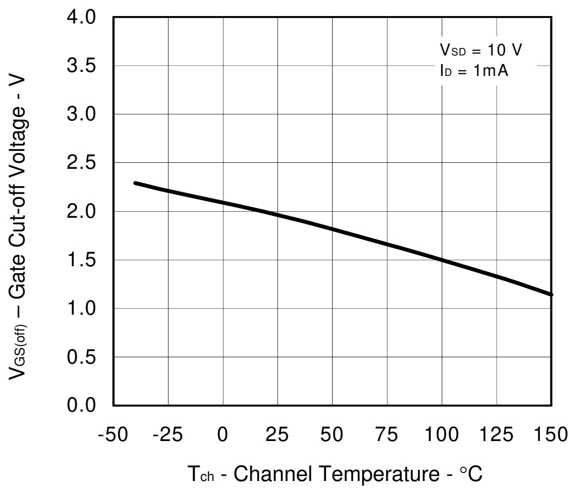
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



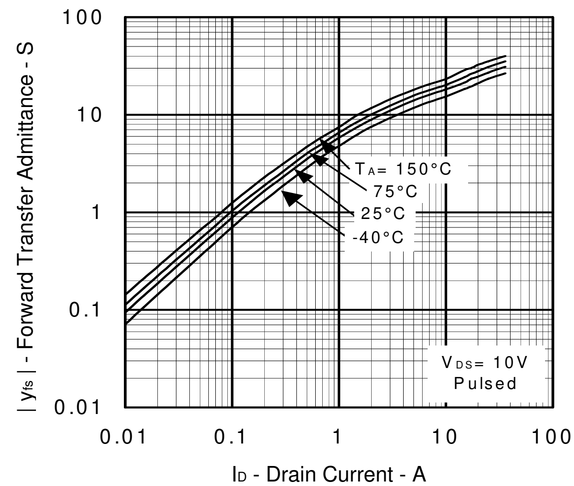
FORWARD TRANSFER CHARACTERISTICS



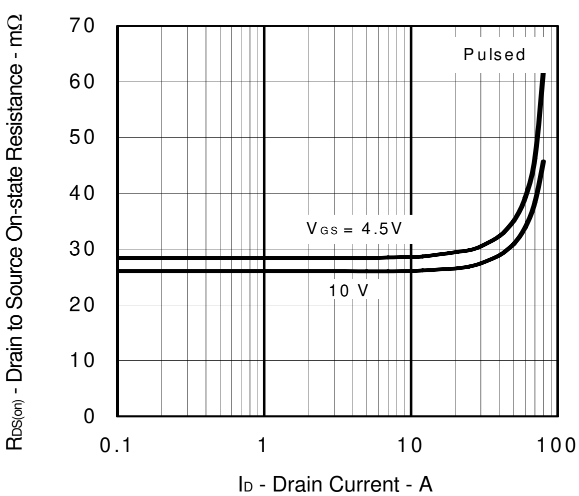
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



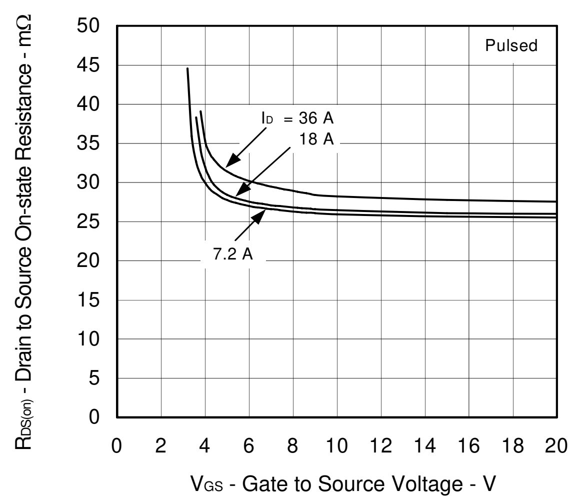
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



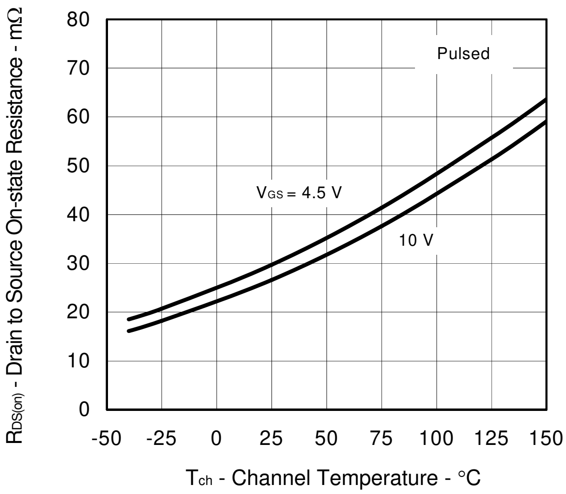
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



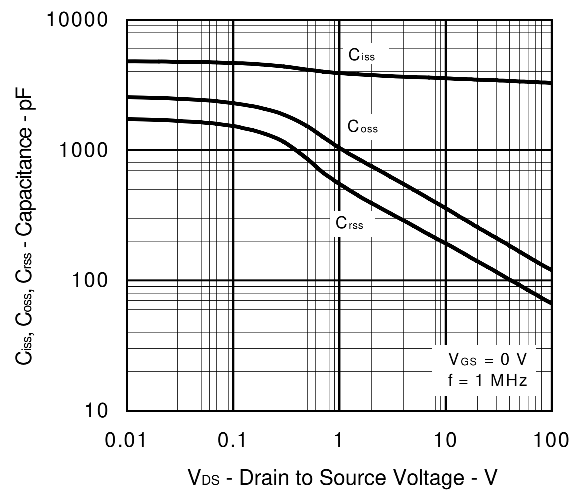
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



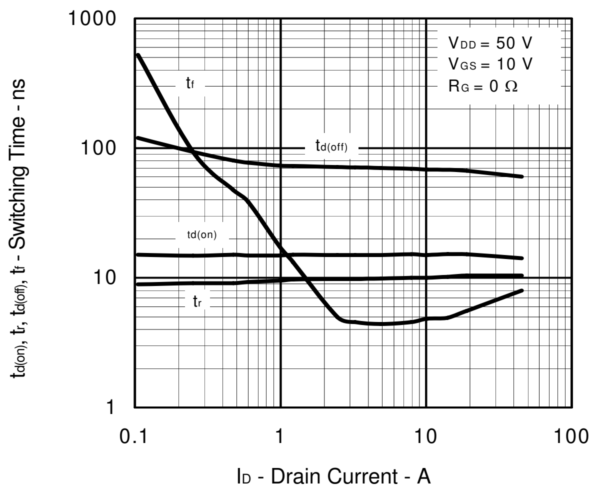
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



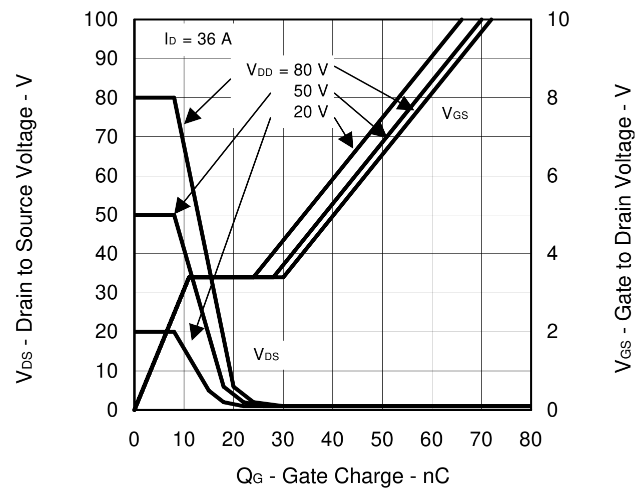
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



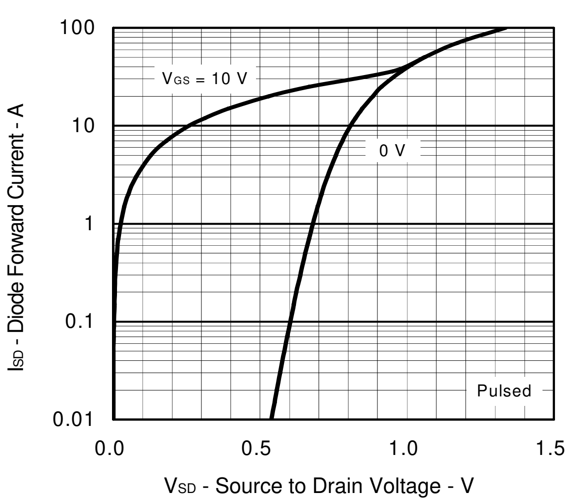
SWITCHING CHARACTERISTICS



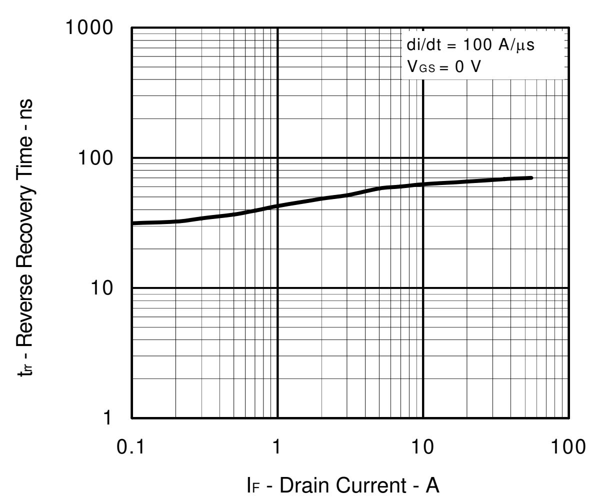
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



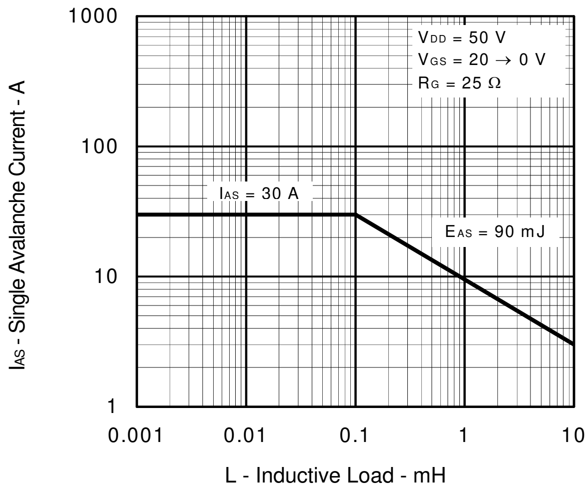
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



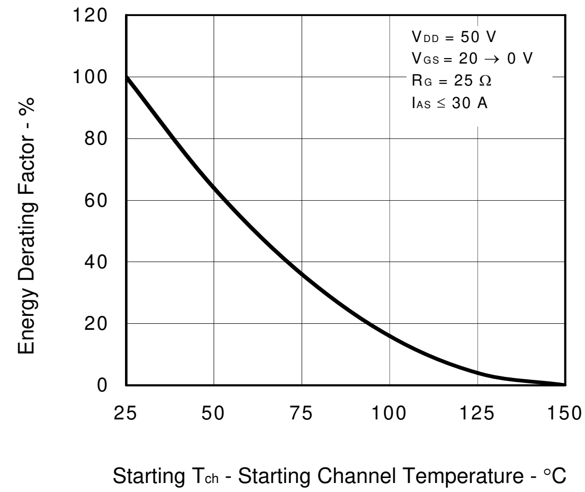
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

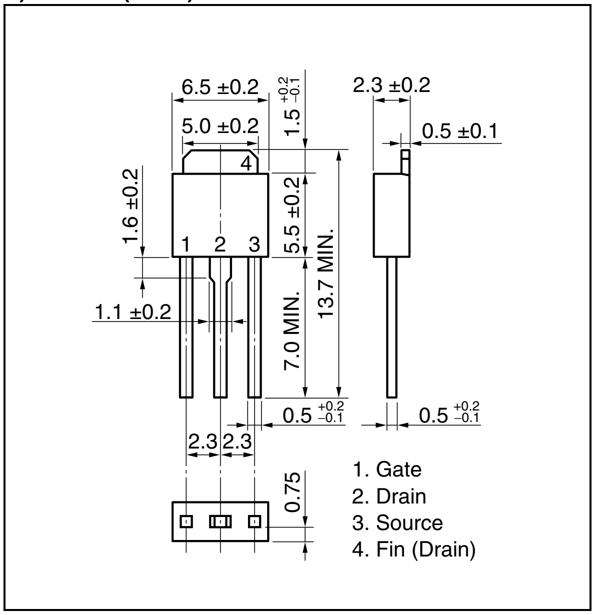


SINGLE AVALANCHE ENERGY
DERATING FACTOR

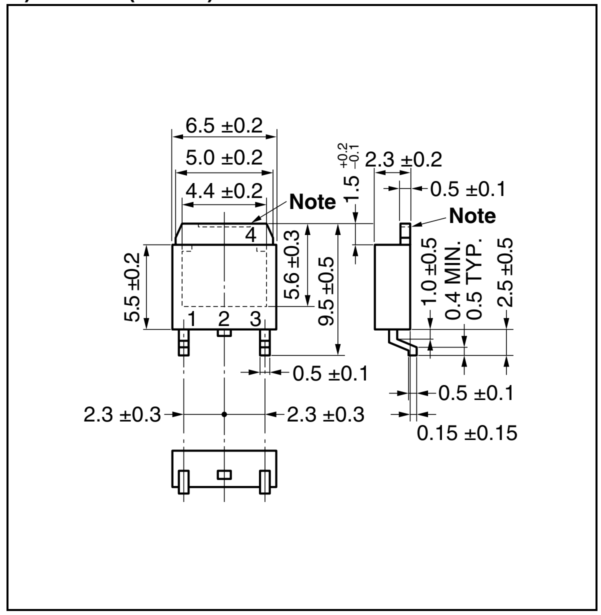


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

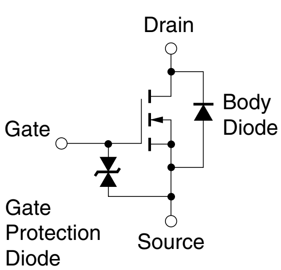


<R> 2) TO-252 (MP-3Z)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.