

# ON Semiconductor

## Is Now

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# FSB50760BSF / FSB50760BSFS

## Motion SPM<sup>®</sup> 5 SUPERFET<sup>®</sup> Series

### General Description

The FSB50760BSF / FSB50760BSFS is an advanced Motion SPM 5 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors such as refrigerators, fans and pumps. These modules integrate optimized gate drive of the built-in MOSFETs (SuperFET technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts and thermal monitoring. The built-in high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.

### Features

- UL Certified No. E209204 (UL1557)
- 600 V  $R_{DS(ON)} = 830 \text{ m}\Omega$  (Max) SuperFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Built-In Bootstrap Diodes Simplify PCB Layout
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500  $V_{rms}$  / min.
- Moisture Sensitive Level (MSL) 3
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives

### Related Source

- [RD-402: Reference Design for Motion SPM 5 Super-FET Series](#)
- [AN-9082 – Motion SPM5 Series Thermal Performance by Contact Pressure](#)
- [AN-9082: User's Guide for Motion SPM 5 Series V2](#)



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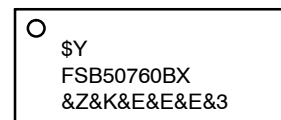


SPM5E-023 / 23LD, PDD STD  
CASE MODEJ



SPM5H-023 / 23LD, PDD STD,  
SPM23-BD  
CASE MODEM

### MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FSB50760X	= Specific Device Code
⇒ X	= SF or SFS

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FSB50760BSF / FSB50760BSFS

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
50760BSF	FSB50760BSF	SPM5P-023	Rail	NA	15
50760BSFS	FSB50760BSFS	SPM5Q-023	Tape & Reel	330 mm	450

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
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### INVERTER PART (Each MOSFET Unless Otherwise Specified)

V <sub>PN</sub>	DC Link Input Voltage, Drain-Source Voltage of Each MOSFET		600	V
BV <sub>DSS</sub>	Drain-Source Voltage	V <sub>IN</sub> = 0V, I <sub>D</sub> = 250 μA	600	V
I <sub>PN</sub>	Zero-Bias Static Leakage Current	V <sub>PN</sub> = 400 V, V <sub>IN</sub> = 0 V, V <sub>DD</sub> = V <sub>BS</sub> = 0 V, T <sub>C</sub> = T <sub>J</sub> = 25°C for all phase	40	μA
*I <sub>D 25</sub>	Each MOSFET Drain Current, Continuous	T <sub>C</sub> = 25°C	3.6	A
*I <sub>D 80</sub>	Each MOSFET Drain Current, Continuous	T <sub>C</sub> = 80°C	2.7	A
*I <sub>DP</sub>	Each MOSFET Drain Current, Peak	T <sub>C</sub> = 25°C, PW < 100 μs	9.4	A
*I <sub>DRMS</sub>	Each MOSFET Drain Current, Rms	T <sub>C</sub> = 80°C, F <sub>PWM</sub> < 20 kHz	1.9	A <sub>rms</sub>
*P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> = 25°C, For Each MOSFET	14.5	W

### CONTROL PART (Each HVIC Unless Otherwise Specified)

V <sub>DD</sub>	Control Supply Voltage	Applied Between V <sub>DD</sub> and COM	20	V
V <sub>BS</sub>	High-side Bias Voltage	Applied Between V <sub>B</sub> and V <sub>S</sub>	20	V
V <sub>IN</sub>	Input Signal Voltage	Applied Between IN and COM	-0.3 ~ V <sub>DD</sub> +0.3	V

### BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified.)

V <sub>RRMB</sub>	Maximum Repetitive Reverse Voltage		600	V
* I <sub>FB</sub>	Forward Current	T <sub>C</sub> = 25°C	0.5	A
* I <sub>FPB</sub>	Forward Current (Peak)	T <sub>C</sub> = 25°C, Under 1ms Pulse Width	1.5	A

### THERMAL RESISTANCE

R <sub>th(j-c)Q</sub>	Junction to Case Thermal Resistance (Note 1)	Inverter MOSFET part, (Per Module)	2.15	°C/W
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### TOTAL SYSTEM

T <sub>J</sub>	Operating Junction Temperature		-40 ~ 150	°C
T <sub>STG</sub>	Storage Temperature		-40 ~ 125	°C
V <sub>ISO</sub>	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connection Pins to Heatsink	1500	V <sub>rms</sub>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

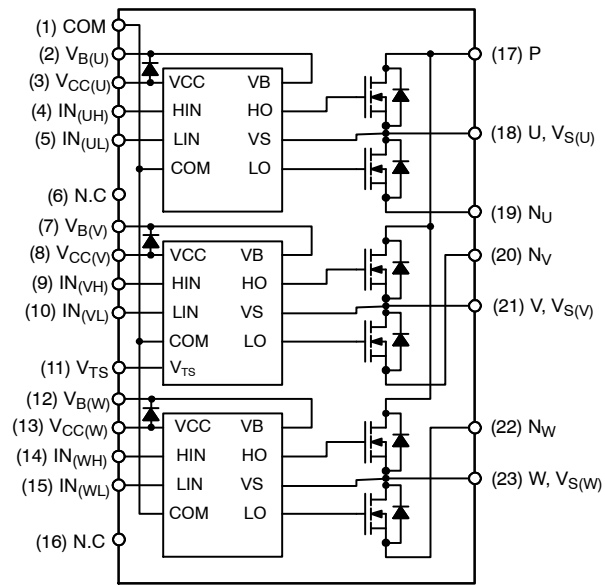
1. For the Measurement Point of Case Temperature T<sub>C</sub>, Please refer to Figure 4.
2. Marking “\*” Is Calculation Value or Design Factor.
3. Using continuously under heavy loads or excessive assembly conditions (e.g. the application of high temperature/ current/ voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/ current/ voltage, etc.) are within the absolute maximum ratings and the operating ranges.

## FSB50760BSF / FSB50760BSFS

### PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{DD(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	N.C	N.C
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{DD(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{TS}$	Output for HVIC Temperature Sensing
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{DD(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	N.C	N.C
17	P	Positive DC-Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	$N_U$	Negative DC-Link Input for U Phase
20	$N_V$	Negative DC-Link Input for V Phase
21	V, $V_{S(V)}$	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	$N_W$	Negative DC-Link Input for W Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving

## FSB50760BSF / FSB50760BSFS



4. Source Terminal of Each Low-Side MOSFET is Not Connected to Supply Ground or Bias Voltage Ground Inside Motion SPM 5 product. External Connections Should be Made as Indicated in Figure 3.

**Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)**

# FSB50760BSF / FSB50760BSFS

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , $V_{DD} = V_{BS} = 15\text{ V}$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### INVERTER PART (Each MOSFET Unless Otherwise Specified)

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{IN} = 0\text{ V}$ , $I_D = 1\text{ mA}$ (Note 5)	600	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{IN} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$	-	-	1	mA
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{DD} = V_{BS} = 15\text{ V}$ , $V_{IN} = 5\text{ V}$ , $I_D = 2\text{ A}$	-	0.59	0.83	$\Omega$
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{DD} = V_{BS} = 15\text{ V}$ , $V_{IN} = 0\text{ V}$ , $I_D = -2\text{ A}$	-	-	1.2	V
$t_{ON}$	Switching Times	$V_{PN} = 300\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_D = 2\text{ A}$ ON / OFF $R_G = 1.5\text{ K}\Omega / 200\text{ }\Omega$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive Load $L = 3\text{ mH}$ High- and Low-Side MOSFET Switching (Note 6)	-	980	-	ns
$t_{OFF}$			-	1280	-	ns
$t_{rr}$			-	200	-	ns
$E_{ON}$			-	110	-	$\mu\text{J}$
$E_{OFF}$			-	13	-	$\mu\text{J}$
RBSOA	Reverse-Bias Safe Operating Area	$V_{PN} = 400\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_D = I_{DP}$ , $V_{DS} = BV_{DSS}$ , $T_J = 150^\circ\text{C}$ High- and Low-Side MOSFET Switching (Note 7)	Full Square			

### CONTROL PART (Each HVIC Unless Otherwise Specified)

$I_{QDD}$	Quiescent $V_{DD}$ Current	$V_{DD} = 15\text{ V}$ , $V_{IN} = 0\text{ V}$	Applied Between $V_{DD}$ and COM	-	-	200	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Current	$V_{BS} = 15\text{ V}$ , $V_{IN} = 0\text{ V}$	Applied Between $V_{B(U)-U}$ , $V_{B(V)-V}$ , $V_{B(W)-W}$	-	-	100	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Supply	$V_{DD} - \text{COM}$	$V_{DD} = 15\text{ V}$ , $f_{PWM} = 20\text{ kHz}$ , Duty = 50%, Applied to One PWM Signal Input for Low-Side	-	-	900	$\mu\text{A}$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$V_{B(U)-V_{S(U)}}$ , $V_{B(V)-V_{S(V)}}$ , $V_{B(W)-V_{S(W)}}$	$V_{DD} = V_{BS} = 15\text{ V}$ , $f_{PWM} = 20\text{ kHz}$ , Duty = 50%, Applied to One PWM Signal Input for High-Side	-	-	800	$\mu\text{A}$
$UV_{DDD}$	Low-Side Undervoltage Protection (Figure 8)	$V_{DD}$ Undervoltage Protection Detection Level		7.4	8.0	9.4	V
$UV_{DDR}$		$V_{DD}$ Undervoltage Protection Reset Level		8.0	8.9	9.8	V
$UV_{BSD}$	High-Side Undervoltage Protection (Figure 9)	$V_{BS}$ Undervoltage Protection Detection Level		7.4	8.0	9.4	V
$UV_{BSR}$		$V_{BS}$ Undervoltage Protection Reset Level		8.0	8.9	9.8	V
$V_{TS}$	HVIC Temperature sensing voltage output	$V_{DD} = 15\text{ V}$ , $T_{HVIC} = 25^\circ\text{C}$ (Note 8)		600	790	980	mV
$V_{IH}$	ON Threshold Voltage	Logic High Level	Applied between IN and COM	-	-	2.9	V
$V_{IL}$	OFF Threshold Voltage	Logic Low Level		0.8	-	-	V

### BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified)

$V_{FB}$	Forward Voltage	$I_F = 0.1\text{ A}$ , $T_C = 25^\circ\text{C}$ (Note 9)	-	2.5	-	V
$t_{rrB}$	Reverse Recovery Time	$I_F = 0.1\text{ A}$ , $T_C = 25^\circ\text{C}$	-	80	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{PN}$	Supply Voltage	Applied between P and N	-	300	400	V
$V_{DD}$	Control Supply Voltage	Applied between $V_{DD}$ and COM	13.5	15.0	16.5	V
$V_{BS}$	High-Side Bias Voltage	Applied between $V_B$ and $V_S$	13.5	15.0	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between $V_{IN}$ and COM	3.0	-	$V_{DD}$	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
$t_{dead}$	Blanking Time for Preventing Arm-Short	$V_{DD} = V_{BS} = 13.5 \sim 16.5 \text{ V}, T_J \leq 150^\circ\text{C}$	1.0	-	-	$\mu\text{s}$
$f_{PWM}$	PWM Switching Frequency	$T_J \leq 150^\circ\text{C}$	-	20	-	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

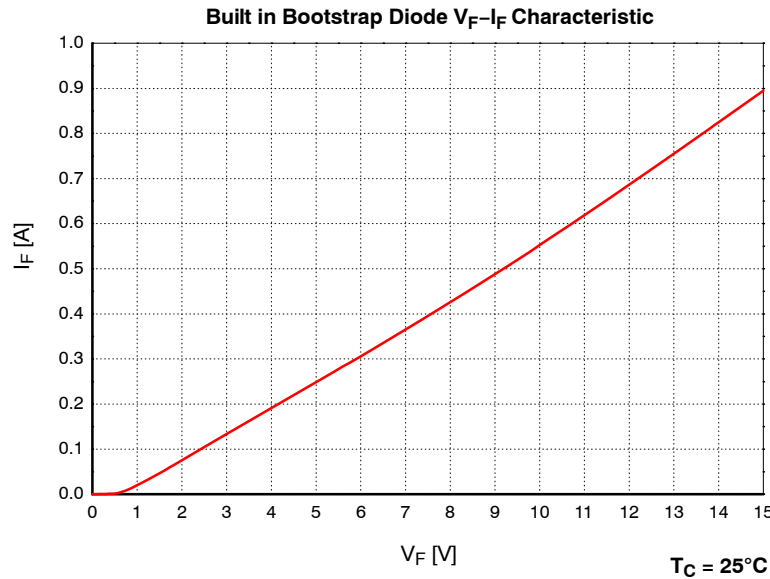


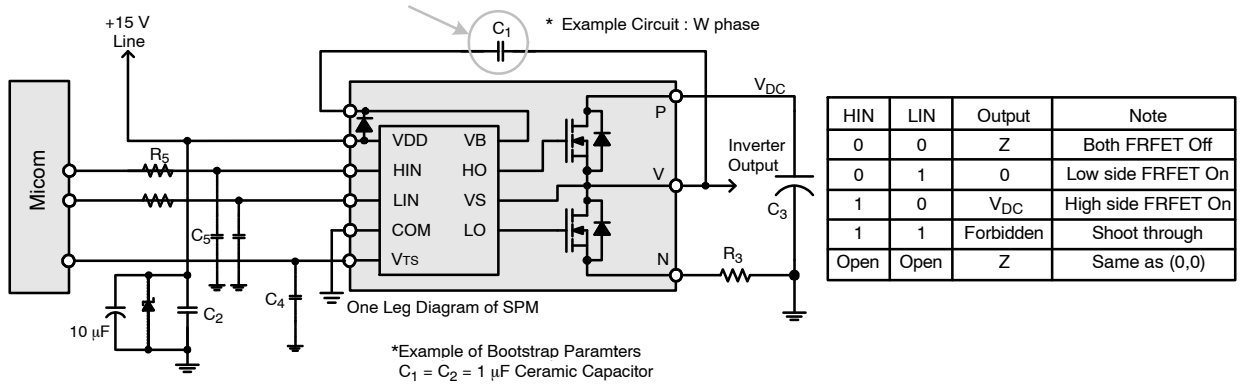
Figure 2. Built in Bootstrap Diode Characteristics (Typical)

NOTES:

5.  $BV_{DSS}$  is the Absolute Maximum Voltage Rating Between Drain and Source Terminal of Each MOSFET Inside Motion SPM 5 product.  $V_{PN}$  Should be Sufficiently Less Than This Value Considering the Effect of the Stray Inductance so that  $V_{DS}$  Should Not Exceed  $BV_{DSS}$  in Any Case.
6.  $t_{ON}$  and  $t_{OFF}$  Include the Propagation Delay Time of the Internal Drive IC. Listed Values are Measured at the Laboratory Test Condition, and They Can be Different According to the Field Applications Due to the Effect of Different Printed Circuit Boards and Wirings. Please see Figure 6 for the Switching Time Definition with the Switching Test Circuit of Figure 7.
7. The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 6 for the RBSOA test circuit that is same as the switching test circuit.
8.  $V_{TS}$  is only for sensing temperature of module and cannot shutdown MOSFETs automatically.
9. Built in bootstrap diode includes around  $15 \Omega$  resistance characteristic. Please refer to Figure 2.

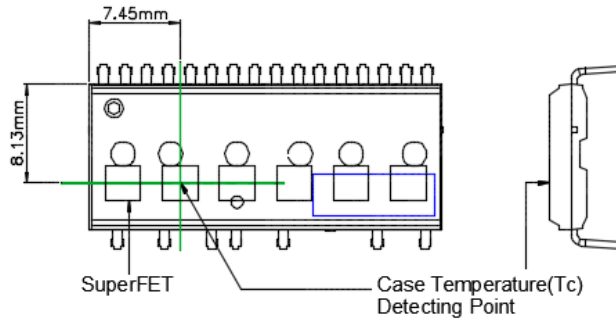
# FSB50760BSF / FSB50760BSFS

These values depend on PWM control algorithm



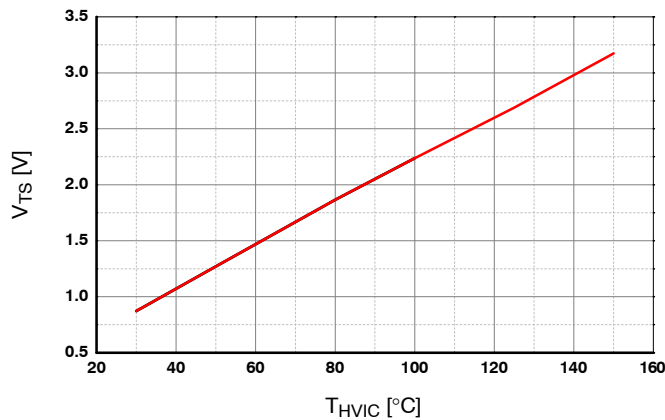
- Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- RC coupling ( $R_5$  and  $C_5$ ) and  $C_4$  at each input of Motion SPM and Micom (Indicated as Dotted Lines) may be used to prevent improper signal due to surge noise.
- Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as  $C_1$ ,  $C_2$  and  $C_3$  should have good high frequency characteristics to absorb high-frequency ripple current.

**Figure 3. Recommended MCU Interface and Bootstrap Circuit with Parameters**



- Attach the thermocouple on top of the heatsink-side of SPM (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

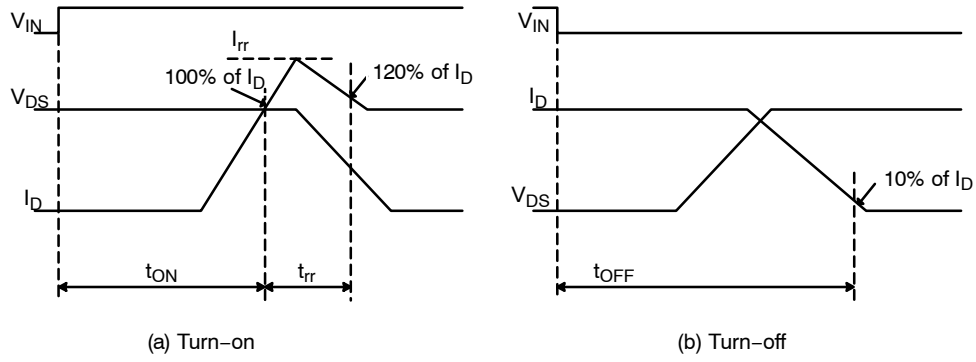
**Figure 4. Case Temperature Measurement**



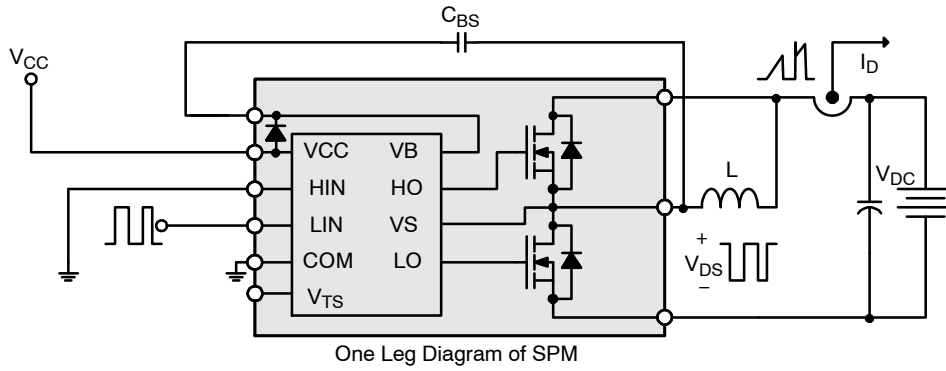
**Figure 5. Temperature Profile of  $V_{TS}$  (Typical)**



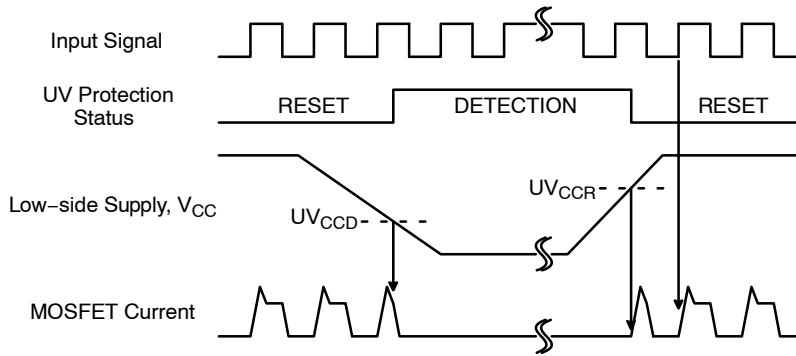
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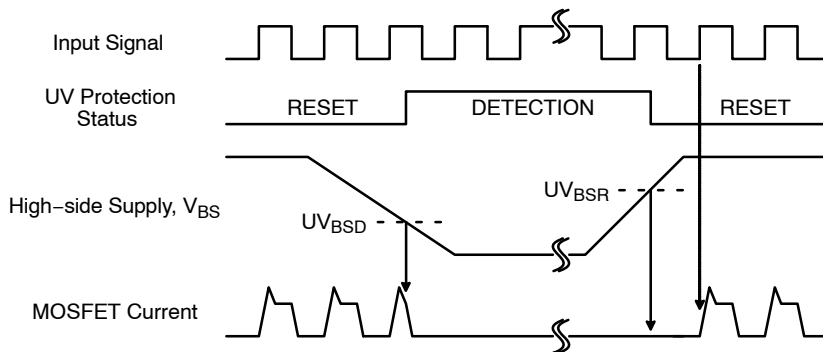
**Figure 6. Switching Time Definitions**



**Figure 7. Switching and RBSOA (Single-Pulse) Test Circuit (Low-side)**



**Figure 8. Under-Voltage Protection (Low-Side)**



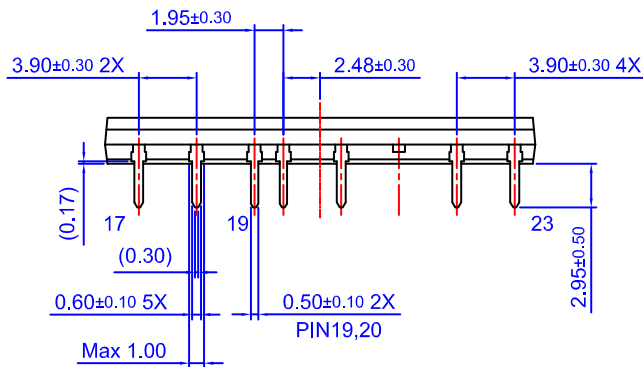
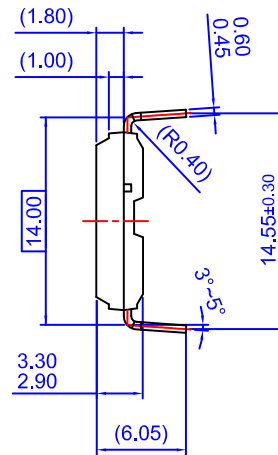
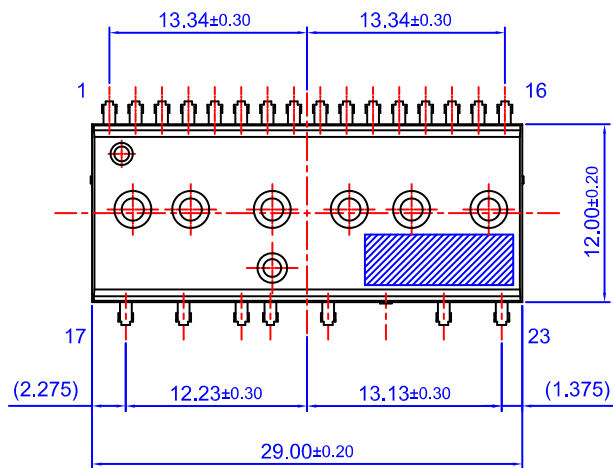
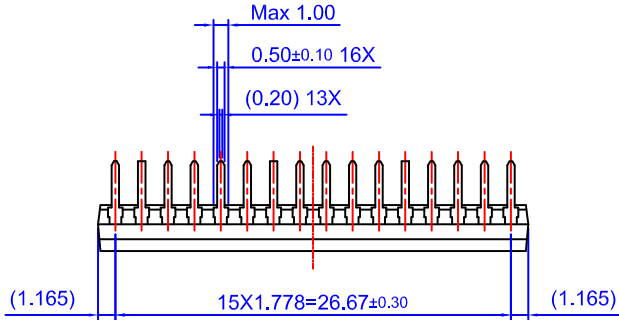
**Figure 9. Under-Voltage Protection (High-Side)**



# FSB50760BSF / FSB50760BSFS

## PACKAGE DIMENSIONS

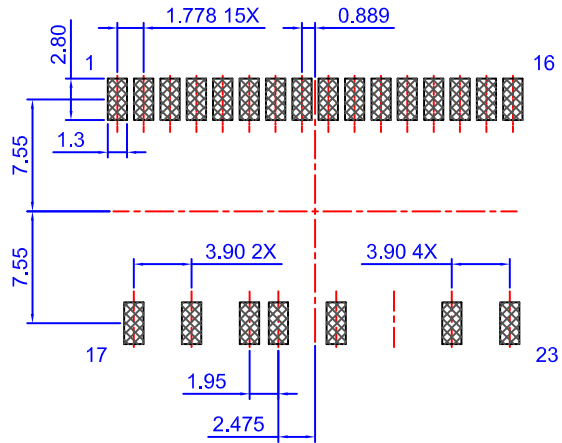
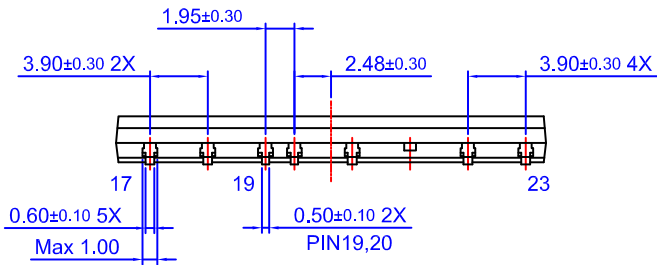
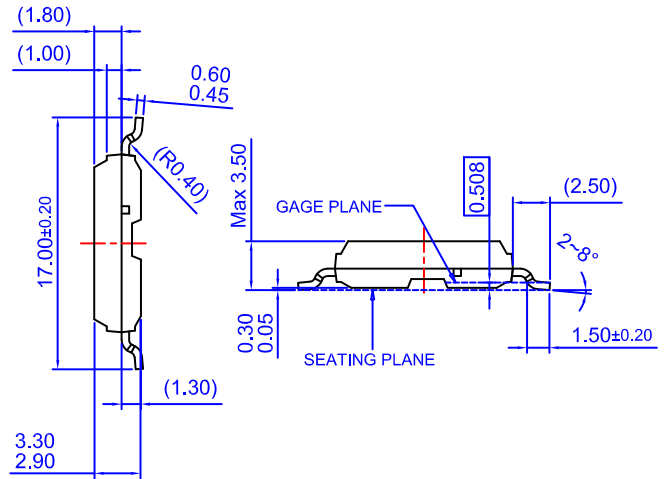
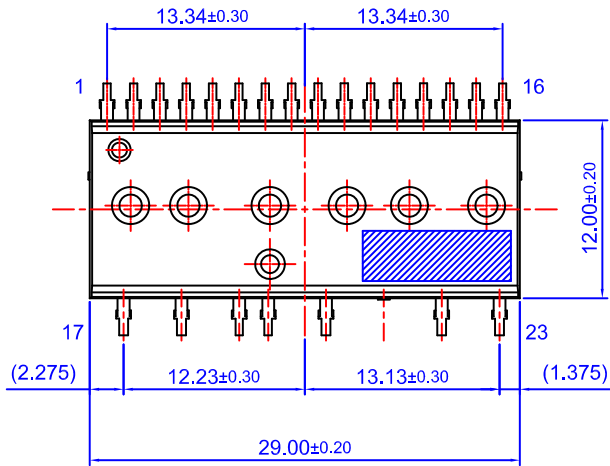
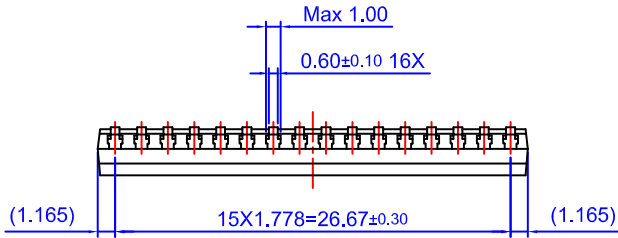
SPM5E-023 / 23LD, PDD STD, FULL PACK, DIP TYPE  
CASE MODE J  
ISSUE O



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SPM5H-023 / 23LD, PDD STD, SPM23-BD (Ver1.5) SMD TYPE  
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