BVA305C

DIGITAL VARIABLE GAIN AMPLIFIER

40MHz - 5000MHz

Device Features

- Integrate DSA to Amp Functionality
- 40-5000MHz Broadband Performance
- 14.3dB Gain @ 1.9GHz
- 3.6dB Noise Figure at max gain setting @ 1.9GHz
- 14.0dBm P1dB @ 1.9GHz
- 27.7dBm OIP3 @ 1.9GHz
- No matching circuit needed
- Attenuation: 0.5 dB steps up to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- Wide Power supply range of +2.7 to +5.5V (DSA)
- Single Fixed +3V supply (Amp)
- High attenuation accuracy (DSA to Amp)
  ±(0.25 + 3% x Atten) @ 1.9 GHz
- 1.8V control logic compatible
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

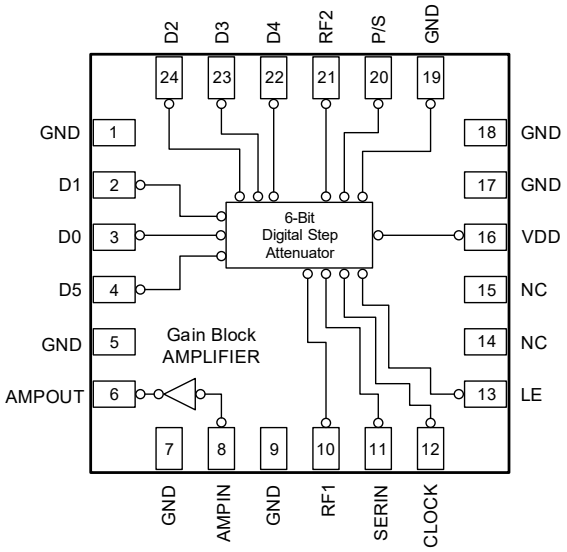


Figure 2. Functional Block Diagram

Product Description

The BVA305C is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 3V supply with a broadband frequency range of 40MHz to 5000MHz.

The BVA305C integrates a high performance digital step attenuator and a high linearity, broadband gain block amplifier using the small package (4x4mm QFN package) and operating voltage 3V DC .

Both DSA and gain block amplifier in BVA305C are internally matched to 50 Ohms and It is easy to use with no external matching components required.

The BVA305C always initialize to the maximum attenuation setting on power-up for both Serial and Parallel mode until next programming word is inputted.

The BVA305C is targeted for use in wireless infrastructure, point-to-point or can be used for any general purpose wireless application.

Application

- 3G/4G/5G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			40		5000	MHz
Gain[2]		Attenuation = 0dB @ 1900MHz		14.3		dB
Attenuation Control range		0.5dB Step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	0.04GHz - 1GHz	Any bit or bit combination			±(0.25 + 2.5% of Attenuation setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of Attenuation setting)	
	2GHz - 3GHz				±(0.25 + 3.5% of Attenuation setting)	
	3GHz - 4GHz				±(0.25 + 4% of Attenuation setting)	
	4GHz - 5GHz				±(0.25 + 4.5% of Attenuation setting)	
Input Return loss	0.04GHz - 2GHz	Attenuation = 0dB		15		dB
	2GHz - 4GHz			17		
	4GHz - 5GHz			10		
Output Return loss	0.04GHz - 2GHz			18		
	2GHz - 4GHz			12		
	4GHz - 5GHz			12		
Output Power for 1dB Compression		Attenuation = 0dB @ 1900MHz		14.0		dBm
Output Third Order Intercept Point[3]		Attenuation = 0dB @ 1900MHz		27.7		dBm
		Output power = 0dBm / tone, Separated by 1MHz				
Noise Figure		Attenuation = 0dB @ 1900MHz		3.6		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		3		V
Supply Current			40	52	60	mA
Control Interface		Serial / parallel mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Maximum Spurious level[4]		Measured @ DSA RF1, RF2 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3V, measure on Evaluation Board (DSA to AMP)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of 0dBm per tone separated by 1MHz.
4. The unwanted spurious due to built-in negative voltage generator. Typical generated fundamental frequency is 6MHz.

Table 2. Typical RF Performance[1]

Parameter	Frequency							Unit
	70[2]	900[3]	1900[3]	2140[3]	2650[3]	3500[3]	4600[4]	MHz
Gain[4]	17.4	16.0	14.3	13.8	12.7	11.4	9.9	dB
S11	-12.8	-18.2	-20.9	-21.3	-19.8	-15.6	-10.2	dB
S22	-23.4	-16.3	-16.8	-15.6	-13.8	-11.4	-14.1	dB
OIP3[5]	31.0	30.6	27.7	27.2	26.5	24.7	22.7	dBm
P1dB	14.8	14.9	14.0	13.7	13.3	12.6	12.0	dBm
Noise Figure	2.8	3.2	3.6	3.7	3.9	4.1	4.8	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3V,50 Ω system. measure on Evaluation Board. (DSA to AMP)
2. 70MHz measured with application circuit refer to table 13.
3. 900MHz, 1900MHz, 2140MHz, 2650MHz, 3500MHz measured with application circuit refer to table 15.
4. 4600MHz measured with application circuit refer to table 17.
5. Gain data has PCB & Connectors insertion loss de-embedded.
6. OIP3 measured with two tones at an output of 0dBm per tone separated by 1MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	Amp/DSA			3.6 / 5.5	V
Supply Current	Amp		110		mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+12 / +30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Amp + DSA	40		5000	MHz
Supply Voltage	Amp		3		V
	DSA	2.7		5.5	V
Operating Temperature	Amp + DSA	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

Figure 3. Pin Configuration (Top View)

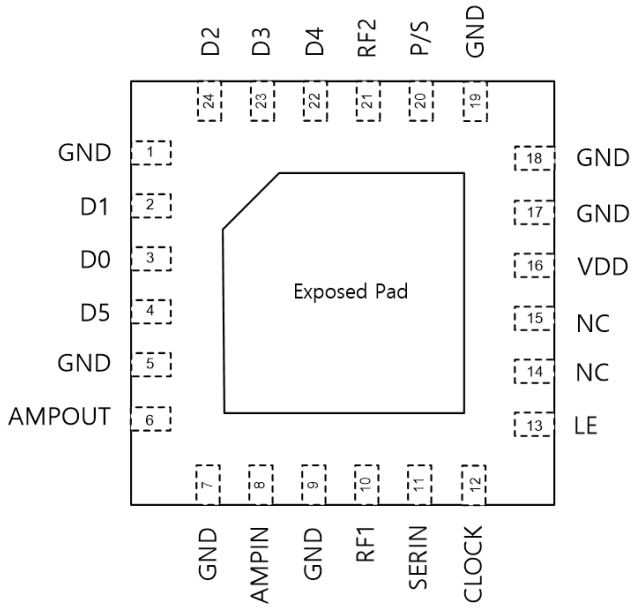


Table 5. Pin Description

Pin	Pin name	Description
1,5,7,9,17,18,19	GND	Ground, These pins must be connected to ground
2	D1	Parallel Control Voltage Inputs, Attenuation control bit 1dB
3	D0	Parallel Control Voltage Inputs, Attenuation control bit 0.5dB
4	D5	Parallel Control Voltage Inputs, Attenuation control bit 16dB
6	AMPOUT	RF Gain block Amplifier output Port
8	AMPIN	RF Gain block Amplifier input Port
10	RF1[1]	RF1 port (Digital Step Attenuator RF Input) This pin can also be used as an output because the design is bidirectional. RF1 is DC-coupled and matched to 50 Ω
11	SERIN	Serial interface data input
12	CLOCK	Serial interface clock input
13	LE	Latch Enable input
14, 15	NC	Not connected, It is recommended to connect to ground.
16	VDD	DSA Power Supply (nominal 3V)
20	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
21	RF2[1]	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bidirectional. RF2 is DC-coupled and matched to 50 Ω.
22	D4	Parallel Control Voltage Inputs, Attenuation control bit 8dB
23	D3	Parallel Control Voltage Inputs, Attenuation control bit 4dB
24	D2	Parallel Control Voltage Inputs, Attenuation control bit 2dB
EXPOSE PAD	GND	Exposed pad: The exposed pad must be connected to ground for proper operation

Note: 1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met

Programming Options

BVA305C can be programmed using either the parallel or serial interface, which is selectable via P/S pin (Pin20).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW.

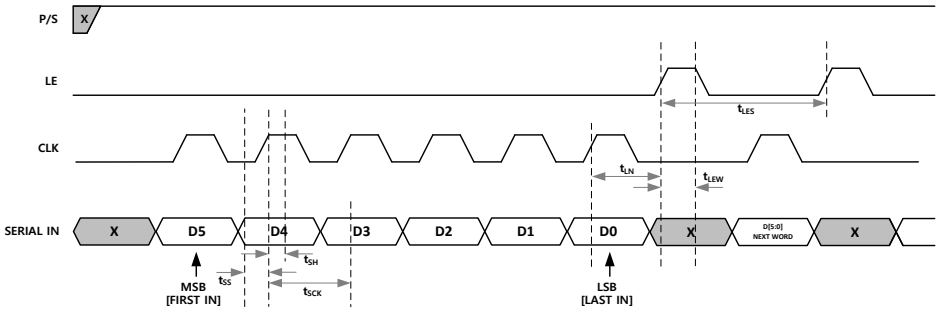
Serial Control Mode

The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (2,3,4,22,23,24) should be grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 6. 6-Bit Serial Word Sequence

D5	Attenuation 16dB Control Bit
D4	Attenuation 8dB Control Bit
D3	Attenuation 4dB Control Bit
D2	Attenuation 2dB Control Bit
D1	Attenuation 1dB Control Bit
D0	Attenuation 0.5dB Control Bit

Figure 4. Serial Mode Resister Timing Diagram



The BVA305C has a 3-wire serial peripheral interface (SPI): serial data input (Data), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled HIGH to latch the new attenuation state into the device. LE must be set to LOW to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept HIGH (see Figure 4 and Table 9).

Table 7. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns
t_{LES}	Minimum LE pulse spacing	600			ns

Table 9. Truth Table for Serial Control Word

Digital Control Input						Attenuation
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	(dB)
LOW	LOW	LOW	LOW	LOW	LOW	0 (Reference)
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

Parallel Control Mode

The BVA305C has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 10. The parallel control interface is activated when P/S is set to LOW. There are two modes of parallel operation: direct parallel and latched parallel

Direct Parallel Mode

The LE pin must be kept High. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 2, 3, 4, 22,23, 24]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled LOW to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 5 and Table 11).

Power-UP Status

The BVA305C basically is set the maximum attenuation state when the initially powered up for all serial and latched parallel mode status until the next programming word is inputted.

If the BVA305C powered up in serial mode, all parallel control pins should be set to logic Low.

Figure 5. Latched Parallel Mode Timing Diagram

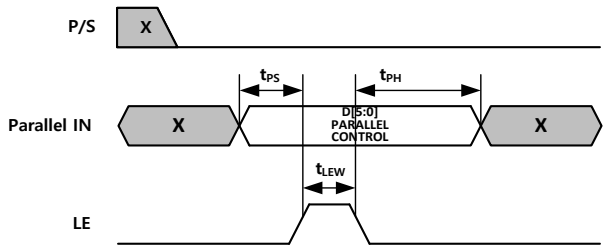


Table 10. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Table 11. Truth Table for the Parallel Control Word

D0	D1	D2	D3	D4	D5	P/S	LE	Attenuation State
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	Reference Loss
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0.5dB
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	1dB
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	2dB
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	4dB
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	8dB
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	16dB
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5dB

Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:40 ~ 800MHz)

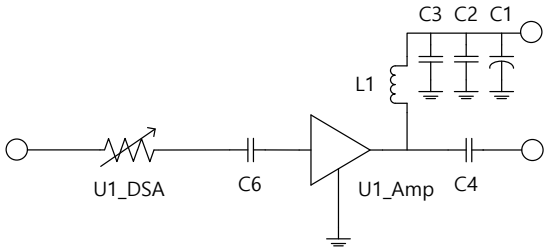
Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 13

Table 12. Typical RF Performance(40 ~ 800MHz)

parameter	Frequency			Unit
	70	200	500	MHz
Gain[1]	17.4	17.1	16.7	dB
S11	-12.8	-24.1	-26.9	dB
S22	-23.4	-23.7	-19.9	dB
OIP3[2]	31.0	31.3	31.3	dBm
P1dB	14.8	15.0	15.3	dBm
N.F	2.8	2.8	2.9	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 13. 40~800MHz IF Application Circuit



Application Circuit Values	Frequency band	IF Circuit
		40MHz ~ 800MHz
	C6/C4	2.2nF[1]
	L1	330nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 6. Gain vs. Frequency
over Temperature

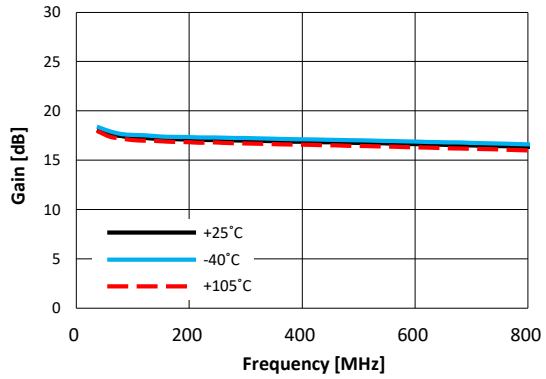


Figure 7. Gain vs. Frequency
over Major Attenuation States

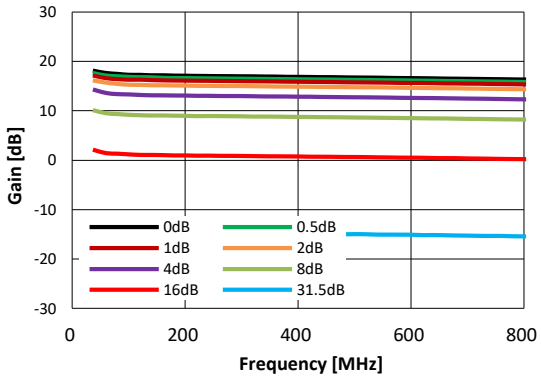


Figure 8. Input Return Loss vs. Frequency
over Major Attenuation States

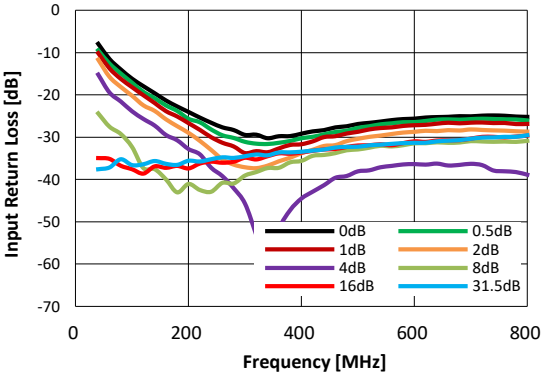
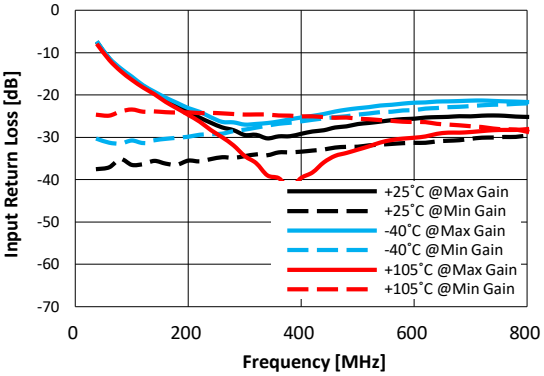


Figure 9. Input Return Loss vs. Frequency
over Temperature (Min / Max Gain State)



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:40 ~ 800MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 13

Figure 10. Output Return Loss vs. Frequency
over Major Attenuation States

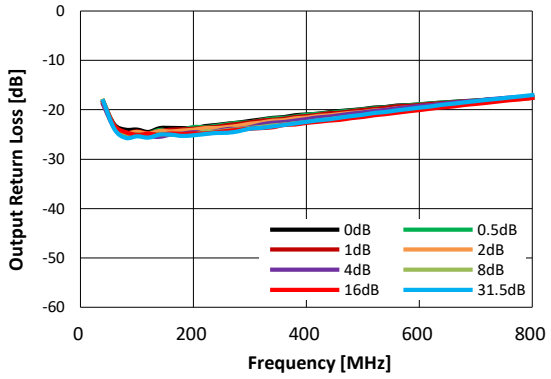
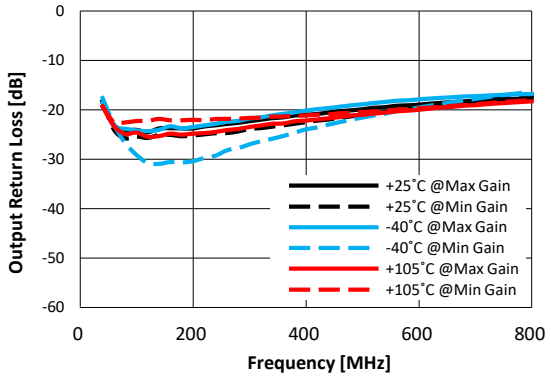


Figure 11. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 12. OIP3 vs. Frequency
Over Temperature (Max Gain State)

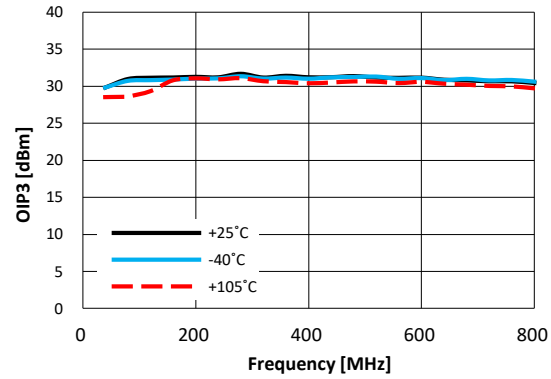


Figure 13. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

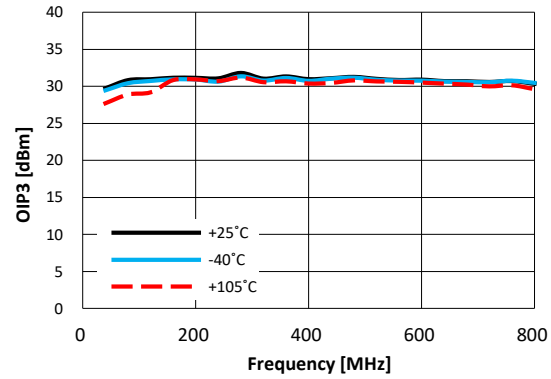


Figure 14. P1dB vs. Frequency
Over Temperature (Max Gain State)

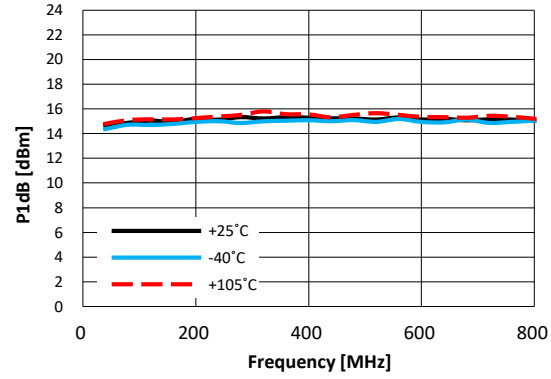
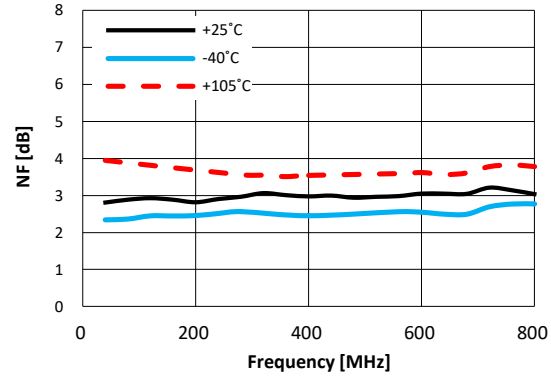


Figure 15. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:40 ~ 800MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 13

Figure 16. Attenuation Error vs Frequency
over Major Attenuation Steps

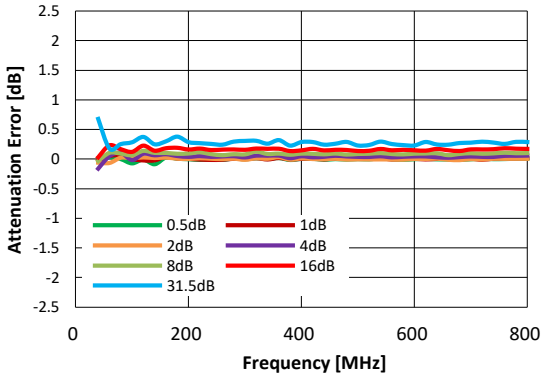


Figure 17. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

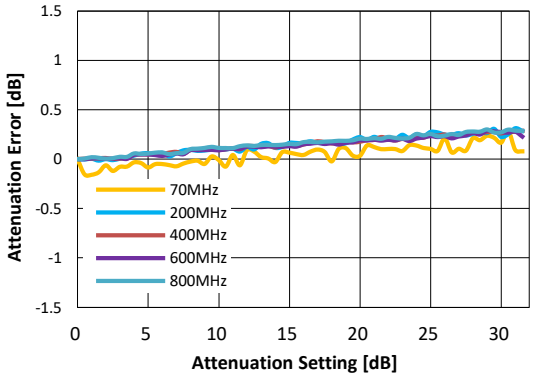


Figure 18. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency

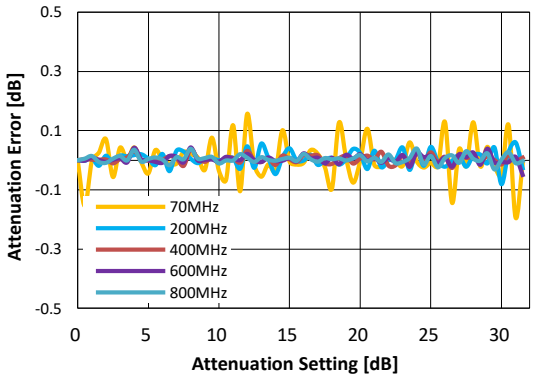


Figure 19. Attenuation Error at 70MHz vs Temperature
Over All Attenuation States

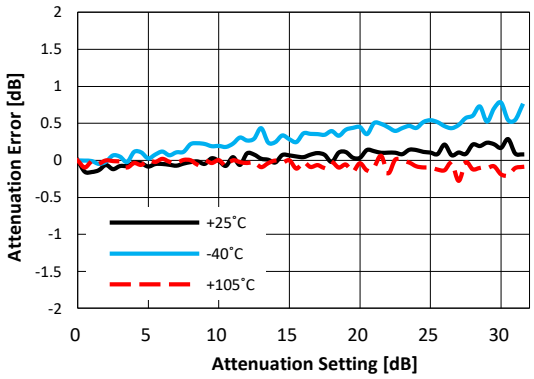


Figure 20. Attenuation Error at 200MHz vs Temperature
Over All Attenuation States

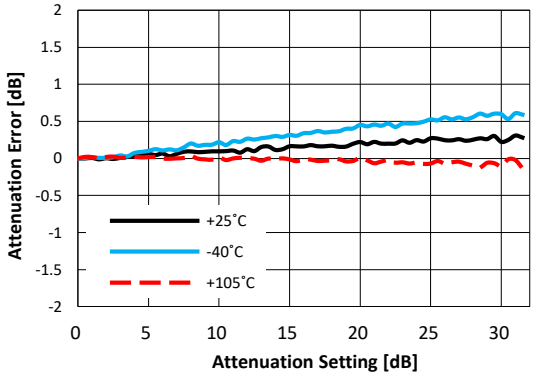
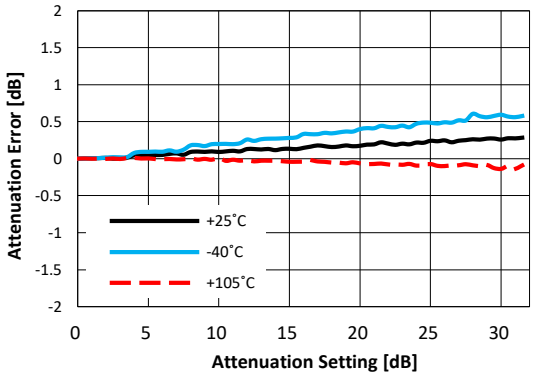


Figure 21. Attenuation Error at 400MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:40 ~ 800MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 13

Figure 22. Attenuation Error at 600MHz vs Temperature
Over All Attenuation States

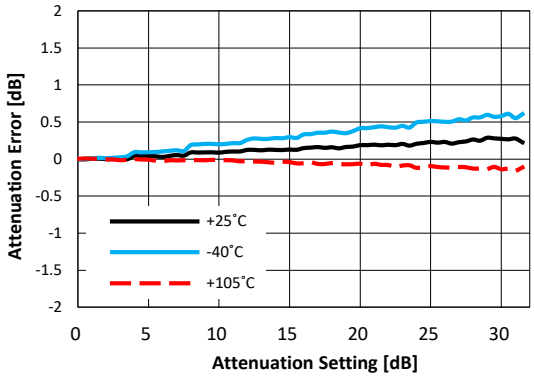
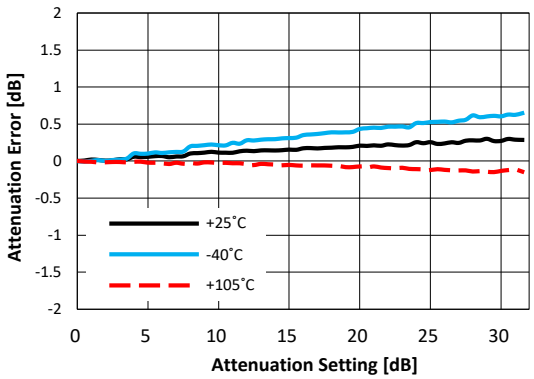


Figure 23. Attenuation Error at 800MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:800 ~ 4000MHz)

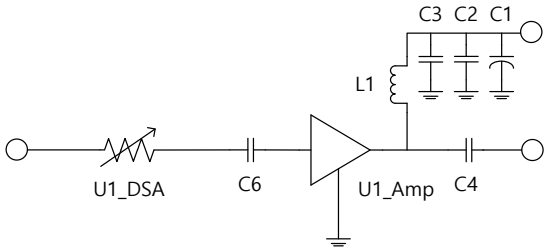
Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 15

Table 14. Typical RF Performance(800 ~ 4000MHz)

parameter	Frequency					Unit
	900	1900	2140	2650	3500	MHz
Gain[1]	16.0	14.3	13.8	12.7	11.4	dB
S11	-18.2	-20.9	-21.3	-19.8	-15.6	dB
S22	-16.3	-16.8	-15.6	-13.8	-11.4	dB
OIP3[2]	30.6	27.7	27.2	26.5	24.7	dBm
P1dB	14.9	14.0	13.7	13.3	12.6	dBm
N.F	3.2	3.6	3.7	3.9	4.1	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 15. 800 ~ 4000MHz RF Application Circuit



Application Circuit Values	Frequency band	RF Circuit
		800MHz ~ 4000MHz
	C6/C4	22pF[1]
	L1	18nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 24. Gain vs. Frequency
over Temperature (Max Gain State)

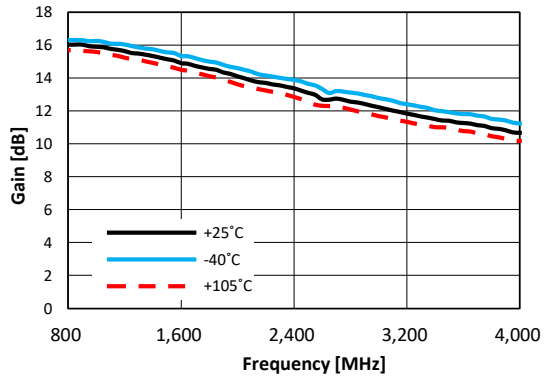


Figure 25. Gain vs. Frequency
over Major Attenuation States

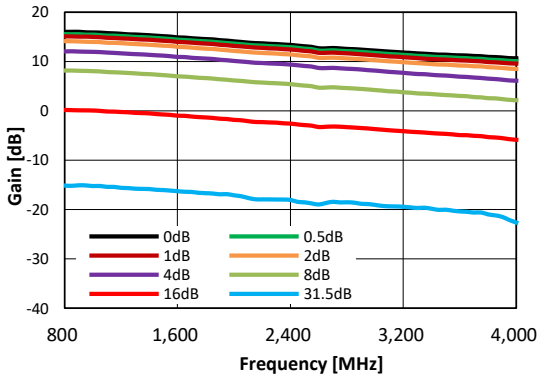


Figure 26. Input Return Loss vs. Frequency
over Major Attenuation States

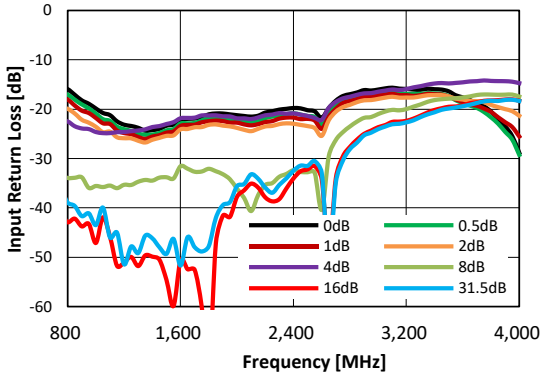
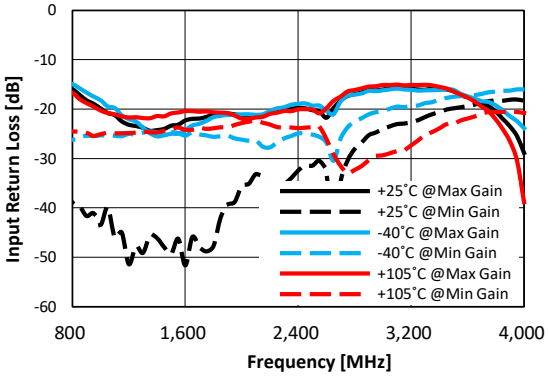


Figure 27. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 15

Figure 28. Output Return Loss vs. Frequency
over Major Attenuation States

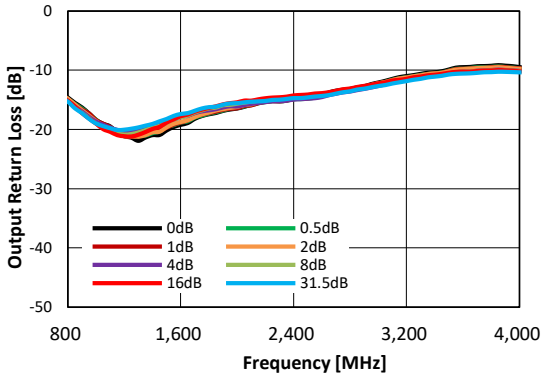
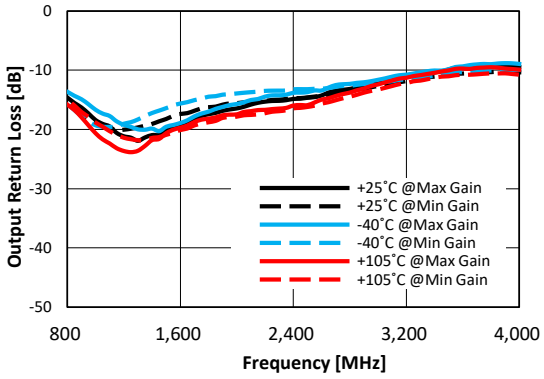


Figure 29. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 30. OIP3 vs. Frequency
Over Temperature (Max Gain State)

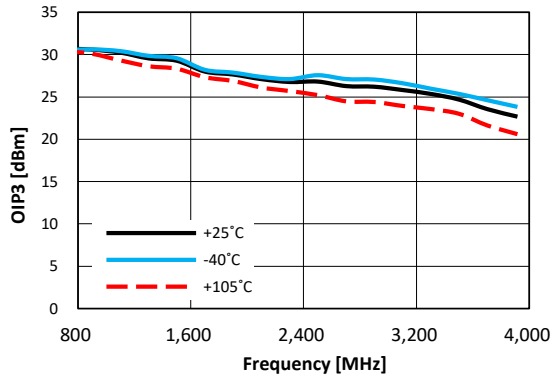


Figure 31. OIP3 vs. Frequency
Over Temperature (15.5dB Atteuation State)

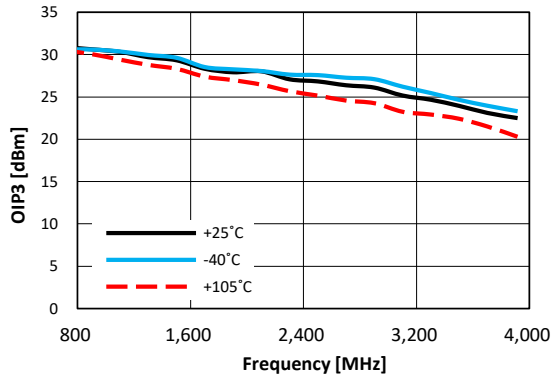


Figure 32. P1dB vs. Frequency
Over Temperature (Max Gain State)

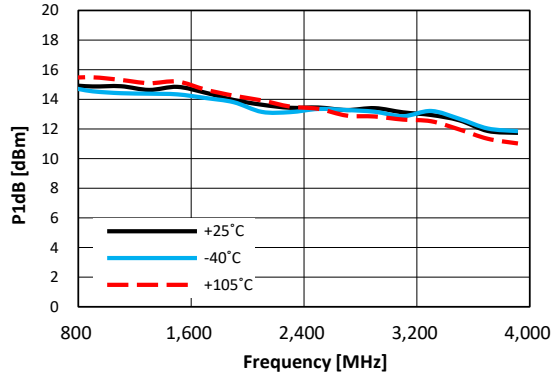
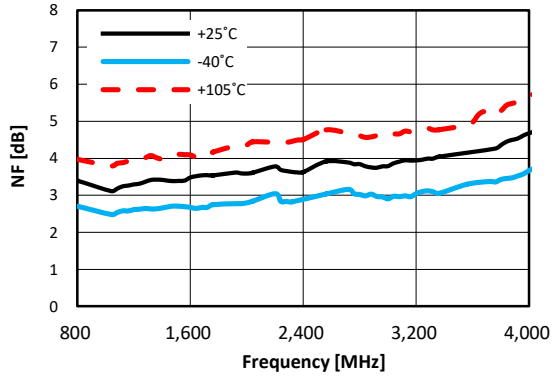


Figure 33. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 15

Figure 34. Attenuation Error vs Frequency
over Major Attenuation Steps

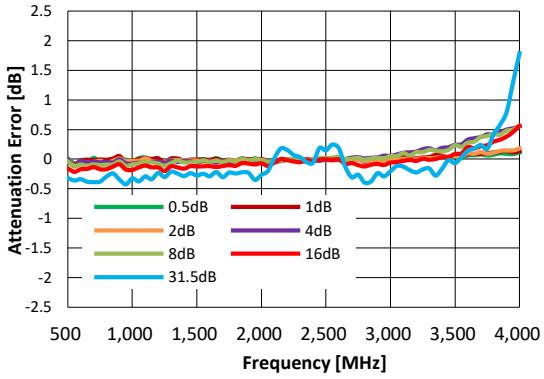


Figure 35. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

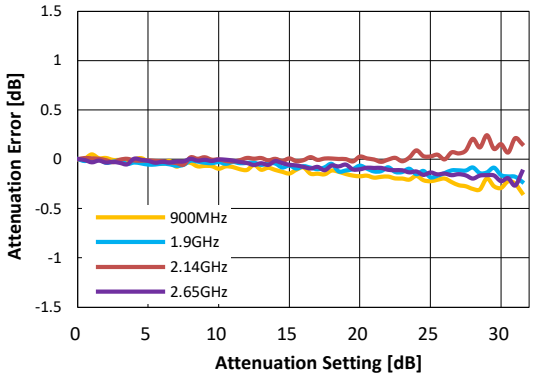


Figure 36. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency (Max Gain State)

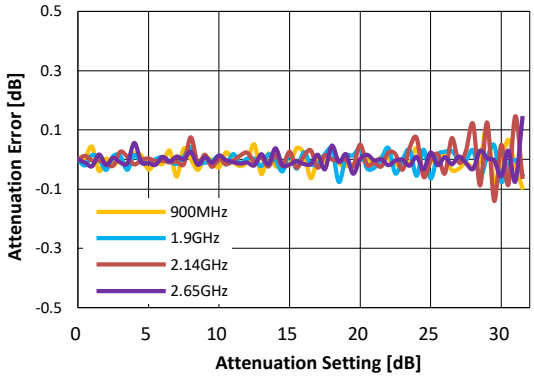


Figure 37. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States

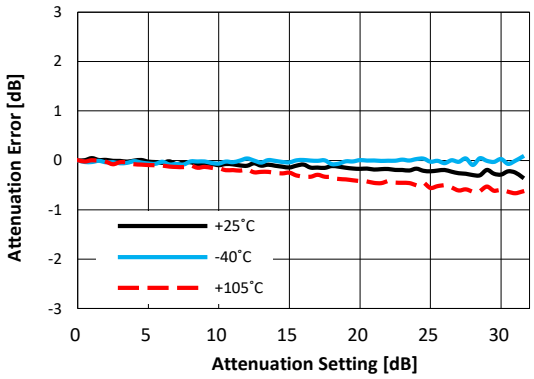


Figure 38. Attenuation Error at 1.9GHz vs Temperature
Over All Attenuation States

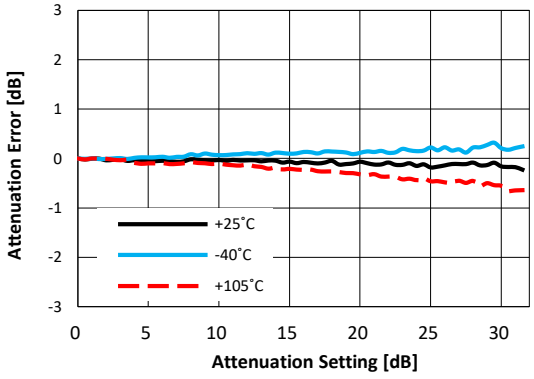
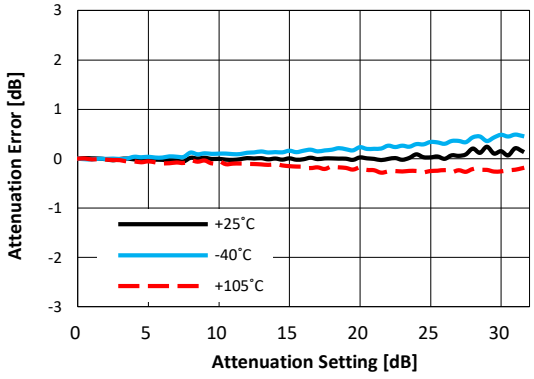


Figure 39. Attenuation Error at 2.14GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:800 ~ 4000MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 15

Figure 40. Attenuation Error at 2.65GHz vs Temperature

Over All Attenuation States

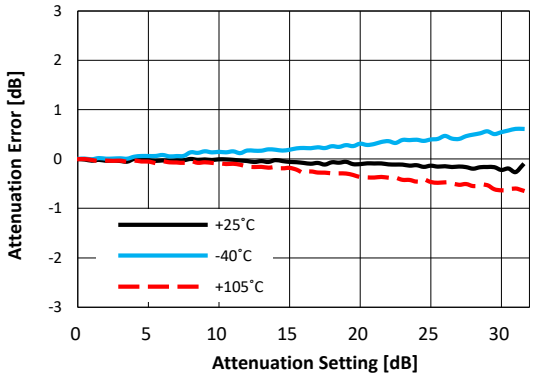
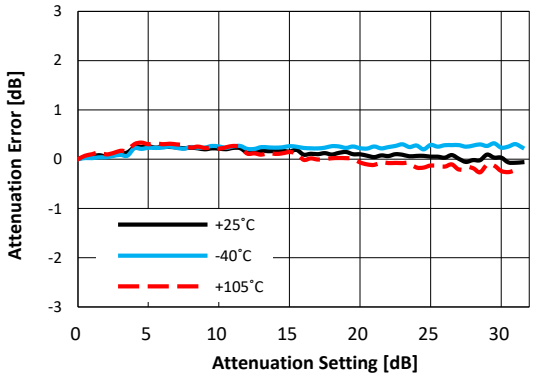


Figure 41. Attenuation Error at 3.5GHz vs Temperature

Over All Attenuation States



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:4000 ~ 5000MHz)

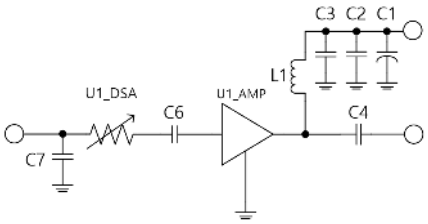
Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 17

Table 16. Typical RF Performance(4000 ~ 5000MHz)

parameter	Frequency			Unit
	4200	4600	4900	MHz
Gain[1]	10.5	9.9	9.4	dB
S11	-13.3	-10.2	-9.3	dB
S22	-13.8	-14.1	-14.8	dB
OIP3[2]	24.7	22.7	21.5	dBm
P1dB	12.8	12.0	11.3	dBm
N.F	4.4	4.8	5.3	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

Table 17. 4000 ~ 5000MHz RF Application Circuit



Application Circuit Values	Frequency band	RF Circuit
		4000MHz ~ 5000MHz
	C6/C4	2pF[1]
	C7	0.3pF[1]
	L1	15nH[1]

1. This value can be changed little by little according to the frequency bond and bandwidth.

Figure 42. Gain vs. Frequency
over Temperature

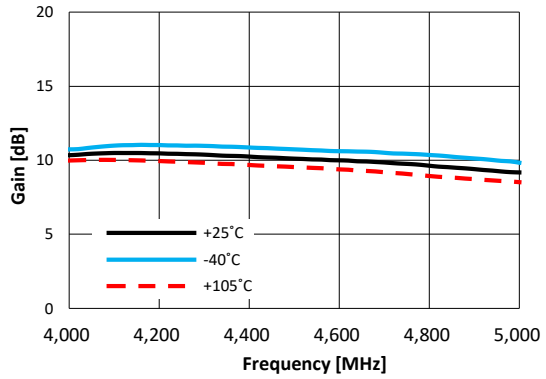


Figure 43. Gain vs. Frequency
over Major Attenuation States

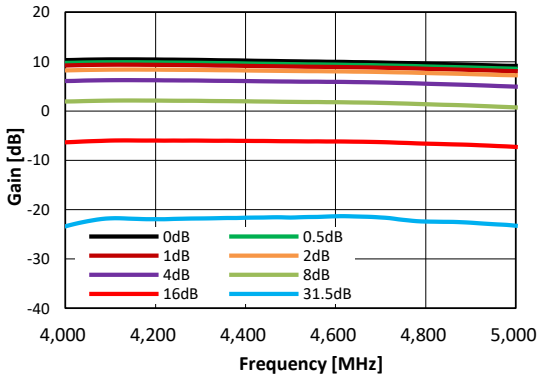


Figure 44. Input Return Loss vs. Frequency
over Major Attenuation States

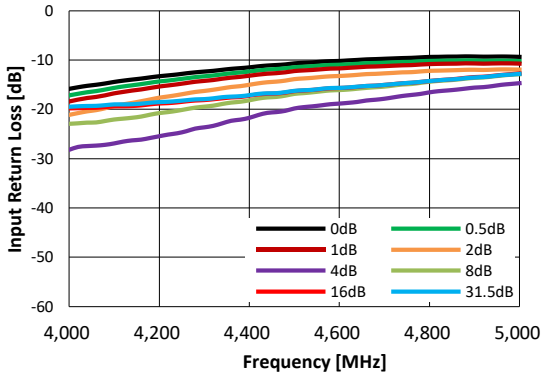
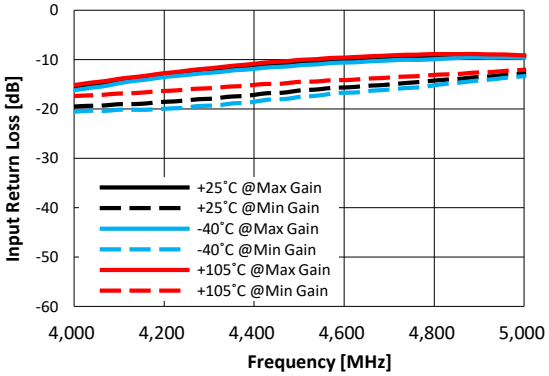


Figure 45. Input Return Loss vs. Frequency
over Temperature (Min / Max Gain State)



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:4000 ~ 5000MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 17

Figure 46. Output Return Loss vs. Frequency
over Major Attenuation States

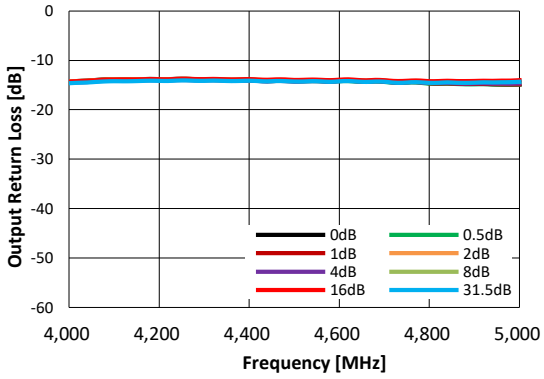
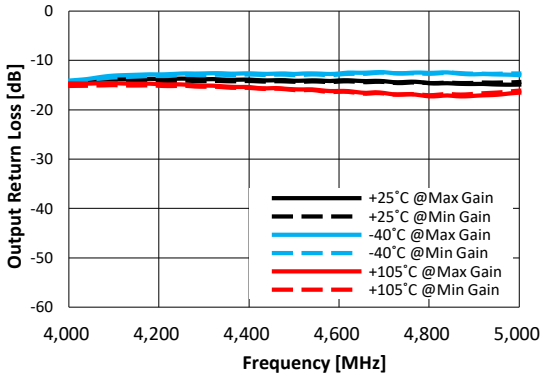


Figure 47. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 48. OIP3 vs. Frequency
Over Temperature (Max Gain State)

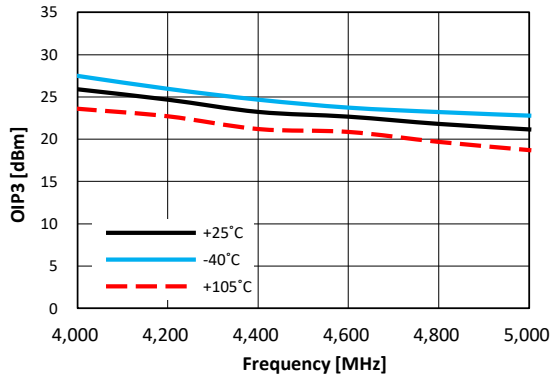


Figure 49. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

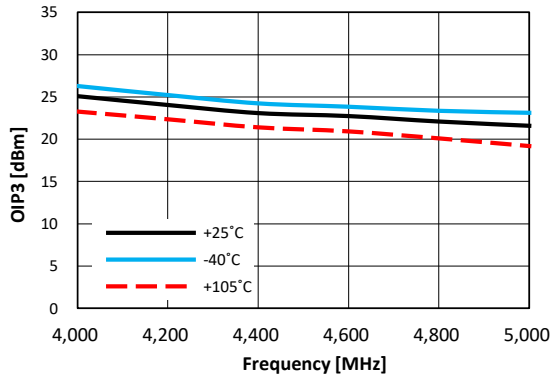


Figure 50. P1dB vs. Frequency
Over Temperature (Max Gain State)

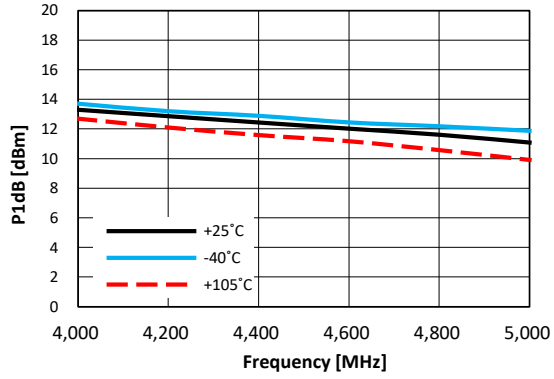
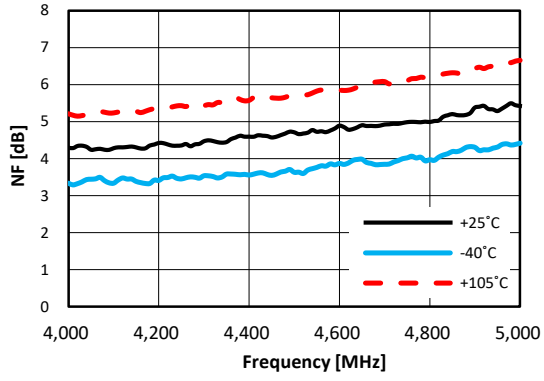


Figure 51. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA305C EVK - PCB (Application Circuit:4000 ~ 5000MHz)

Typical Performance Data @ 25°C and VDD = 3V unless otherwise noted and Application Circuit refer to Table 17

Figure 52. Attenuation Error vs Frequency
over Major Attenuation Steps

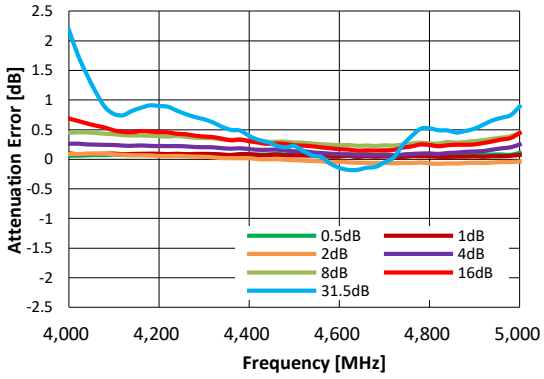


Figure 53. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

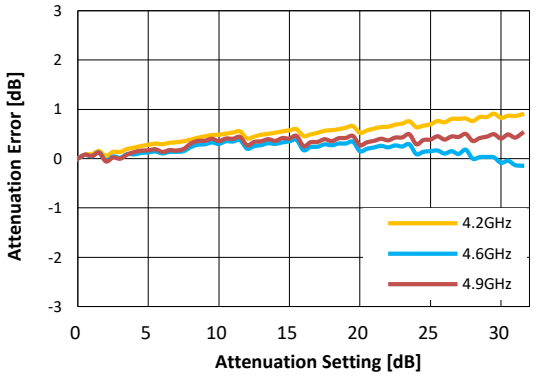


Figure 54. 0.5dB Step Attenuation vs Attenuation Setting
over Major Frequency

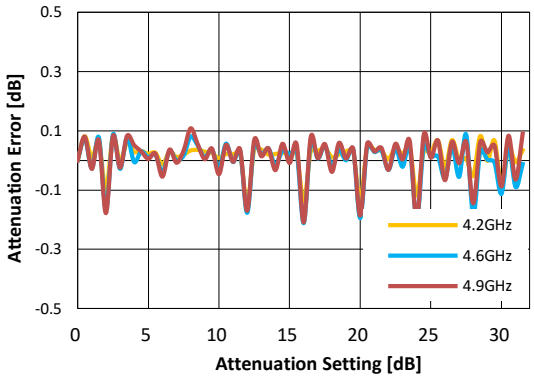


Figure 55. Attenuation Error at 4.2GHz vs Temperature
Over All Attenuation States

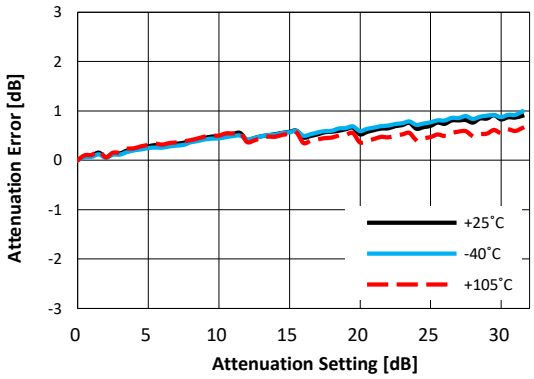


Figure 56. Attenuation Error at 4.6GHz vs Temperature
Over All Attenuation States

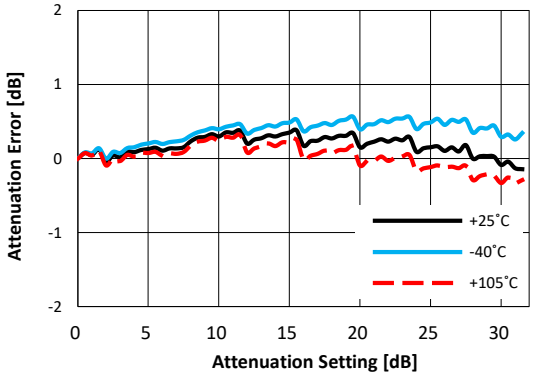


Figure 57. Attenuation Error at 4.9GHz vs Temperature
Over All Attenuation States

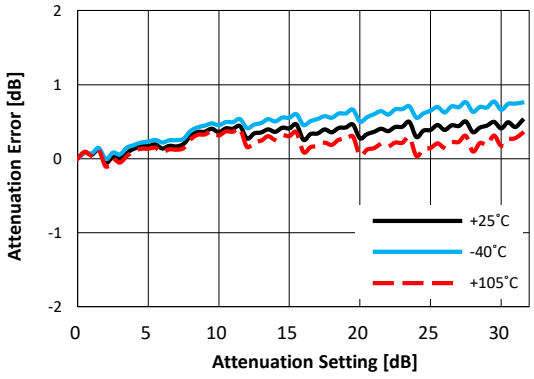


Figure 58. Evaluation Board Schematic

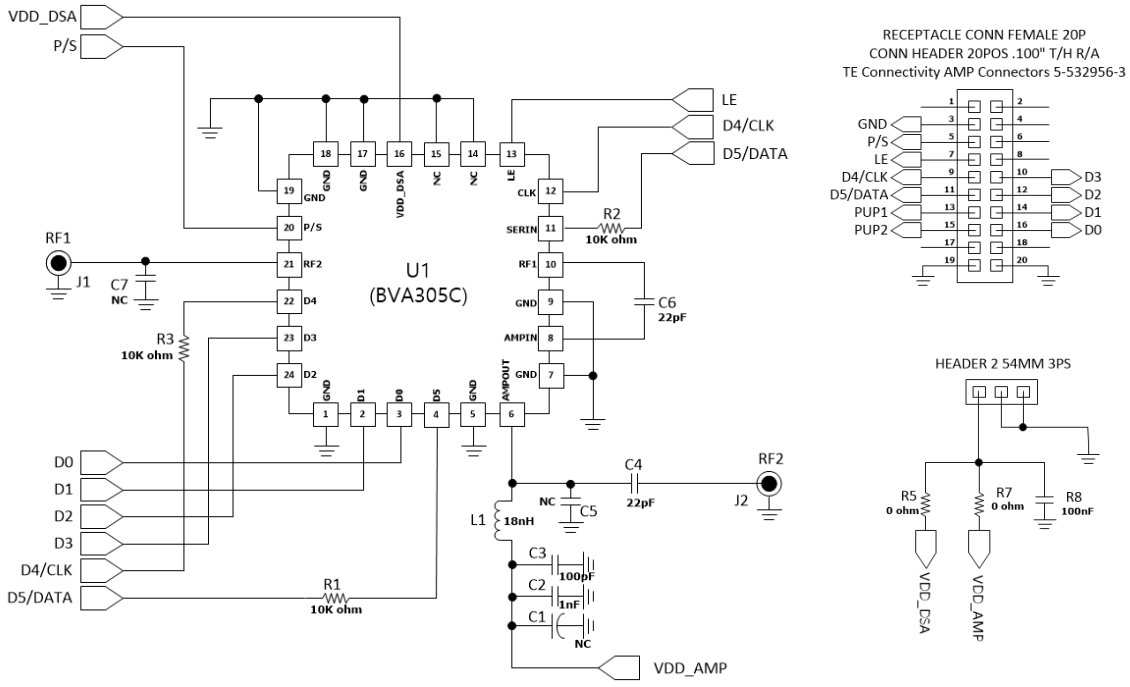


Figure 59. Evaluation Board PCB

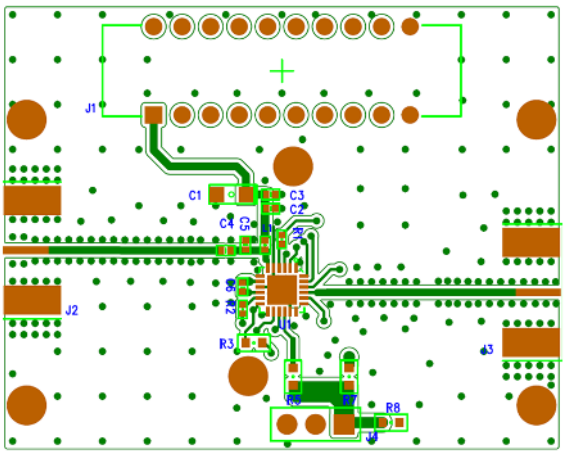


Table 18. Application Circuit

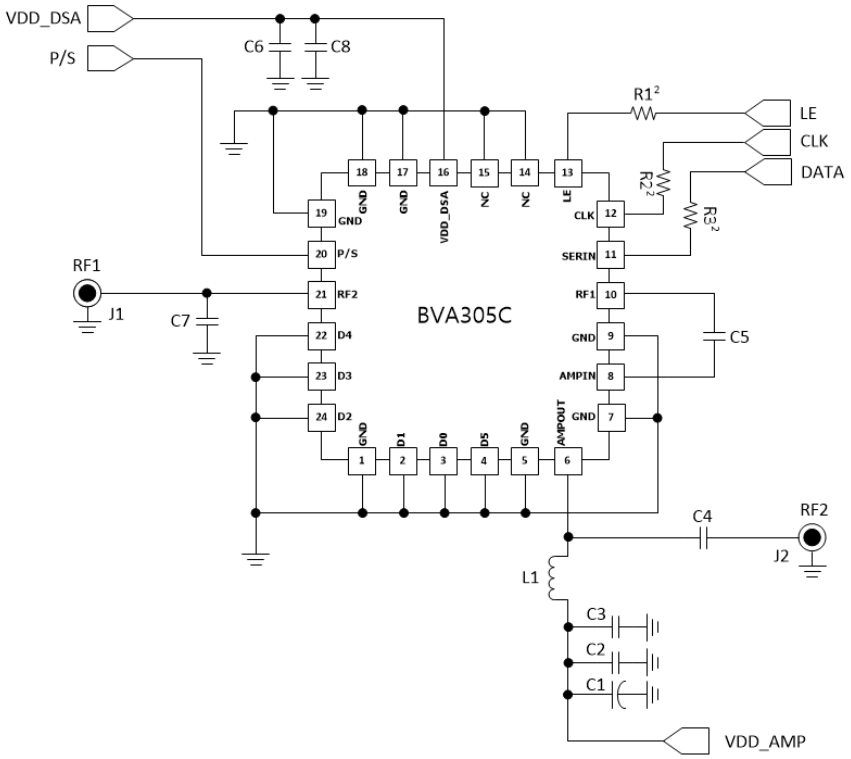
Application Circuit Values Example			
Frequency band	IF Circuit	RF Circuit	RF Circuit
C6/C4	2.2nF	22pF	2pF
C7	NC	NC	0.3pF
L1	330nH	18nH	15nH

Table 19. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C4,C6	2	CAP 0402 22pF J 50V	IF circuit refer to table 18
2	C2	1	CAP 0402 1000pF J 50V	
3	C1	1	TANTAL 3216 10UF 16V	
4	C22	1	TANTAL 3216 0.1uF 35V	
5	L1	1	IND 1608 18nH	IF circuit refer to table 18
6	C3	1	CAP 0402 100pF J 50V	
7	R1,R2	2	RES 1005 J 10K ohm	
8	R3	1	RES 1608 J 10K ohm	
9	R4,R5,R7	3	RES 1608 J 0ohm	
10	J1	1	Receptacle connector	
11	U1	1	QFN4X4_24L_BVA305C	
12	J2,J3	2	SMA_END_LAUNCH	

Notice: Evaluation Board for Marketing Release was set to 800MHz to 4GHz application circuit (Refer to Table 13)

Figure 60. Recommended Serial mode Application Circuit schematic



1. BVA305C is set to default minimum gain state when it is initially powered up. (Maximum attenuation state)
2. Recommended to add the R1/R2/R3 with value of 1k ohm.

Figure 61. Suggested PCB Land Pattern and PAD Layout

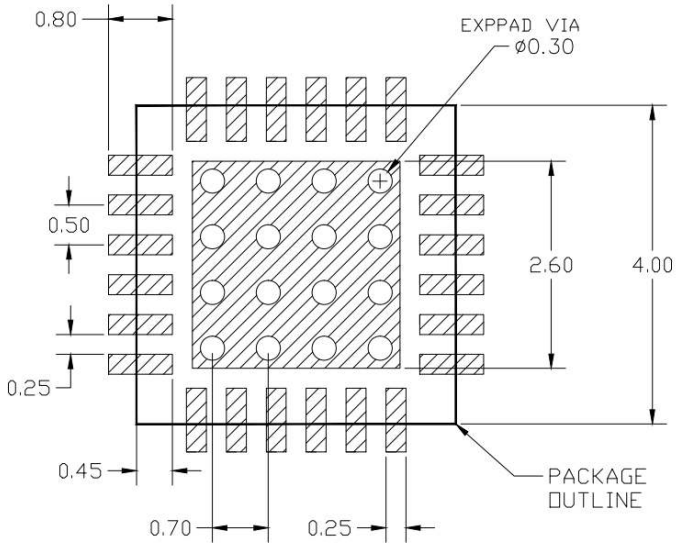
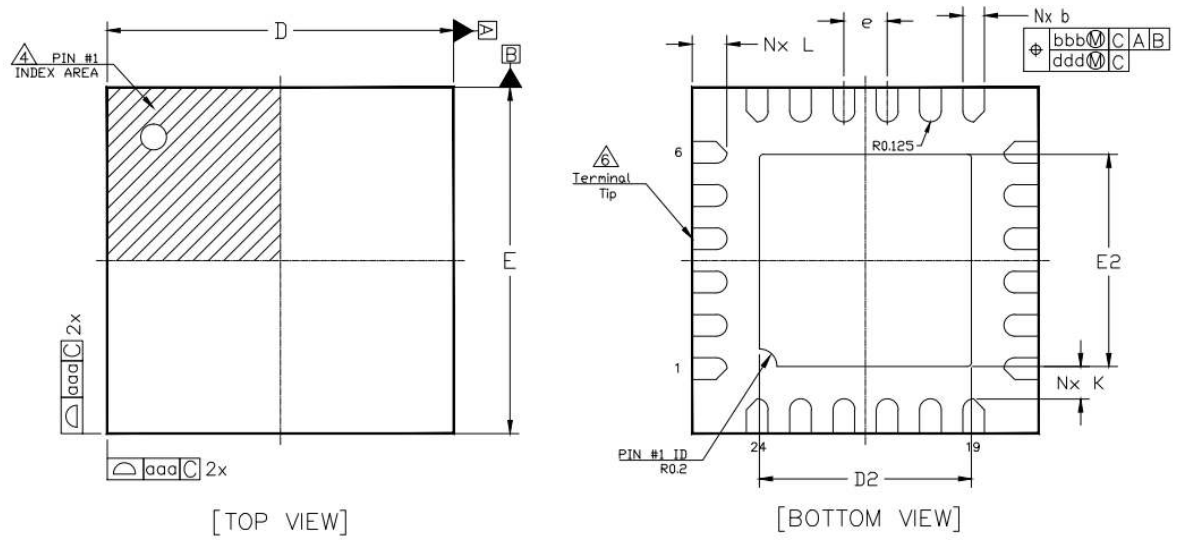


Figure 62. Package Outline Dimension



NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)				
Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.18	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.30	2.45	2.55	
E2	2.30	2.45	2.55	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
ND		6		5
NE		6		5

Figure 63. Evaluation Board PCB Layer Information

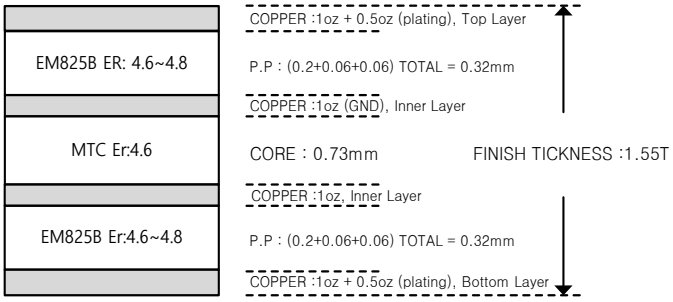
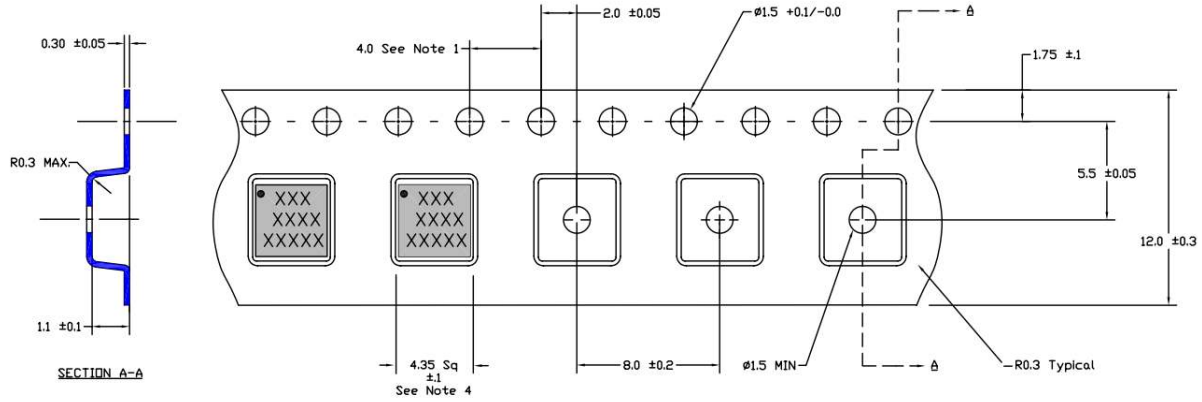


Figure 64. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 65. Package Marking

Marking information:	
BVA305C	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1A
Value:	250V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020

Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**