International
IOR Rectifier

IR20153S & (PbF)

HIGH SIDE DRIVER WITH RECHARGE

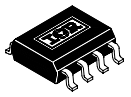
Features

- Floating channel designed for bootstrap operation
  Fully operational up to 150V
  Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout
- Internal recharge FET for bootstrap refresh
- Internal deadtime of 11∝s and 0.8∝s
- CMOS Schmitt-triggered input logic
- Output out of phase with input
- Reset input
- Split pull-up and pull-down gate drive pins
- Also available LEAD-FREE (PbF)

Product Summary

V_{OFFSET}	150V max.
I_O+/-	400mA @ VBS=7V, 1.5A @ VBS=16V
V_{OUT}	5-20V
$t_{on/off}$	1.0 and 0.3 ∝s

Package

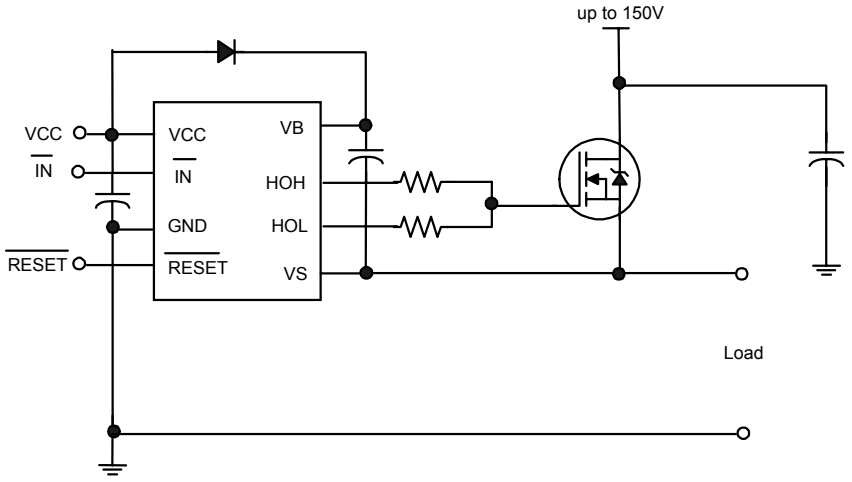


8-Lead SOIC

Description

The IR20153S is a high voltage, high speed power MOSFET driver . Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS output down to 3.3V. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high or low side configuration which operates up to 150 volts.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. This is a stress only rating and operation of the device at these or any conditions exceeding those indicated in the operational sections of this specifications is not implied.

Symbol	Definition	Min.	Max.	Units
V_B	High side driver output stage voltage	-5.0	170	V
V_S	High side floating supply offset voltage	- 8.0	150	
V_{HO}	Output voltage gate high connection	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{IN}	Input voltage (IN and RESET)		-0.3	V_{CC} +0.3
dV/dt	Allowable offset voltage slew rate	—	50	V/nsec
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 2. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND. The VS offset rating is tested with all suppliers biased at Vcc=5V and VBS=7V.

Symbol	Definition	Min.	Max.	Units
V_B	High side driver output stage voltage	V_S + 5	V_S + 20	V
V_S	High side floating supply offset voltage	-1.6	150	
V_{HO}	Output voltage gate high connection	V_S	V_B	
V_{CC}	Supply voltage	5	20	
V_{IN}	Input voltage (IN and RESET)	0	Vcc	
T_A	Ambient temperature	-55	150	°C

Electrical Characteristics

Unless otherwise specified, V_{CC} = 5V, V_{BS} = 7V, V_S = 0V, IN = 0V, RES = 5V, load R = 50Ω, C = 6.8nF (see Figure 3). Unless otherwise noted, these specifications apply for an operating ambient temperature of T_A =25°C.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VCC Supply Characteristics						
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	—	—	4.3	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	2.5	—	—		V_{CC} dropping from 5V
$V_{CCUVHYS}$	V_{CC} supply undervoltage lockout hysteresis	0.01	0.3	0.60		
I_{QCC}	V_{CC} supply current	—	—	400	uA	V_{CC} = 3.6V & 6.5V
VBS Supply Characteristics						
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	—	—	4.3	V	V_{BS} rising from 0V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	2.5	—	—		V_{BS} dropping from 5V
$V_{BSUVHYS}$	V_{BS} supply undervoltage lockout hysteresis	0.01	0.3	0.60		
I_{QBS1}	V_{BS} supply current	—	—	100	∝A	static mode, V_{BS} = 7V, IN = 0V or 5V
I_{QBS2}	V_{BS} supply current	—	—	200	∝A	static mode, V_{BS} = 16V, IN = 0V or 5V
VB. VS Supply Characteristics						
I_{LK}	Offset supply leakage current	—	—	50	∝A	V_B = V_S = 150V
Gate Driver Characteristics						
I_{o+1}	Peak output source current	250	400	—	mA	
I_{o+2}	Peak output source current	800	1500	—	mA	V_{BS} = 16V
t_{r1}	Output rise time	—	0.2	0.4	∝sec	
t_{r2}	Output rise time	—	0.1	0.2	∝sec	V_{BS} = 16V
I_{o-1}	Peak output sink current	250	400	—	mA	IN = 5V
I_{o-2}	Peak output sink current	800	1500	—	mA	V_{BS} = 16V, IN = 5V
t_{f1}	Output fall time	—	0.2	0.4	∝sec	IN = 5V
t_{f2}	Output fall time	—	0.1	0.2	∝sec	V_{BS} = 16V, IN = 5V
t_{on}	Input-to-Output Turn-on propogation delay (50% input level to 10% output level)	—	1.0	2.0	∝sec	
t_{off}	Input-to-Output Turn-off propogation delay (50% input level to 90% output level)	—	0.3	0.9	∝sec	
$t_{res,off}$	RES-to-Output Turn-off propogation delay (50% input level to 90% [t_{phl}] output levels)	—	0.3	0.9	∝sec	

Electrical Characteristics

Unless otherwise specified, V_{CC} = 5V, V_{BS} = 7V, V_S = 0V, IN = 0V, RES = 5V, load R = 50Ω, C = 6.8nF (see Figure 3). Unless otherwise noted, these specifications apply for an operating ambient temperature of T_A =25°C.

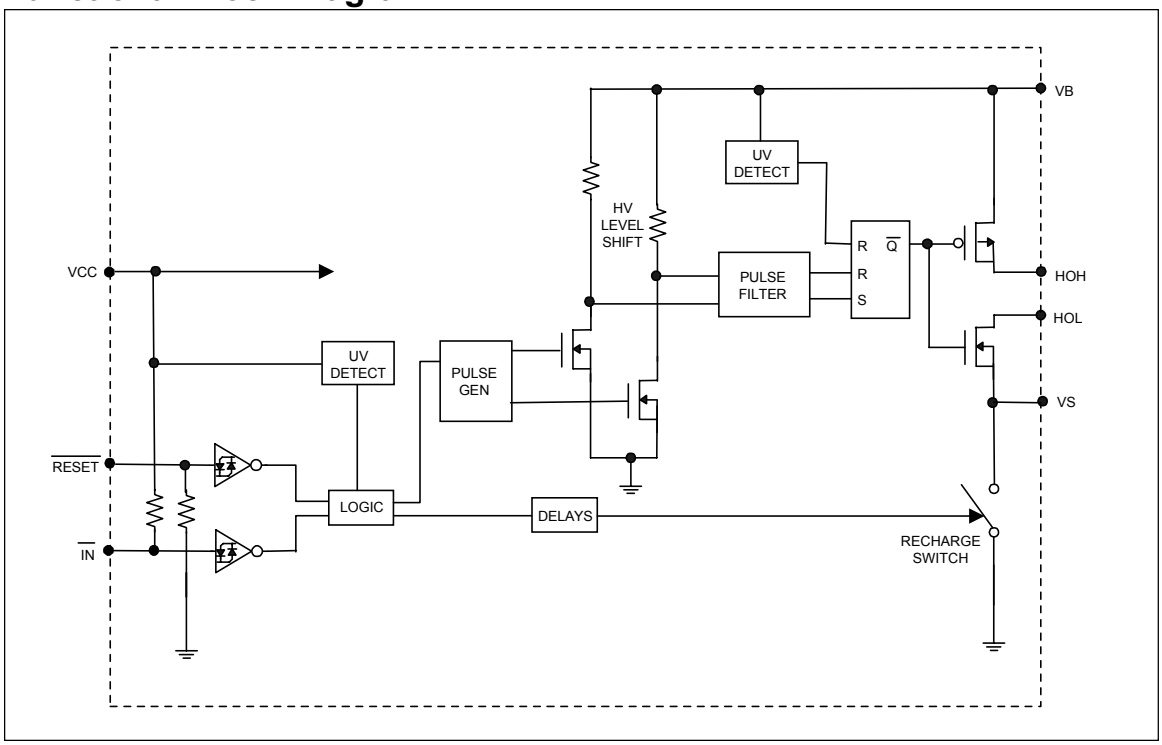
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Gate Driver Characteristics cont.						
$t_{res,on}$	RES-to-Output Turn-On Propogation Delay (50% input level to 10% [t_{plh}] output levels)	-	1.0	2.0	∝sec	
Input Characteristics						
V_{INH}	High Logic Level Input Threshold	3	-	-	V	
V_{INL}	Low Logic Level Input Threshold	-	-	1.4	V	
R_{IN}	High Logic Level Input Resistance	40	100	220	kΩ	
V_{H_RES}	High Logic Level RES Input Threshold	3	-	-	V	
V_{L_RES}	Low Logic Level RES Input Threshold	-	-	1.4	V	
R_{RES}	High Logic Level RES Input Resistance	40	100	220	kΩ	
Recharge Characteristics (see Figure 3a)						
t_{on_rech}	Recharge Transistor Turn-On Propogation Delay	7	11	15	∝sec	V_S = 5V
t_{off_rech}	Recharge Transistor Turn-Off Propogation Delay	-	0.3	0.9	∝sec	
V_{RECH}	Recharge Output Transistor On-State Voltage Drop	-	-	1.2	V	I_S = 1mA, IN = 5V
Deadtime Characteristics						
DT_{HOFF}	High Side Turn-Off to Recharge gate Turn-On	7	11	15	∝sec	
DT_{HON}	Recharge gate Turn-Off to High Side Turn-On0.	0.4	0.8	1.5	∝sec	

A True table for V_{CC}, VBS, RESET, IN, H_O and RechFET is shown as follows. This truth table is for ACTIVE LOW IN.

V_{CC}	VBS	RESET-	IN-	H_O	RechFET
$<V_{ccUVLO-}$	$<V_{BSUVLO-}$	HIGH	HIGH	OFF	ON
$<V_{ccUVLO-}$	$<V_{BSUVLO-}$	HIGH	LOW	OFF	ON
$<V_{ccUVLO-}$	$<V_{BSUVLO-}$	LOW	HIGH	OFF	ON
$<V_{ccUVLO-}$	$<V_{BSUVLO-}$	LOW	LOW	OFF	ON
$<V_{ccUVLO-}$	$>V_{BSUVLO+}$	HIGH	HIGH	OFF	ON
$<V_{ccUVLO-}$	$>V_{BSUVLO+}$	HIGH	LOW	OFF	ON
$<V_{ccUVLO-}$	$>V_{BSUVLO+}$	LOW	HIGH	OFF	ON
$<V_{ccUVLO-}$	$>V_{BSUVLO+}$	LOW	LOW	OFF	ON
$>V_{ccUVLO+}$	$<V_{BSUVLO-}$	HIGH	HIGH	OFF	ON
$>V_{ccUVLO+}$	$<V_{BSUVLO-}$	HIGH	LOW	OFF	OFF
$>V_{ccUVLO+}$	$<V_{BSUVLO-}$	LOW	HIGH	OFF	ON
$>V_{ccUVLO+}$	$<V_{BSUVLO-}$	LOW	LOW	OFF	ON
$>V_{ccUVLO+}$	$>V_{BSUVLO+}$	HIGH	HIGH	OFF	ON[1]
$>V_{ccUVLO+}$	$>V_{BSUVLO+}$	HIGH	LOW	ON	OFF[1]
$>V_{ccUVLO+}$	$>V_{BSUVLO+}$	LOW	HIGH	OFF	ON[1]
$>V_{ccUVLO+}$	$>V_{BSUVLO+}$	LOW	LOW	OFF	ON[1]

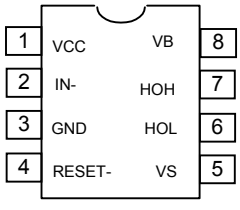
RESET = HIGH indicates that high side MOSFET is allowed to be turned on.
RESET = LOW indicates that high side MOSFET is OFF.
IN = LOW indicates that high side MOSFET is on.
IN = HIGH indicates that high side MOSFET is off.
RechFET = ON indicates that the recharge MOSFET is on.
RechFET = OFF indicates that the recharge MOSFET is off.
[1] Note: Refer to the RESET functionality graph of Figure 7, for VCC and VBS voltage ranges under which the functionality is normal.

Functional Block Diagram



Lead Definitions and Assignments

Symbol	Description
VCC	Driver Supply
IN-	Driver Control Signal Input
GND	Ground
RESET	Driver Enable Signal Input
VS	MOSFET Source Connection
H_{OL}	MOSFET Gate Low Connection
H_{OH}	MOSFET Gate High Connection
VB	Driver Output Stage Supply



8-Lead SOIC

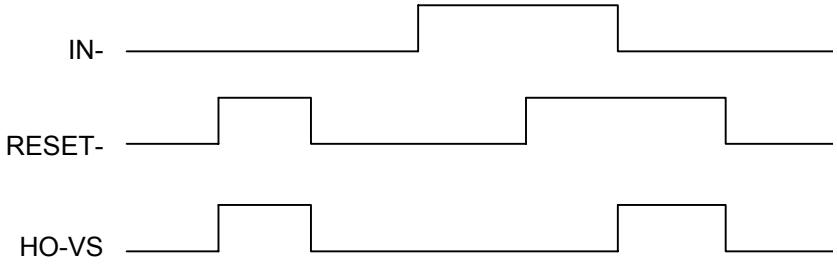


Figure 1. Input/Output Functional Diagram

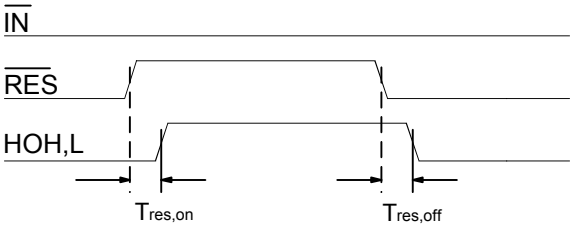


Figure 1a. Reset Timing Diagram

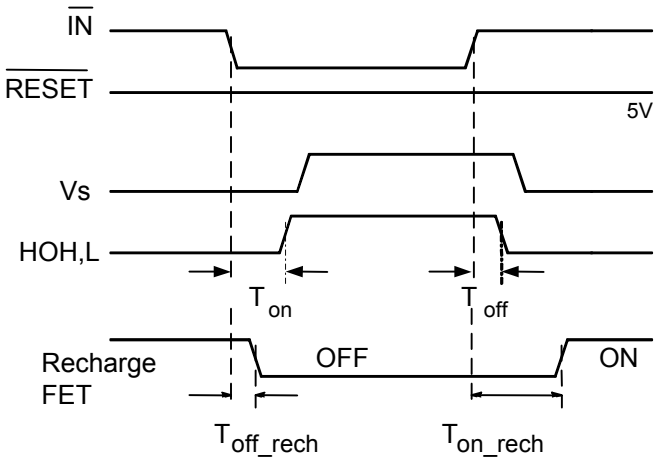


Figure 2. Input/Output Timing Diagram

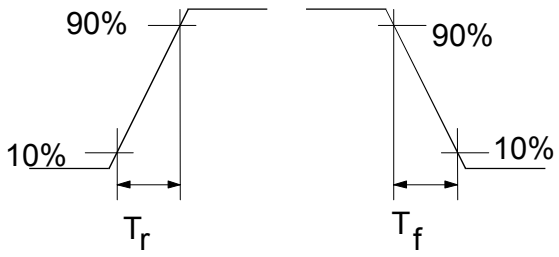


Figure 2a. Output Timing Diagram

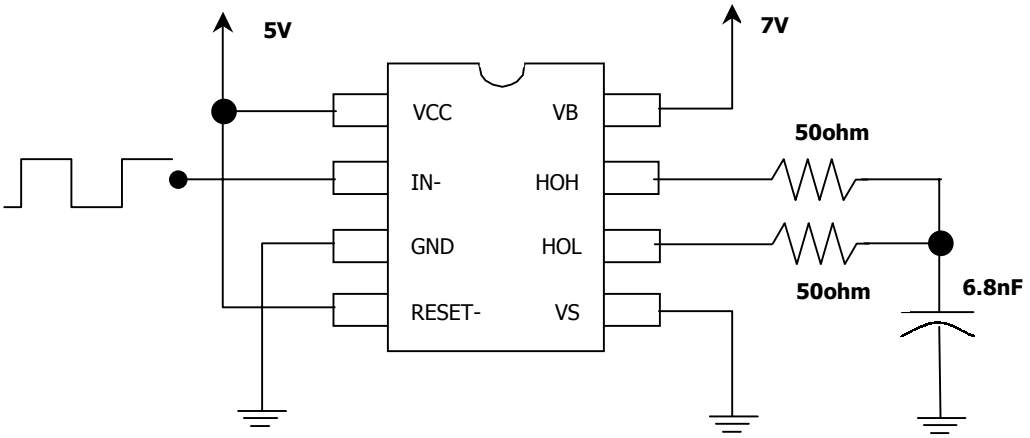


Figure 3. Switching Time Test Circuit

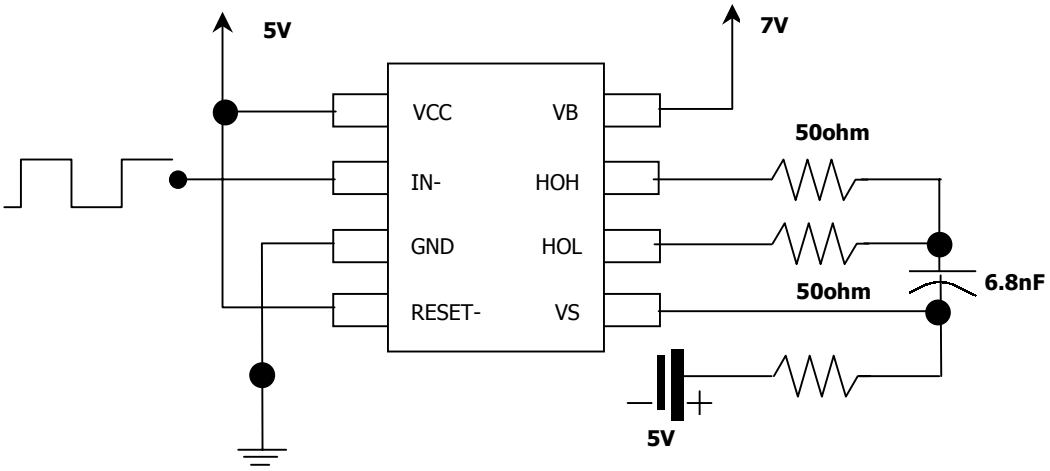


Figure 3a. Ton_rech and Toff_rech Test Circuit

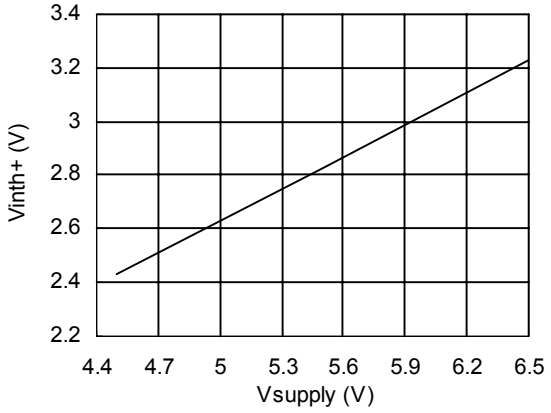


Figure 4. Positive Input and Reset Threshold Voltage vs. Vsupply

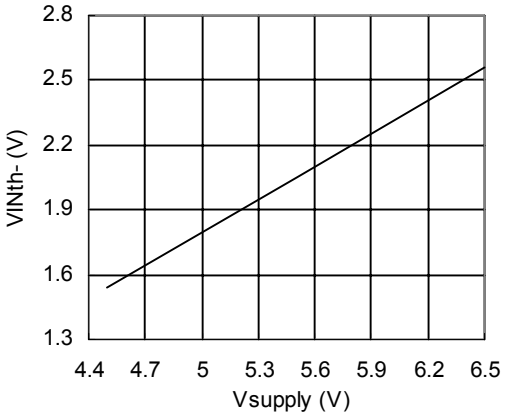


Figure 5. Negative Input and Reset Threshold Voltage vs. Vsupply

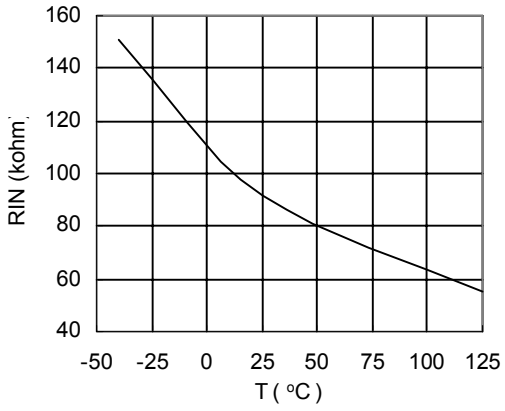


Figure 6. Input and Reset Impedance vs. Temperature

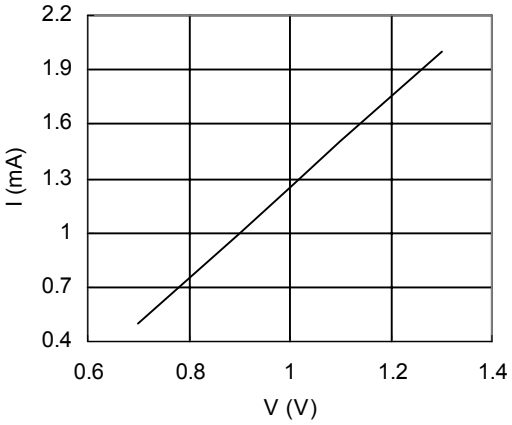


Figure 7. Recharge FET I-V Curve

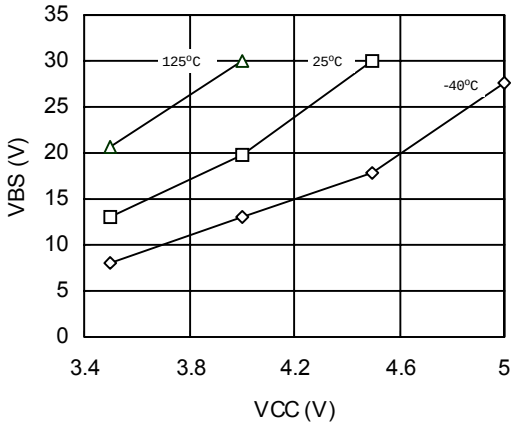


Figure 8. Reset Functionality

This graph explains the functionality limitation as a function of VCC, VBS and temperature. Each curve on the graph represents VCC Vs. VBS, for a particular temperature. For each particular temperature and VCC, the output is non-functional for any value of VBS above the drawn curve. But for any value of VBS below the curve the functionality is fine.

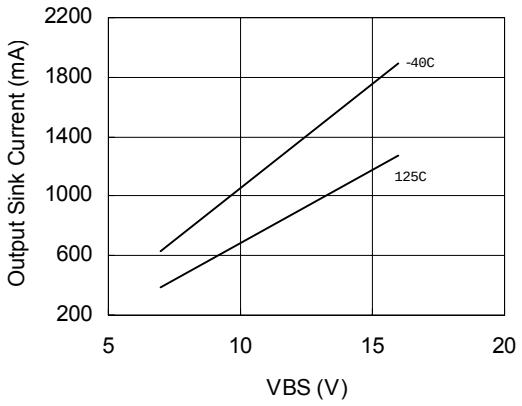


Figure 9. Output Sink Current vs. VBS

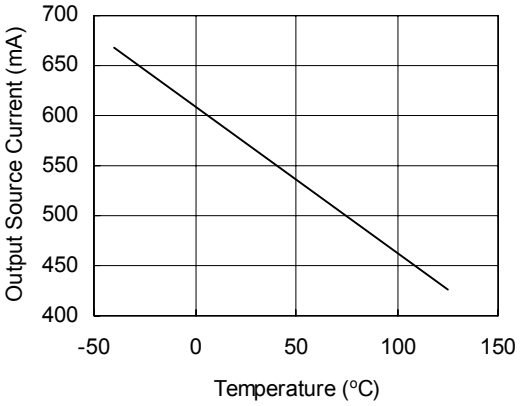


Figure 10. Output Source Current vs. Temperature, VBS=7V

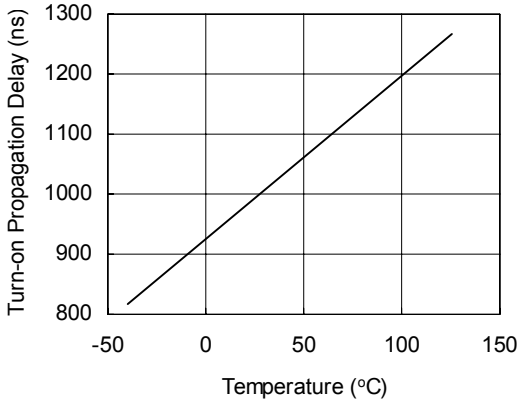


Figure 11. Turn-on Propagation Delay vs. Temperature, VBS=7V

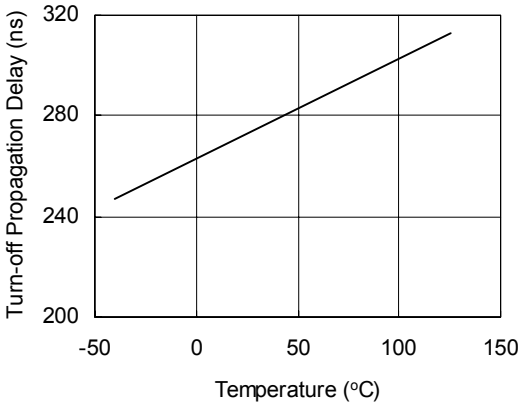


Figure 12. Turn-off Propagation Delay vs. Temperature, VBS=7V

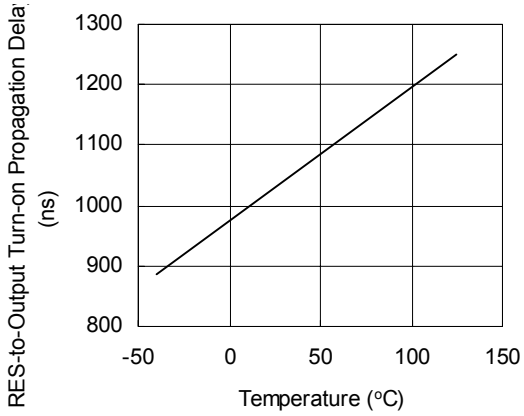


Figure 13. RES-to-Output Turn-on Propagation Delay vs. Temperature, VBS=7V

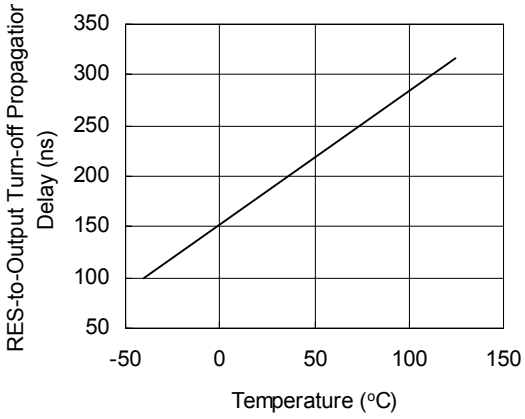


Figure 14. RES-to-Output Turn-off Propagation Delay vs. Temperature, VBS=7V

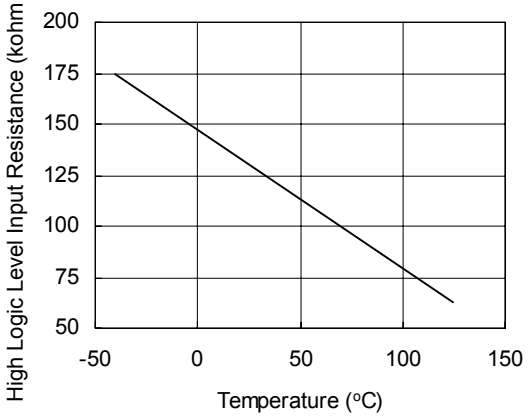


Figure 15. High Logic Level Input Resistance vs. Temperature, VBS=7V

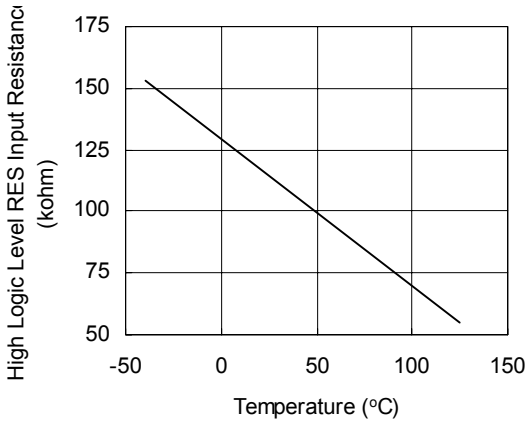


Figure 16. High Logic Level RES Input Resistance vs. Temperature, VBS=7V

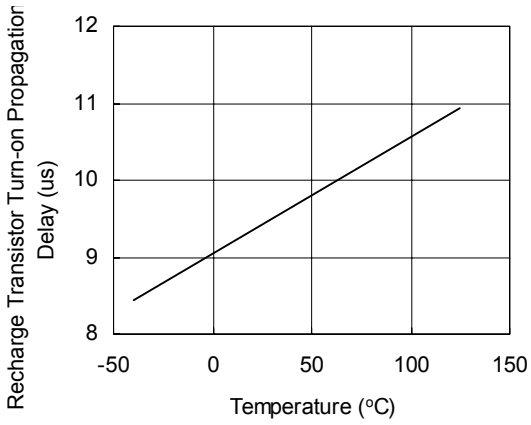


Figure 17. Recharge Transistor Turn-on Propagation Delay vs. Temperature, VBS=7V

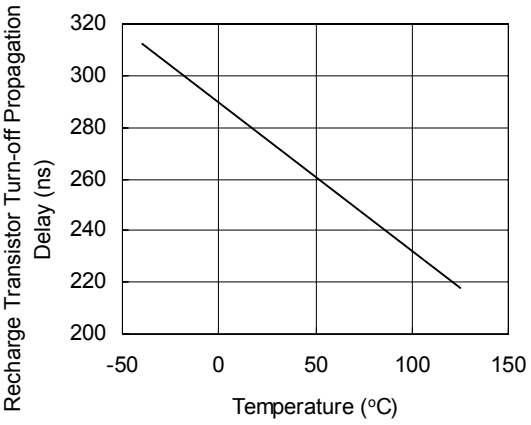


Figure 18. Recharge Transistor Turn-off Propagation Delay vs. Temperature, VBS=7V

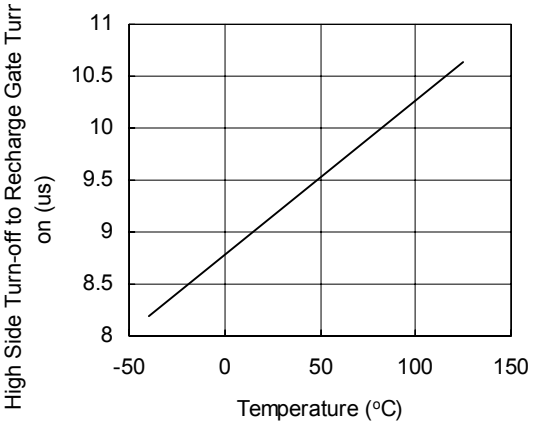


Figure 19. High Side Turn-off to Recharge Gate Turn-on vs. Temperature, VBS=7V

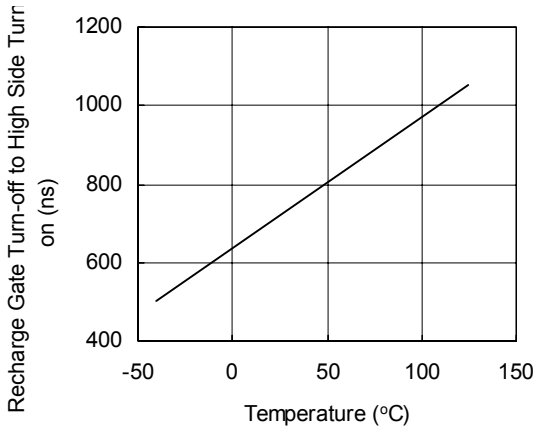
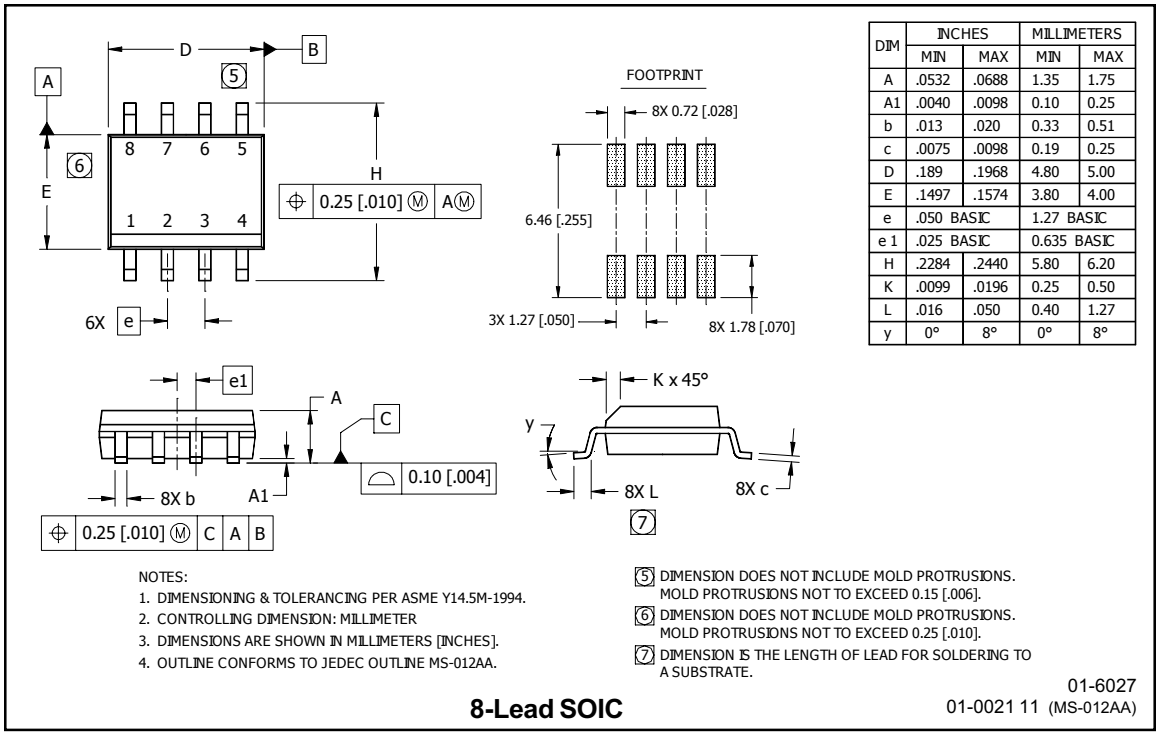


Figure 20. Recharge Gate Turn-off to High Side Turn-on vs. Temperature, VBS=7V

Case outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

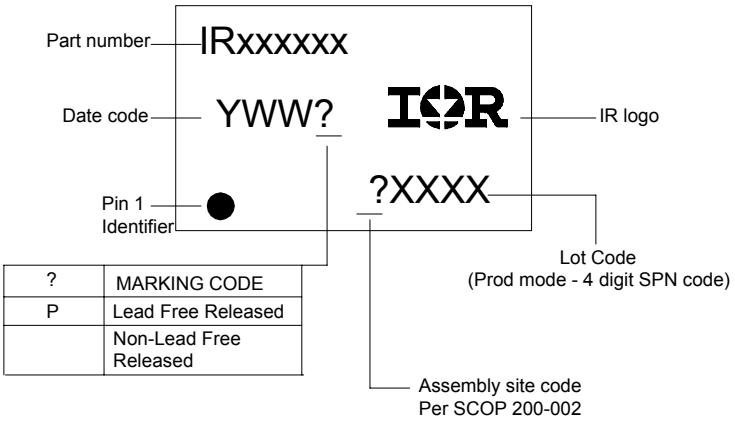
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8-Lead SOIC

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead SOIC IR20153S order IR20153S

Leadfree Part
8-Lead SOIC IR20153S order IR20153SPbF

Thisproduct has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web Site *http://www.irf.com*
Data and specifications subject to change without notice.
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
10/25/2004