NCV8461

Self Protected High Side Driver with Temperature Shutdown and Current Limit

The NCV8461 is a fully protected High−Side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids and other activators. The device is internally protected from an overload condition by an active current limit and thermal shutdown. A diagnostic output reports OFF state open load conditions as well as thermal shutdown.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- CMOS (3 V / 5 V) Compatible Control Input
- Off State Open Load Detection
- Open Drain Diagnostic Output
- Overvoltage Protection
- Undervoltage Shutdown
- Loss of Ground and Loss of V_D Protection
- ESD Protection
- Reverse Battery Protection (with external resistor)
- Very Low Standby Current
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

FEATURE SUMMARY

Overvoltage Protection	V_{OV}	41	V
R_{DSon} (max) T_J = 25°C	R_{ON}	350	mΩ
Output Current Limit (typ)	I_{lim}	1.2	A
Operating Voltage Range	V_{OP}	5 − 34	V

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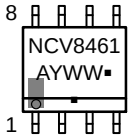
SOIC−8
CASE 751
STYLE 11

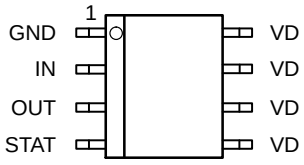
MARKING DIAGRAM



NCV8461 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV8461DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

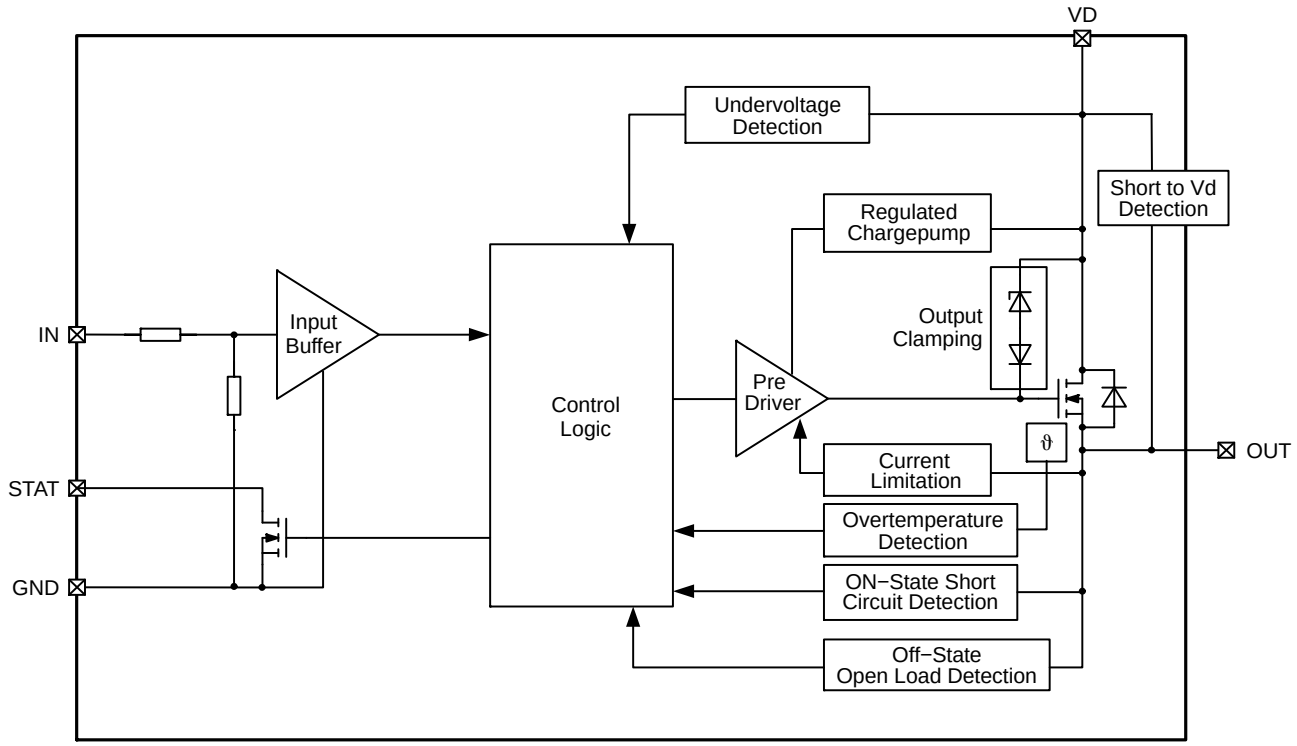


Figure 1. Block Diagram

SO8 PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	GND	Ground
2	IN	Logic Level Input
3	OUT	Output
4	STAT	Status Output
5	V_D	Supply Voltage
6	V_D	Supply Voltage
7	V_D	Supply Voltage
8	V_D	Supply Voltage

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
DC Supply Voltage (Note 1)	V_D	−16	40	V
Peak Transient Input Voltage (Note 1) (Load Dump 38 V, V_D = 14 V, ISO7637−2 pulse5)	V_{peak}		52	V
Input Voltage	V_{in}	−10	16	V
Input Current	I_{in}	−5	5	mA
Output Current (Note 1)	I_{out}	−	Internally Limited	A
Status Current	I_{status}	−5	5	mA
Power Dissipation Tc = 25°C (Note 1)	P_{tot}	1.5		W
Electrostatic Discharge (Note 1) (HBM Model 100 pF / 1500 Ω) Input All Other Pins		 ±1.5 ±5		DC kV kV
Single Pulse Inductive Load Switching Energy (Note 1) V_D = 13.5 V; I_L = 0.5 A, T_{Jstart} = 150°C	E_{AS}	−	300	mJ
Operating Junction Temperature	T_J	−40	+150	°C
Storage Temperature	$T_{storage}$	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Not subjected to production testing

Table 2. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max. Value	Units
Thermal Resistance (Note 2) Junction−to−Soldering Point Junction−to−Ambient (6 cm square pad size, FR−4, 2 oz Cu)	 R_{thJS} R_{thJA}	 31 84	°C/W

2. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance. See spec table and page 6 for further reverse battery information.

Table 3. ELECTRICAL CHARACTERISTICS (V_D = 13.5 V; −40°C < T_J < 150°C unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Operating Supply Voltage	V_D		5	−	34	V
Undervoltage Shutdown	V_{UV}				5	V
Undervoltage Restart	V_{UV_Res}				5.5	V
Overvoltage Protection	V_{OV}	I_D = 4 mA	41			V
On Resistance	R_{ON}	I_{out} = 0.3 A; 6 V < V_D < 40 V, T_J = 25°C I_{out} = 0.3 A; 6 V < V_D < 40 V, T_J = 150°C		250 450	350 700	mΩ
Standby Current	I_D	Off State, V_{in} = V_{out} = 0 V On State; V_{in} = 5 V, I_{out} = 0 A		13 1	35 1.7	μA mA
Output Leakage Current	$I_{L(off)}$				12	μA
INPUT CHARACTERISTICS						
Input Voltage − Low	V_{in_low}				0.8	V
Input Voltage − High	V_{in_high}		2.2			V
Input Hysteresis Voltage	V_{hyst}			0.3		V
Off State Input Current	I_{in_OFF}	V_{in} = 0.7 V	1		10	μA
On State Input Current	I_{in_ON}	V_{in} = 5.0 V	1		10	μA
Input Resistance (Note 3)	R_I		1.5	3.5		KΩ
Input Clamp Voltage	V_{in_cl}	I_{in} = 1 mA I_{in} = −1 mA	14 −18	16 −16	18 −14	V
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	t_{d_on}	to 90% V_{out}, R_L = 47 Ω			140	μs
Turn−Off Delay Time	t_{d_off}	to 10% V_{out}, R_L = 47 Ω			170	μs
Slew Rate On	dV_{out}/dt_{on}	10% to 30% Vout, R_L = 47 Ω			2	V / μs
Slew Rate Off	dV_{out}/dt_{off}	70% to 40% Vout, R_L = 47 Ω			2	V / μs
REVERSE BATTERY (Note 3)						
Reverse Battery	$-V_D$	Requires a 150 Ω Resistor in GND Connection			32	V
Forward Voltage	V_F	T_J = 150°C, I_S = 200 mA		0.6		V
STATUS PIN CHARACTERISTICS						
Status Output Voltage Low	V_{stat_low}	I_{stat} = 1.6 mA, T_J = −40°C to 25°C I_{stat} = 1.6 mA, T_J = 150°C (Note 3)			0.4 0.6	V
Status Leakage Current	$I_{stat\_leakage}$	V_{stat} = 5 V			10	μA
Status Invalid Time After Positive Input Slope	$T_{d(STAT)}$			300	700	μs
Status Clamp Voltage	V_{stat_cl}	I_{stat} = 1 mA I_{stat} = −1 mA		10 −1.4		V
PROTECTION FUNCTIONS (Note 4)						
Temperature Shutdown (Note 3)	T_{SD}		150	175	200	°C
Temperature Shutdown Hysteresis (Note 3)	T_{SD_hyst}			10		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles. AEC Q100−12 results available upon request.

Table 3. ELECTRICAL CHARACTERISTICS (V_D = 13.5 V; −40°C < T_J < 150°C unless otherwise specified)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
PROTECTION FUNCTIONS (Note 4)						
Output Current Limit Initial Peak	I_{lim}	T_J = −40°C, V_D = 20 V (Note 3) T_J = 25°C T_J = 150°C (Note 3)	 0.7	 1.2	2	A
Repetitive Short Circuit Current Limit	$I_{lim(SC)}$	T_J = T_{Jt} (Note 3)		1		A
Switch Off Output Clamp Voltage	V_{clamp}	I_D = 4 mA, V_{in} = 0 V	V_D − 41	V_D − 47		V
DIAGNOSTICS CHARACTERISTICS						
Short Circuit Detection Voltage	$V_{OUT(SC)}$			2.8		V
Openload Off State Detection Threshold	V_{OL}	V_{in} = 0 V	1.5		3.5	V
Openload Detection Current	$I_{L(OL)}$			5		μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not subjected to production testing
4. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper hardware/software strategy. If the devices operates under abnormal conditions this hardware/software solutions must limit the duration and number of activation cycles. AEC Q100−12 results available upon request.

Table 4. STATUS PIN TRUTH TABLE

Conditions	Input	Output	Status
Normal Operation	L H	L H	H H
Short Circuit to GND	L H	L L*	H L
Short to $V_{D\ (OFF\ State)}$	L H	H H	L H
Current Limitation	L H	L H**	H H
Overtemperature	L H	L L	H L
OFF State Open Load	L H	H H	L H

* Output = “L”; V_{OUT} < 2 V typ.
** Output = “H”; V_{OUT} > 2 V typ.

REVERSE BATTERY PROTECTION

The NCV8461 provides reverse battery protection up to 32 V. This protection requires a Resistor in the GND path. The recommended GND resistor is 150 Ω, but a variety of resistor values can be chosen for this purpose. The graph below shows the considerations and constraints for selection of the GND resistor. Figure 2 shows the power dissipation in the GND resistor during a 32 V reverse battery event on the left axis, while the right axis shows the voltage drop across the GND resistor while in normal operation. The far right side of the graph is grayed out to indicate that the voltage drop across the resistor is too high, and the part will not be able to turn on with a standard 5 V on the input pin. Selection of the optimal GND resistor requires balancing the power dissipation considerations while in a reverse battery event, with the turn on capability of the input signal during normal operation.

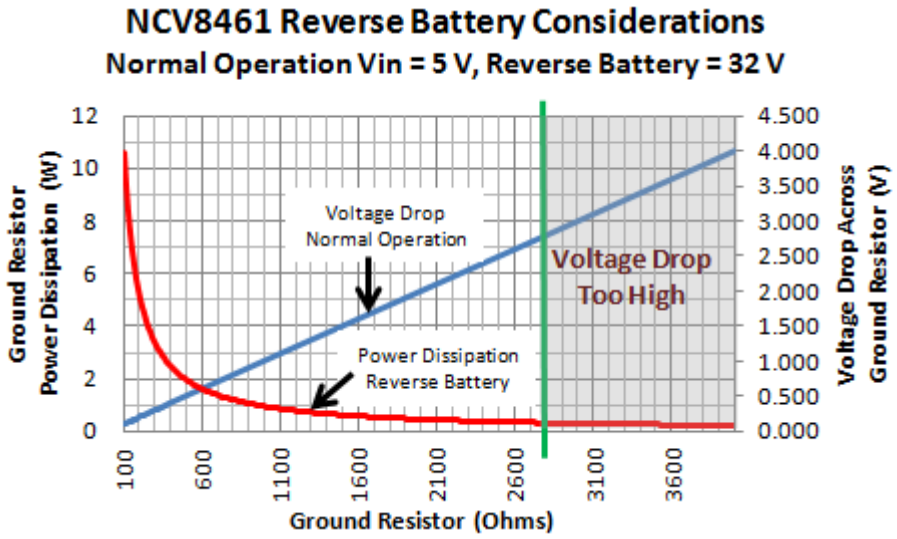


Figure 2. Reverse Battery Considerations

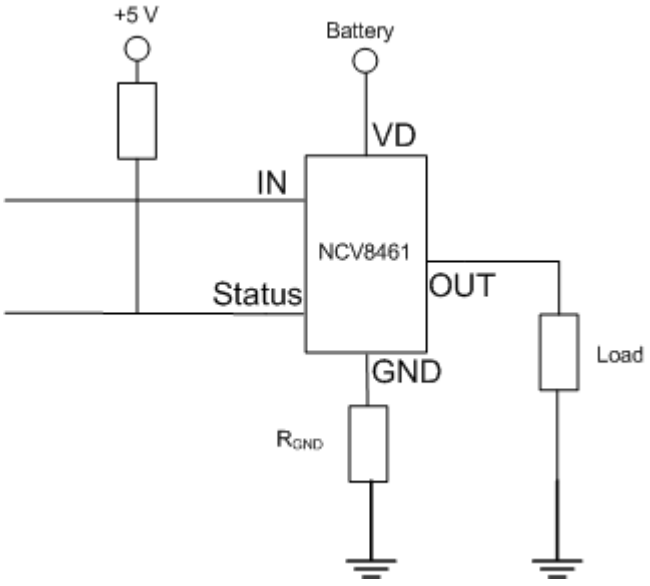


Figure 3. Reverse Battery Protection Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

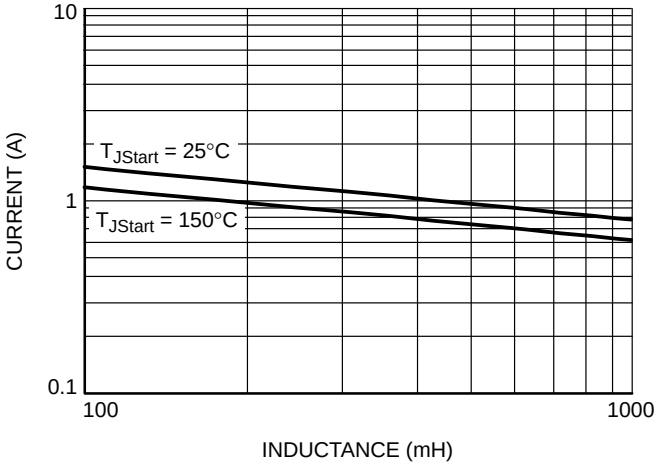


Figure 4. Maximum Single Pulse Switch Off Current vs. Inductance

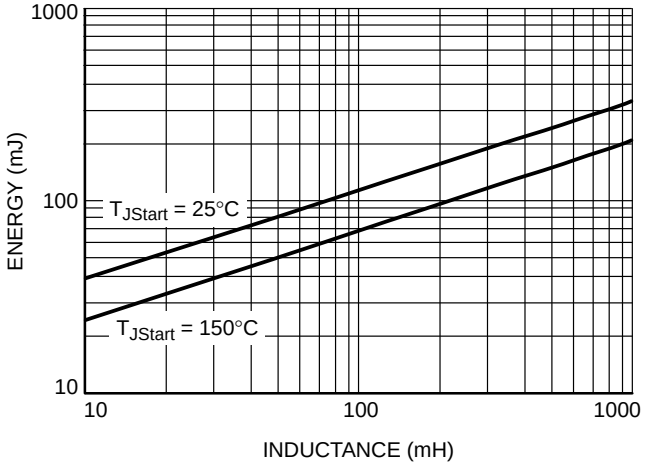


Figure 5. Maximum Single Pulse Switch Off Energy vs. Inductance

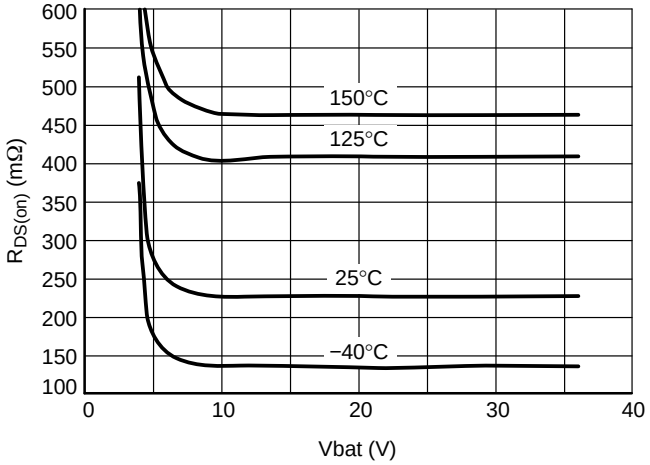


Figure 6. $R_{DS(on)}$ Over Temp and Battery

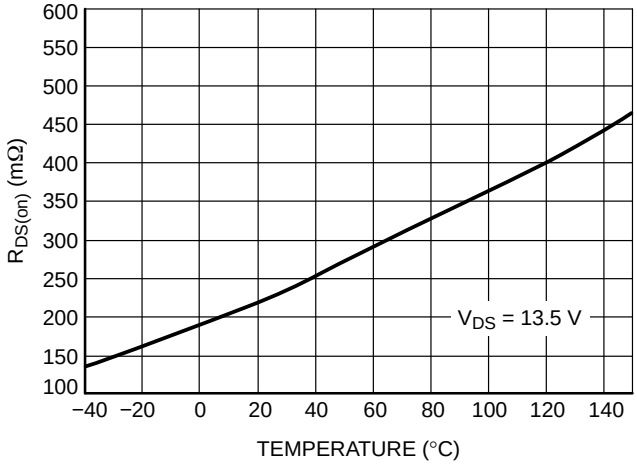


Figure 7. $R_{DS(on)}$ vs. Temperature

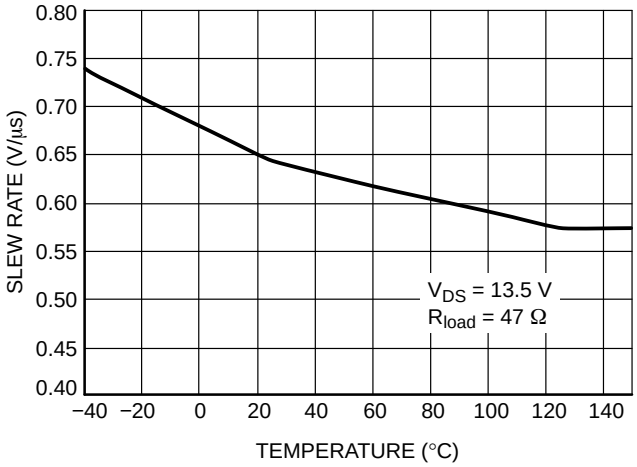


Figure 8. Slew Rate On vs. Temperature

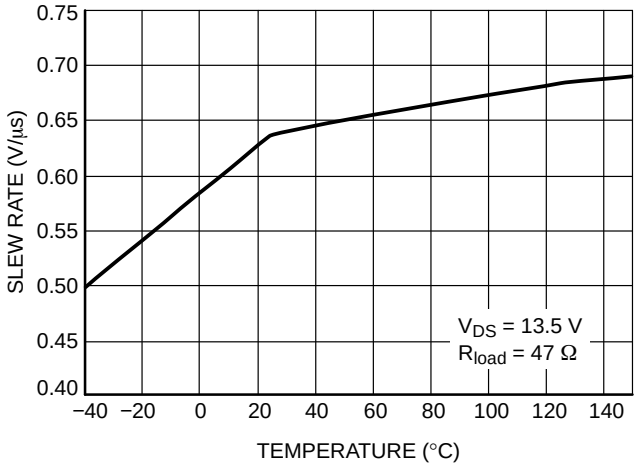


Figure 9. Slew Rate Off vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

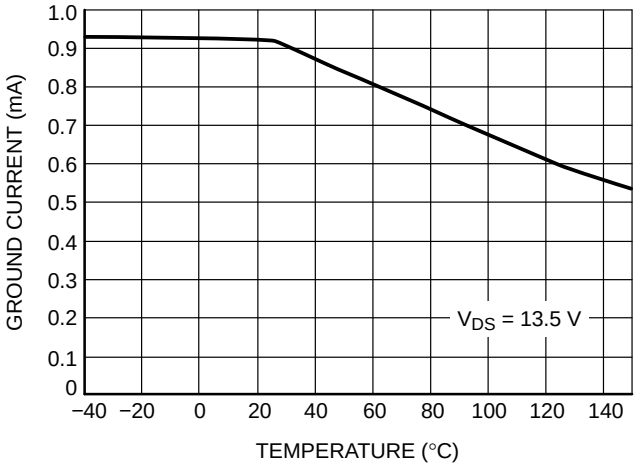


Figure 10. On State Ground Current vs. Temp

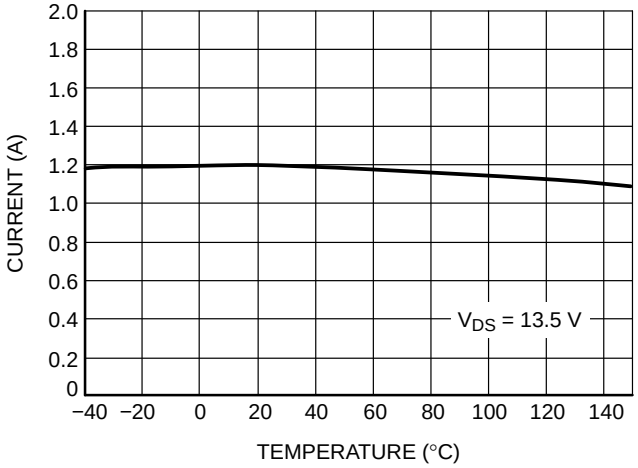


Figure 11. Current Limit vs. Temperature

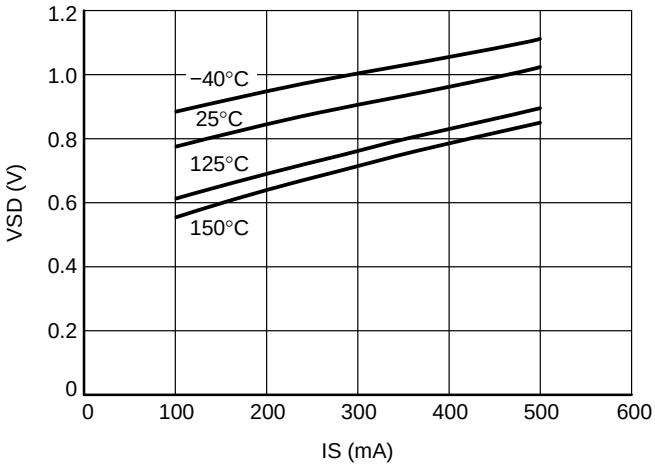


Figure 12. Body Diode

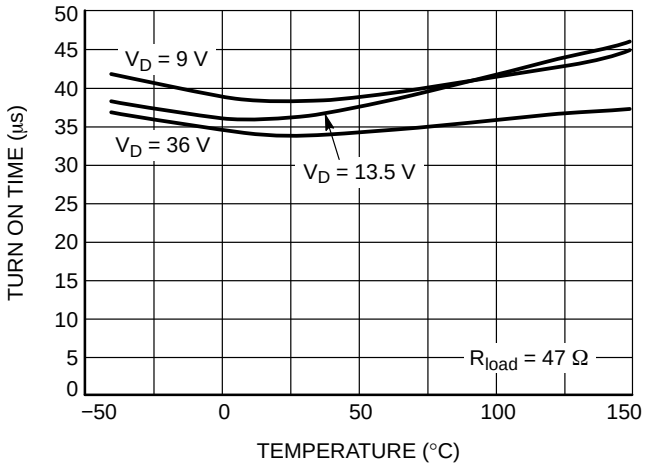


Figure 13. Turn On Time vs. Temperature

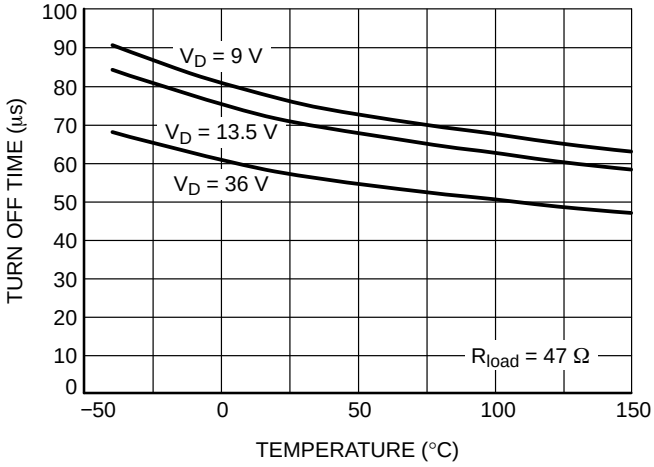


Figure 14. Turn Off Time vs. Temperature

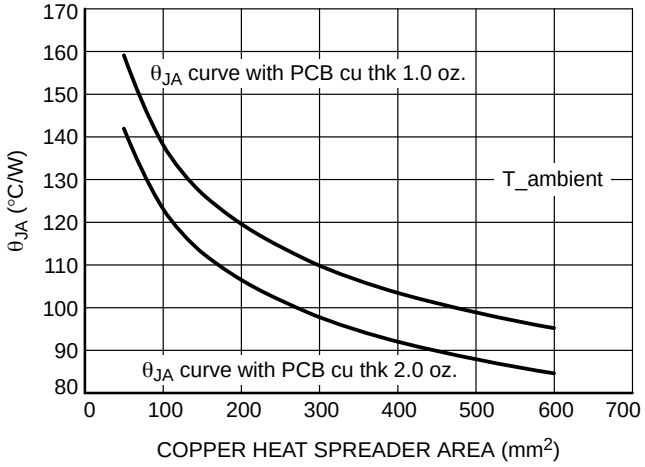


Figure 15. Junction−to−Ambient Thermal Resistance vs. Copper Area

TYPICAL PERFORMANCE CHARACTERISTICS

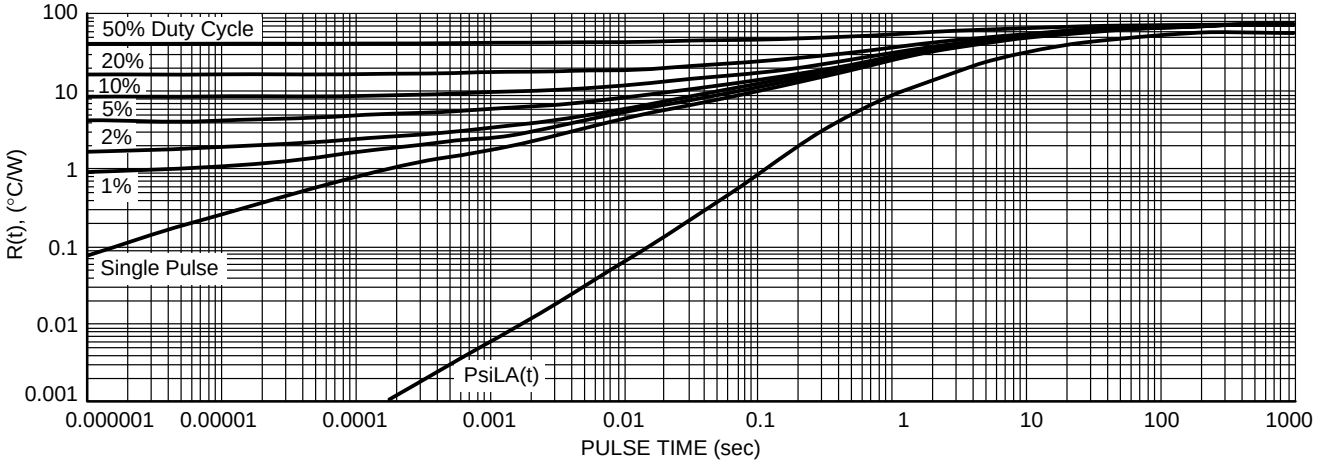


Figure 16. Junction to Ambient Transient Thermal Impedance (600 mm^2 Copper Area)

ISO 7637-2:2011 (E) PULSE TEST RESULTS

ISO 7637−2:2011(E) Test Pulse	Test Severity Levels, 13.5 V System		Delays and Impedance	# of Pulses or Test Time	Pulse / Burst Rep. Time
	III	IV			
1	−112	−150	2 ms, 10 Ω	500 pulses	0.5 s
2a	+55	+112	0.05 ms, 2 Ω	500 pulses	0.5 s
3a	−165	−220	0.1 μs, 50 Ω	1 h	100 ms
3b	+112	+150	0.1 μs, 50 Ω	1 h	100 ms

ISO 7637−2:2011(E) Test Pulse	Test Results	
	III	IV
1	C	C
2a	C	E
3a	C	C
3b	C	C

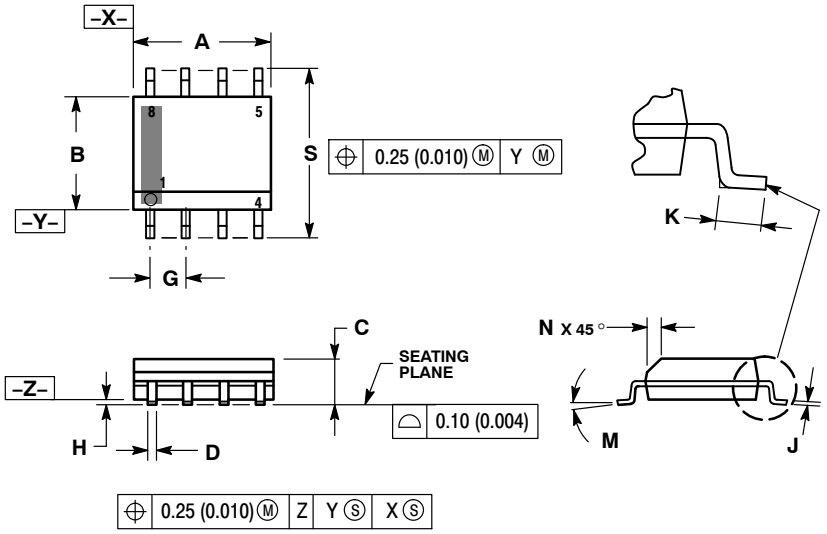
Class	Functional Status
C	One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

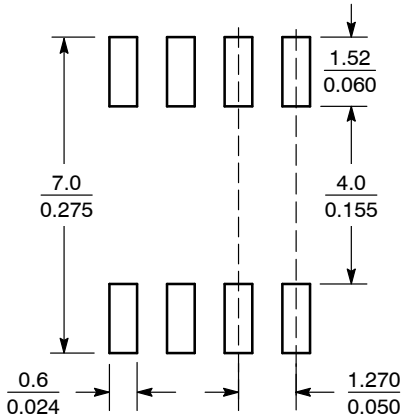
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

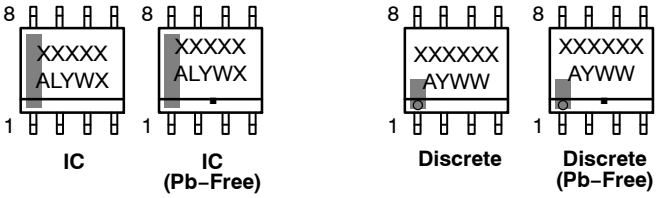
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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